

# 9342 93S42

## CARRY LOOKAHEAD GENERATOR

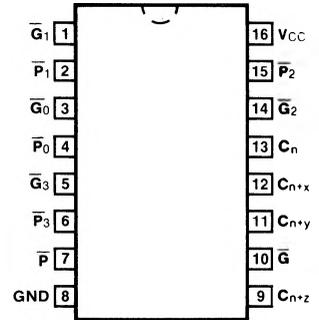
**DESCRIPTION** — The '42 is a high speed lookahead carry generator. It is generally used with the 9341 (54/74181) 4-bit arithmetic logic unit to provide high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the TTL family.

- PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S
- MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS

**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	9342PC, 93S42PC		9B
Ceramic DIP (D)	A	9342DC, 93S42DC	9342DM, 93S42DM	7B
Flatpak (F)	A	9342FC, 93S42FC	9342FM, 93S42FM	4L

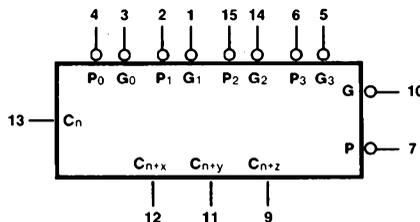
### CONNECTION DIAGRAM PINOUT A



**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
C <sub>n</sub>	Carry Input	1.0/1.0	1.25/1.25
G <sub>0</sub> , G <sub>2</sub>	Carry Generate Inputs (Active LOW)	7.0/7.0	8.75/8.75
G <sub>1</sub>	Carry Generate Input (Active LOW)	8.0/8.0	10/10
G <sub>3</sub>	Carry Generate Input (Active LOW)	4.0/4.0	5.0/5.0
P <sub>0</sub> , P <sub>1</sub>	Carry Propagate Inputs (Active LOW)	4.0/4.0	5.0/5.0
P <sub>2</sub>	Carry Propagate Input (Active LOW)	3.0/3.0	3.75/3.75
P <sub>3</sub>	Carry Propagate Input (Active LOW)	2.0/2.0	2.5/2.5
C <sub>n</sub> + x — C <sub>n</sub> + z	Carry Outputs	20/10	25/12.5
G	Carry Generate Output (Active LOW)	20/10	25/12.5
P	Carry Propagate Output (Active LOW)	20/10	25/12.5

### LOGIC SYMBOL



V<sub>CC</sub> = Pin 16  
GND = Pin 8

**FUNCTIONAL DESCRIPTION** — The '42 lookahead carry generator accepts up to four pairs of active LOW Carry Propagate ( $\overline{P}_0 - \overline{P}_3$ ) and Carry Generate ( $\overline{G}_0 - \overline{G}_3$ ) signals and an active HIGH Carry input ( $C_n$ ) and provides anticipated active HIGH carries ( $C_{n+x}$ ,  $C_{n+y}$ ,  $C_{n+z}$ ) across four groups of binary adders. The '42 also has active LOW Carry Propagate ( $\overline{P}$ ) and Carry Generate ( $\overline{G}$ ) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$

$$\overline{P} = \overline{P_3 P_2 P_1 P_0}$$

Also, the '42 can be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections (Figure a) to and from the ALU to the lookahead carry generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 93S41.

**TRUTH TABLE**

INPUTS									OUTPUTS				
$C_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$C_{n+x}$	$C_{n+y}$	$C_{n+z}$	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
X			X	X	X	X	H	H				H	
X			X	X	H	H	H	X				H	
X			H	H	H	X	H	X				H	
H			H	X	H	X	H	X				H	
X			X	X	X	X	L	X				L	
X			X	X	L	X	X	L				L	
X			L	X	X	L	X	L				L	
L			X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

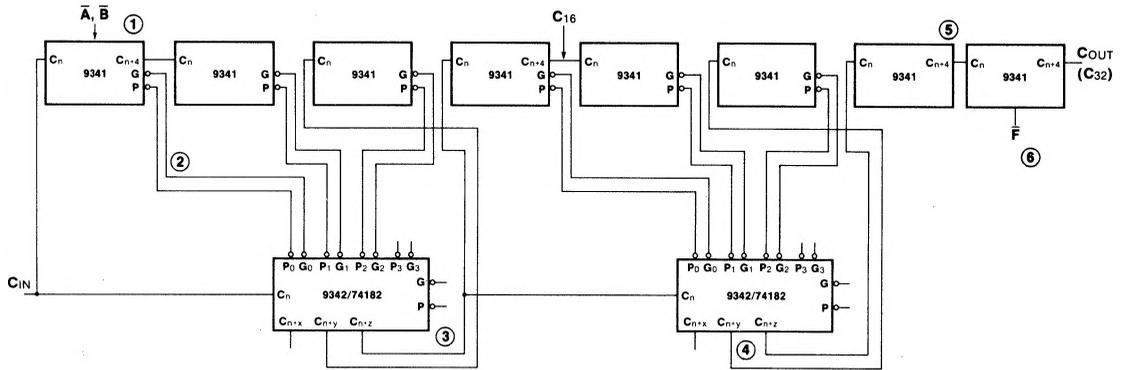
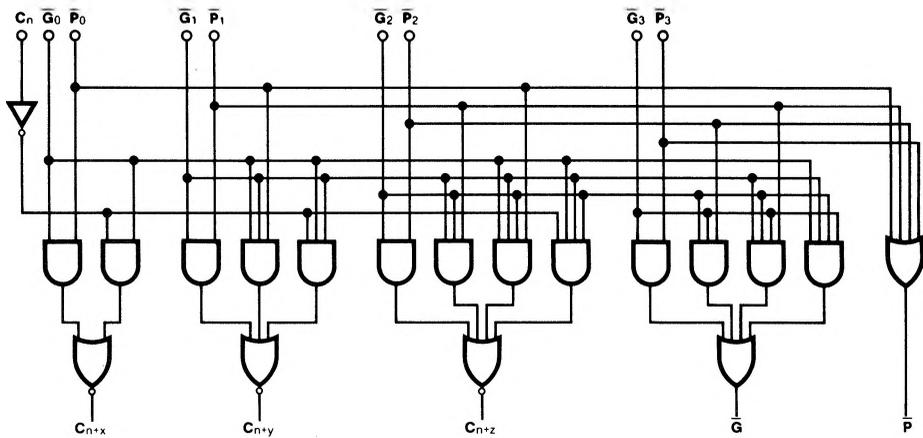


Fig. a 32-Bit ALU with Ripple Carry Between 16-Bit Lookahead ALUs

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)							
SYMBOL	PARAMETER	93XX		93S		UNITS	CONDITIONS
		Min	Max	Min	Max		
I <sub>OS</sub>	Output Short Circuit Current	-40	-100	-40	-100	mA	V <sub>CC</sub> = Max
I <sub>CCH</sub>	Power Supply Current (All Outputs HIGH)	XM	35	45		mA	V <sub>CC</sub> = Max; $\overline{P}_3, \overline{G}_3 = 4.5\text{ V}$ All Other Inputs = Gnd
		XC	39				
I <sub>CCL</sub>	Power Supply Current (All Outputs LOW)	XM	65	80		mA	V <sub>CC</sub> = Max $\overline{G}_0, \overline{G}_1, \overline{G}_2 = 4.5\text{ V}$ All Other Inputs = Gnd
		XC	72				
AC CHARACTERISTICS: V <sub>CC</sub> = +5.0 V, T <sub>A</sub> = +25° C (See Section 3 for waveforms and load configurations)							
SYMBOL	PARAMETER	93XX		93S		UNITS	CONDITIONS
		C <sub>L</sub> = 15 pF R <sub>L</sub> = 400 Ω		C <sub>L</sub> = 15 pF			
		Min	Max	Min	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay C <sub>n</sub> to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	16 19	10 11.5	ns	Figs. 3-1, 3-5 $\overline{P}_0, \overline{P}_1, \overline{P}_2 = \text{Gnd}$ $\overline{G}_0, \overline{G}_1, \overline{G}_2 = 4.5\text{ V}$		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{P}_0, \overline{P}_1$ , or $\overline{P}_2$ to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	13 14	7.0 7.0	ns	Figs. 3-1, 3-4 $\overline{P}_x = \text{Gnd}$ (if not under test) C <sub>n</sub> , $\overline{G}_0, \overline{G}_1, \overline{G}_2 = 4.5\text{ V}$		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{G}_0, \overline{G}_1$ , or $\overline{G}_2$ to C <sub>n+x</sub> , C <sub>n+y</sub> , C <sub>n+z</sub>	13 14	7.0 7.0	ns	Figs. 3-1, 3-4 $\overline{G}_x = 4.5\text{ V}$ (if not under test) C <sub>n</sub> , $\overline{P}_0, \overline{P}_1, \overline{P}_2 = \text{Gnd}$		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{P}_1, \overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$	16 19	7.5 10.5	ns	Figs. 3-1, 3-5 $\overline{P}_x = \text{Gnd}$ (if not under test) $\overline{G}_n, C_n = 4.5\text{ V}$		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{G}_n$ to $\overline{G}$	16 19	7.5 10.5	ns	Figs. 3-1, 3-5 $\overline{G}_x = 4.5\text{ V}$ (if not under test) $\overline{P}_1, \overline{P}_2, \overline{P}_3 = \text{Gnd}$		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{P}_n$ to $\overline{P}$	16 19	6.5 10	ns	Figs. 3-1, 3-5 $\overline{P}_x = \text{Gnd}$ (if not under test)		