National Semiconductor

PRELIMINARY

HPC46083MH
High-Performance microController Emulator

General Description

The HPC46083MH is the emulator device for the HPC16083 and is a member of the HPC™ family of High Performance microControllers. Each member of the family has the same core CPU with a unique memory and I/O configuration to suit specific applications. The HPC46083MH has 8k bytes of on-chip EPROM. The HPC46083MH is a two chip system packaged in a dual cavity ceramic LDCC type package, with a lid on top, and a UV quartz window on bottom. Within the package is an HPC46083 and UV-erasable EPROM with port recreation logic. The EPROM die allows the HPC to function normally, while executing code out of the EPROM. The HPC46083MH may be programmed using a programming card to adapt the part to a normal 27C64 EPROM programmer. The part will function as the normal HPC, and the use of the EPROM should be transparent to the user. The only system design consideration is that pin 5 is V_{PP}, not V_{CC}, and should be tied to V_{CC} during normal operation. Pin 26 should also be tied to V_{CC}.

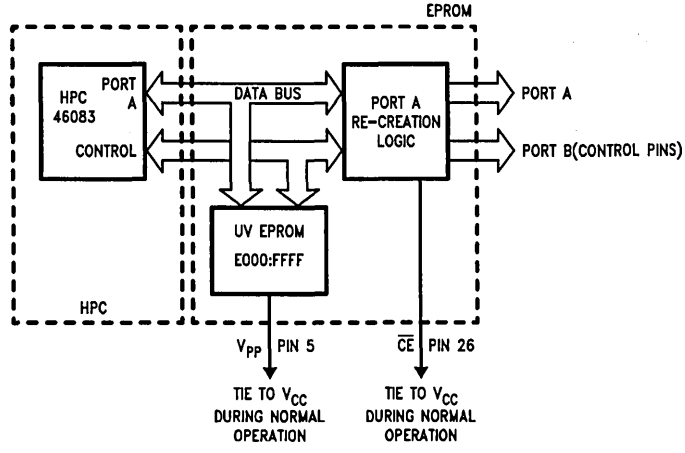
The HPC devices are complete microcomputers on a single chip. All system timing, internal logic, RAM, and I/O are provided on the chip to produce a cost effective solution for high performance applications. On-chip functions such as UART, up to eight 16-bit timers with 4 input capture registers, vectored interrupts, WATCHDOG™ logic and MICROWIRE/PLUS™ provide a high level of system integration. The ability to address up to 64k bytes of external memory enables the HPC to be used in powerful applications typically performed by microprocessors and expensive peripheral chips.

The HPC46083MH is available in 68-pin LDCC type packages.

Features

- HPC family—core features:
  - 16-bit architecture, both byte and word
  - 16-bit data bus, ALU, and registers
  - 64k bytes of external memory addressing
  - FAST—200 ns for fastest instruction when using 20.0 MHz clock
  - High code efficiency—most instructions are single byte
  - 16 x 16 multiply and 32 x 16 divide
  - Eight vectored interrupt sources
  - Four 16-bit timer/counters with 4 synchronous outputs and WATCHDOG logic
  - MICROWIRE/PLUS serial I/O interface
  - CMOS—very low power with two power save modes: IDLE and HALT
- UART—full duplex, programmable baud rate
- Four additional 16-bit timer/counters with pulse width modulated outputs
- Four input capture registers
- 52 general purpose I/O lines (memory mapped)
- 8k bytes of EPROM, 256 bytes of RAM on chip
- Commercial (0°C to +70°C)

Block Diagram (HPC46083 with 8k EPROM shown)



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20 MHz
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	(V_{CC} + 0.5)V to (GND − 0.5)V
ESD	2000V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC_1}	Supply Current $54 + 4 \times f_{in}$	V_{CC} = 5.5V, f_{in} = 20.0 MHz (Note 1)		134	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		62	mA
I_{CC_2}	IDLE Mode Current $0.5 + 1.25 \times f_{in}$	V_{CC} = 5.5V, f_{in} = 20.0 MHz, (Note 1)		26	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz, (Note 1)		3	mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.5V, f_{in} = 0 kHz, (Note 1)		2	mA
		V_{CC} = 2.5V, f_{in} = 0 kHz, (Note 1)		250	μA
INPUT VOLTAGE LEVELS $\overline{RESET}$, NMI, CKI AND WO (SCHMITT TRIGGERED)					
V_{IH_1}	Logic High		0.9 V_{CC}		V
V_{IL_1}	Logic Low			0.1 V_{CC}	V
ALL OTHER INPUTS					
V_{IH_2}	Logic High		0.7 V_{CC}		V
V_{IL_2}	Logic Low			0.2 V_{CC}	V
I_{LI}	Input Leakage Current			±1	μA
C_I	Input Capacitance	(Note 2)		10	pF
C_{IO}	I/O Capacitance	(Note 2)		20	pF
OUTPUT VOLTAGE LEVELS					
V_{OH_1}	Logic High (CMOS)	I_{OH} = −10 μA (Note 2)	V_{CC} − 0.1		V
V_{OL_1}	Logic Low (CMOS)	I_{OH} = 10 μA (Note 2)		0.1	V
V_{OH_2}	Port A/B Drive, CK2 (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −7 mA	2.4		V
V_{OL_2}		I_{OL} = 3 mA		0.4	V
V_{OH_3}	Other Port Pin Drive, WO (open drain) (B_0–B_9, B_{13}, B_{14}, P_0–P_3)	I_{OH} = −1.6 mA	2.4		V
V_{OL_3}		I_{OL} = 0.5 mA		0.4	V
V_{OH_4}	ST1 and ST2 Drive	I_{OH} = −6 mA	2.4		V
V_{OL_4}		I_{OL} = 1.6 mA		0.4	V
V_{RAM}	RAM Keep-Alive Voltage	(Note 3)	2.5	V_{CC}	V
I_{OZ}	TRI-STATE Leakage Current			±5	μA

Note 1: I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0). I_{CC_1} is measured with $\overline{RESET}$ = V_{SS}. I_{CC_3} is measured with NMI = V_{CC}, CKI driven to V_{IH1} and V_{IL1}, with rise and fall times less than 10 ns.

Note 2: This is guaranteed by design and not tested.

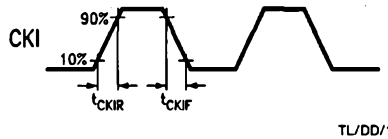
Note 3: Test duration is 100 ms.

20 MHz (1 Wait State Operation)
AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C

Symbol	Parameter	Min	Max	Units
f_C = CKI freq.	Operating Frequency (Note 4)	2	20.0	MHz
$t_{C1} = 1/f_C$	Clock Period	50	500	ns
t_{CKIR} (Note 3)	CKI Rise Time		7	ns
t_{CKIF} (Note 3)	CKI Fall Tiime		7	ns
$[t_{CKIH}/(t_{CKIH} + t_{CKIL})]100$	Duty Cycle	45	55	%
$t_C = 2/f_C$	Timing Cycle	100	1000	ns
$t_{LL} = ½\,t_C - 12$	ALE Pulse Width	38		ns
t_{DC1C2R} (Notes 1, 2)	Delay from CKI Falling Edge to CK2 Rising Edge	0	55	ns
t_{DC1C2F} (Notes 1, 2)	Delay from CKI Falling Edge to CK2 Falling Edge	0	55	ns
$t_{DC1ALER}$ (Notes 1, 2)	Delay from CKI Rising Edge to ALE Rising Edge	10	50	ns
$t_{DC1ALEF}$ (Notes 1, 2)	Delay from CKI Rising Edge to ALE Falling Edge	10	50	ns
$t_{DC2ALER} = ¼\,t_C + 35$ (Note 2)	Delay from CK2 Rising Edge to ALE Rising Edge		65	ns
$t_{DC2ALEF} = ¼\,t_C + 35$ (Note 2)	Delay from CK2 Falling Edge to ALE Falling Edge		65	ns
$t_{ST} = ¼\,t_C - 20$	Address Valid to ALE Falling Edge	5		ns
$t_{VP} = ¼\,t_C - 5$	Address Hold from ALE Falling Edge	20		ns
$t_{WAIT} = t_C = WS$	Wait State Period	100		ns
$f_{XIN} = f_C/19$	External Timer Input Frequency		1.05	MHz
t_{XIN}	Pulse Width for Timer Inputs	100		ns
f_{MW}	External MICROWIRE/PLUS Clock Input Frequency		1.25	MHz
$f_U = f_C/8$	External UART Clock Input Frequency		2.5	MHz

CKI Input Signal Characteristics

Rise/Fall Time



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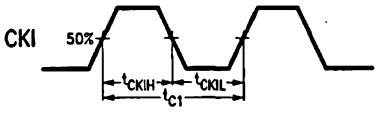
Duty Cycle



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Read Cycle Timing

Symbol	Parameter	Min	Max	Units
$t_{ARR} = 1/4\ t_C - 5$	ALE Falling Edge to $\overline{RD}$ Falling Edge	20		ns
$t_{RW} = 1/2\ t_C + WS - 10$	$\overline{RD}$ Pulse Width	140		ns
$t_{DR} = 3/4\ t_C - 20$	Data Hold after Rising Edge of $\overline{RD}$	0	55	ns
$t_{ACC} = t_C + WS - 85$ (Note 2)	Address Valid to Input Data Valid		115	ns
$t_{RD} = 1/2\ t_C + WS - 85$	$\overline{RD}$ Falling Edge to Input Data Valid		65	ns
$t_{RDA} = t_C - 5$	$\overline{RD}$ Rising Edge to Address Valid	95		ns

Note: Bus Output (Port A) C_L = 100 pF, CK2 Output C_L = 50 pF, other Outputs C_L = 80 pF. AC parameters are tested using DC Characteristics Inputs and non CMOS Outputs. Measurement of AC specifications is done with external clock driving CKI with 50% duty cycle. The capacitive load on CKO must be kept below 15 pF or AC measurements will be skewed.

Note: WS = t_{WAIT} * number of pre-programmed wait states. Minimum and Maximum values are calculated from maximum operating frequency with one (1) wait state pre-programmed.

Note 1: Do not design with this parameter unless CKI is driven with an active signal. When using a passive crystal circuit, CKI or CKO **should not** be connected to any external logic since any load (besides the passive components in the crystal circuit) will affect the stability of the crystal unpredictably.

Note 2: These are not directly tested parameters. Therefore the given min/max value cannot be guaranteed. It is, however, derived from measured parameters, and may be used for system design with a high confidence level.

Note 3: This is guaranteed by design and not tested.

Note 4: Maximum frequency with 0 wait states is 6 MHz.

Write Cycle Timing

Symbol	Parameter	Min	Max	Units
$t_{ARW} = 1/2\ t_C - 5$	ALE Falling Edge to $\overline{WR}$ Falling Edge	45		ns
$t_{WW} = 3/4\ t_C + WS - 20$	$\overline{WR}$ Pulse Width	155		ns
$t_{HW} = 1/4\ t_C - 5$	Data Hold after Rising Edge of $\overline{WR}$	20		ns
$t_V = 1/2\ t_C + WS - 20$	Data Valid before Rising Edge of $\overline{WR}$	130		ns

Ready/Hold Timing

Symbol	Parameter	Min	Max	Units
$t_{DAR} = 1/4\ t_C + WS - 80$	Falling Edge of ALE to Falling Edge of RDY		45	ns
$t_{RWP} = t_C + 10$	RDY Pulse Width	110		ns
$t_{SALE} = 1\ 1/4\ t_C + 70$	Falling Edge of $\overline{HLD}$ to Rising Edge of ALE	145		ns
$t_{HWP} = t_C + 10$	$\overline{HLD}$ Pulse Width	110		ns
$t_{HAD} = 1\ 1/4\ t_C + 70$	Rising Edge on $\overline{HLD}$ to Rising Edge on $\overline{HLDA}$		345	ns
$t_{HAE} = 2t_C + 130$	Falling Edge on $\overline{HLD}$ to Falling Edge on $\overline{HLDA}$		330*	ns
$t_{BF} = 1/2\ t_C + 66$	Bus Float after Falling Edge on $\overline{HLDA}$		116	ns
$t_{BE} = 1/2\ t_C + 66$	Bus Enable before Rising Edge of $\overline{HLDA}$	116		ns

***Note:** t_{HAE} may be as long as ($6t_C$ + 8ws + $144t_C$ + 180) depending on which instruction is being executed, the addressing mode and number of wait states. t_{HAE} maximum value tested is for the optimal case.

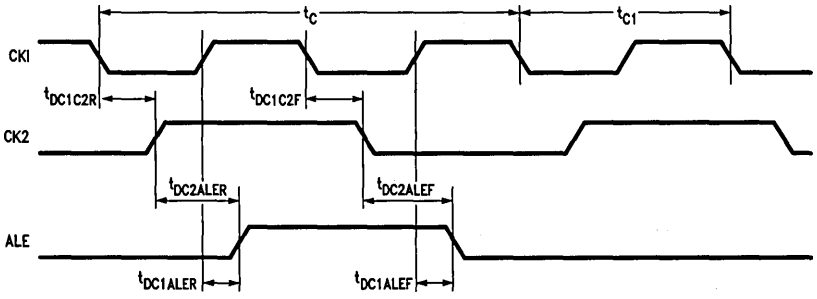
UPI Read/Write Timing

Symbol	Parameter	Min	Max	Units
t_{UAS}	Address Setup Time to Falling Edge of $\overline{URD}$	10		ns
t_{UAH}	Address Hold Time from Rising Edge of $\overline{URD}$	10		ns
t_{RPW}	$\overline{URD}$ Pulse Width	100		ns
t_{OE}	$\overline{URD}$ Falling Edge to Output Data Valid	0	60	ns
t_{OD}	Rising Edge of $\overline{URD}$ to Output Data Invalid	5	70	ns
t_{DRDY}	$\overline{RDRDY}$ Delay from Rising Edge of $\overline{URD}$		70	ns
t_{WDW}	$\overline{UWR}$ Pulse Width	40		ns
t_{UDS}	Input Data Valid before Rising Edge of $\overline{UWR}$	10		ns
t_{UDH}	Input Data Hold after Rising Edge of $\overline{UWR}$	20		ns
t_A	$\overline{WRRDY}$ Delay from Rising Edge of $\overline{UWR}$		70	ns

Note: Bus Output (Port A) C_L = 100 pF, CK2 Output C_L = 50 F, other Outputs C_L = 80 pF.

Timing Waveforms

CKI, CK2, ALE Timing Diagram



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Timing Waveforms (Continued)

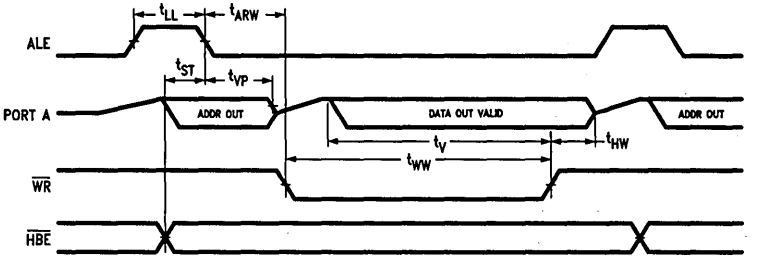

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FIGURE 1. Write Cycle

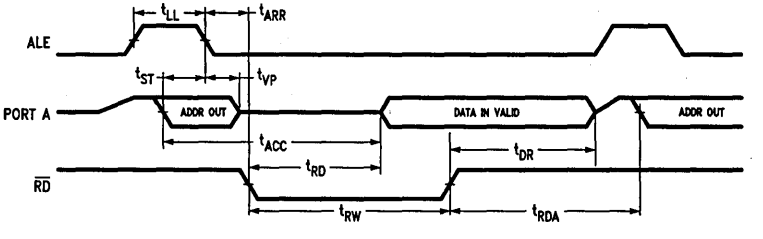

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FIGURE 2. Read Cycle

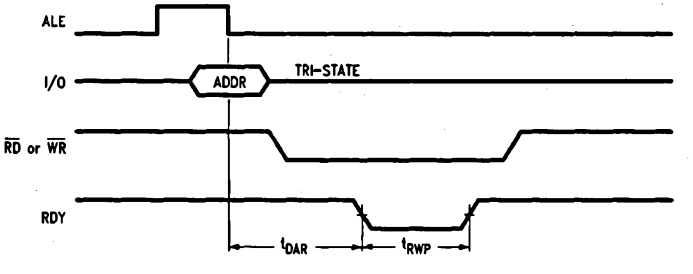

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FIGURE 3. Ready Mode Timing

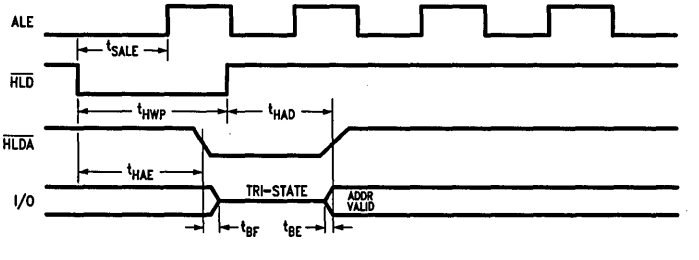

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FIGURE 4. Hold Mode Timing

Timing Waveforms (Continued)

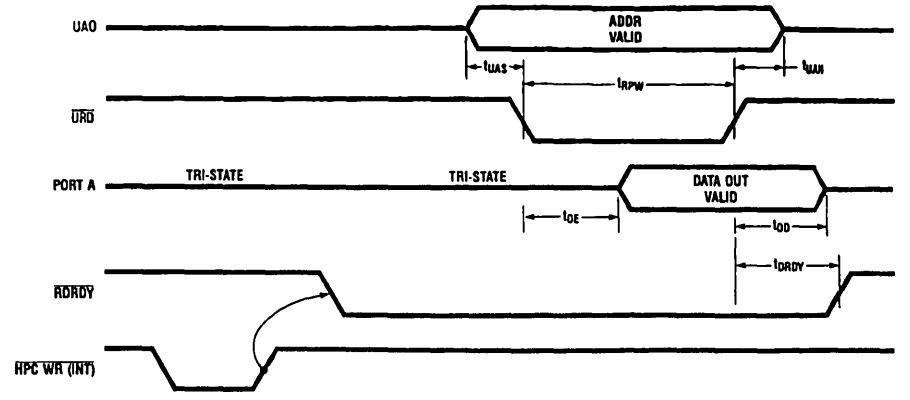

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FIGURE 5. UPI Read Timing

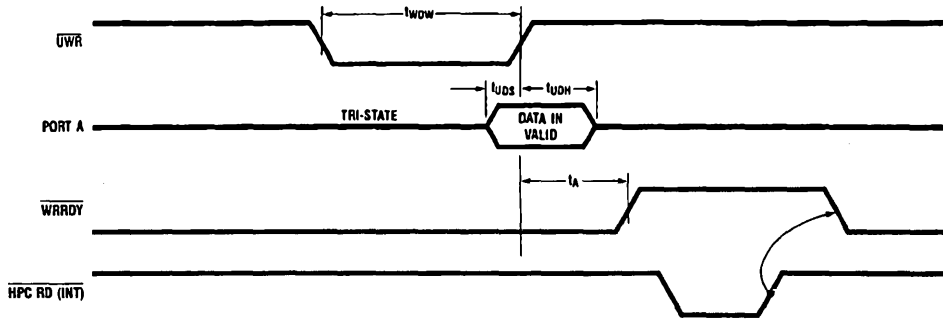

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FIGURE 6. UPI Write Timing

Pin Descriptions

The HPC46083MH is available in 68-pin LDCC packages.

I/O PORTS

Port A is a 16-bit bidirectional I/O port with a data direction register to enable each separate pin to be individually defined as an input or output. When accessing external memory, port A is used as the multiplexed address/data bus.

Port B is a 16-bit port with 12 bits of bidirectional I/O similar in structure to Port A. Pins B10, B11, B12 and B15 are general purpose outputs only in this mode. Port B may also be configured via a 16-bit function register BFUN to individually allow each pin to have an alternate function.

B0:	TDX	UART Data Output
B1:		
B2:	CKX	UART Clock (Input or Output)
B3:	T2IO	Timer2 I/O Pin
B4:	T3IO	Timer3 I/O Pin
B5:	SO	MICROWIRE/PLUS Output
B6:	SK	MICROWIRE/PLUS Clock (Input or Output)
B7:	$\overline{HLDA}$	Hold Acknowledge Output
B8:	TS0	Timer Synchronous Output
B9:	TS1	Timer Synchronous Output
B10:	UA0	Address 0 Input for UPI Mode
B11:	$\overline{WRRDY}$	Write Ready Output for UPI Mode
B12:		
B13:	TS2	Timer Synchronous Output
B14:	TS3	Timer Synchronous Output
B15:	$\overline{RDRDY}$	Read Ready Output for UPI Mode

When accessing external memory, four bits of port B are used as follows:

B10:	ALE	Address Latch Enable Output
B11:	$\overline{WR}$	Write Output
B12:	$\overline{HBE}$	High Byte Enable Output/Input (sampled at reset)
B15:	$\overline{RD}$	Read Output

Port I is an 8-bit input port that can be read as general purpose inputs and is also used for the following functions:

I0:		
I1:	NMI	Nonmaskable Interrupt Input
I2:	INT2	Maskable Interrupt/Input Capture/$\overline{URD}$
I3:	INT3	Maskable Interrupt/Input Capture/$\overline{UWR}$
I4:	INT4	Maskable Interrupt/Input Capture
I5:	SI	MICROWIRE/PLUS Data Input
I6:	RDX	UART Data Input
I7:		

Port D is an 8-bit input port that can be used as general purpose digital inputs.

Port P is a 4-bit output port that can be used as general purpose data, or selected to be controlled by timers 4

Pin Descriptions (Continued)

through 7 in order to generate frequency, duty cycle and pulse width modulated outputs.

POWER SUPPLY PINS

V_{PP} Programming Power

V_{CC1} Positive Power Supply

GND Ground for On-Chip Logic

DGND Ground for Output Buffers

Note: GND and DGND are electrically connected in the package. Both V_{CC} pins and both ground pins must be used.

CLOCK PINS

CKI The Chip System Clock Input

CKO The Chip System Clock Output (inversion of CKI)

Pins CKI and CKO are usually connected across an external crystal.

CK2 Clock Output (CKI divided by 2)

OTHER PINS

$\overline{WO}$ This is an active low open drain output that signals an illegal situation has been detected by the Watch Dog logic.

ST1 Bus Cycle Status Output: indicates first opcode fetch.

ST2 Bus Cycle Status Output: indicates machine states (skip, interrupt and first instruction cycle).

$\overline{RESET}$ is an active low input that forces the chip to restart and sets the ports in a TRI-STATE® mode.

RDY/$\overline{HLD}$ has two uses, selected by a software bit. It's either a READY input to extend the bus cycle for slower memories, or a HOLD request input to put the bus in a high impedance state for DMA purposes.

EXM External memory enable (active high) disables internal EPROM and maps it to external memory.

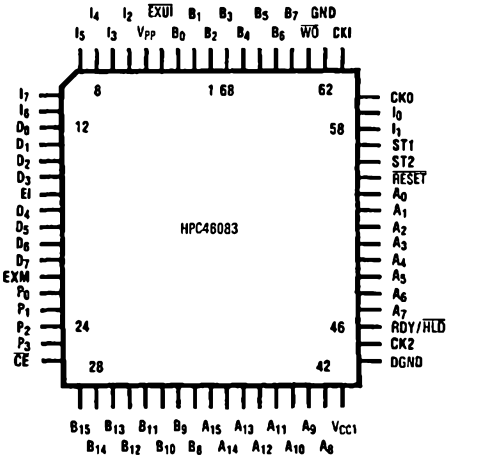
EI External interrupt with vector address FFF1:FFF0. (Rising/falling edge or high/low level sensitive). Alternately can be configured as 4th input capture.

$\overline{EXUI}$ External interrupt which is internally OR'ed with the UART interrupt with vector address FFF3:FFF2 (Active Low).

$\overline{CE}$ Places part in EPROM Programming mode (Active Low).

Connection Diagrams

Leaded Chip Carriers



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Top View

The HPC46083MH is a two chip system packaged in a dual cavity ceramic LDCC package, with a UV quartz window on bottom. Within the package is an HPC46083 and a UV-erasable EPROM with port recreation logic. Code executes out of the EPROM. The HPC46083MH may be programmed using a programming card to adapt the part to a 27C64 EPROM programmer. The part functions as the normal HPC, and the use of the EPROM should be transparent to the user. The only system design consideration is that pin 5 is V_{PP}, not V_{CC}, and should be tied to V_{CC} during normal operation. Pin 26 should also be tied to V_{CC}. DGND is connected internally to V_{SS} via a ground plane internal to the package. This should not cause any functional problems to a normal user of the part. Please be careful when inserting the part that the polarity dot is on pin 1.

When programming the part, care should be taken to use only the NSC HPC-EMU-PRGM 980420174 Programming card. This is easily distinguished by the large Yamaichi socket on the top. When programming it in the NSC MOLE Brain Board programmer be sure to use the Chip 2764 option in the programming menu. Use 13.5V ±0.5V for V_{PP}. The part will program in most 27C64 EPROM programmers, however refer to the data sheet to ensure that all timing requirements are met in the programming algorithm. Normal erase times under a UV light run about 45 mins., but may vary depending on the intensity of the light.

Suggested sockets and extractor tool:

Socket #	AMP	PLCC #821574-1 #6141749
	YAMAICHI	IC51-0684-390 IC120-0684-204
	ENPLAS	PLCC-68-1.27-02
Extractor Tool #	AMP	821566-1

Programming Information

DC Electrical Characteristics $T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Supply Current during Programming Pulse $\overline{RESET} = \overline{CE} = V_{IL}$		60	mA
I_{CC}	V_{PP} Supply Current		35	mA

Note 1: V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.

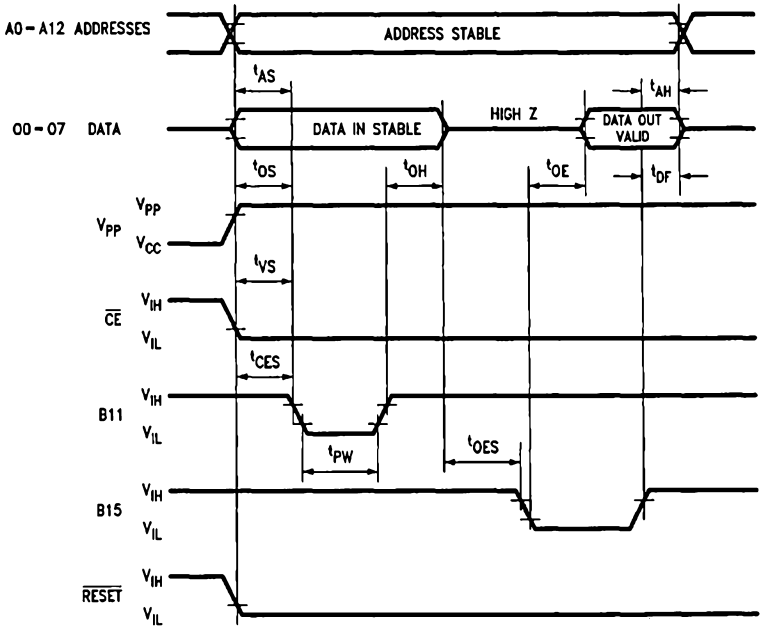
Note 2: V_{PP} must not be greater than 14V including overshoot. During $\overline{CE}$ = B11 = V_{IL}, V_{PP} must not be switched from 5V to 13.5V or vice-versa.

Note 3: During power up the B11 pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC Electrical Characteristics $T_A = 25 \pm 5°C$, $V_{CC} = 5.50V \pm 5\%$, $V_{PP} = 13.5 \pm 0.5V$

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Setup Time	2			μs
t_{CES}	$\overline{CE}$ Enable Setup Time	2			μs
t_{OES}	B_{11} Enable Setup Time	2			μs
t_{OS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{OH}	Data Hold Time	2			μs
t_{DF}	Chip Disable to Output Float Delay	0		130	ns
t_{OE}	Data Valid from B_{11} Enable			130	ns
t_{VS}	V_{PP} Setup Time	2			μs
t_{PW}	B_{15} Pulse Width	1	5	10	ms

Programming Waveform



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Programming Information (Continued)

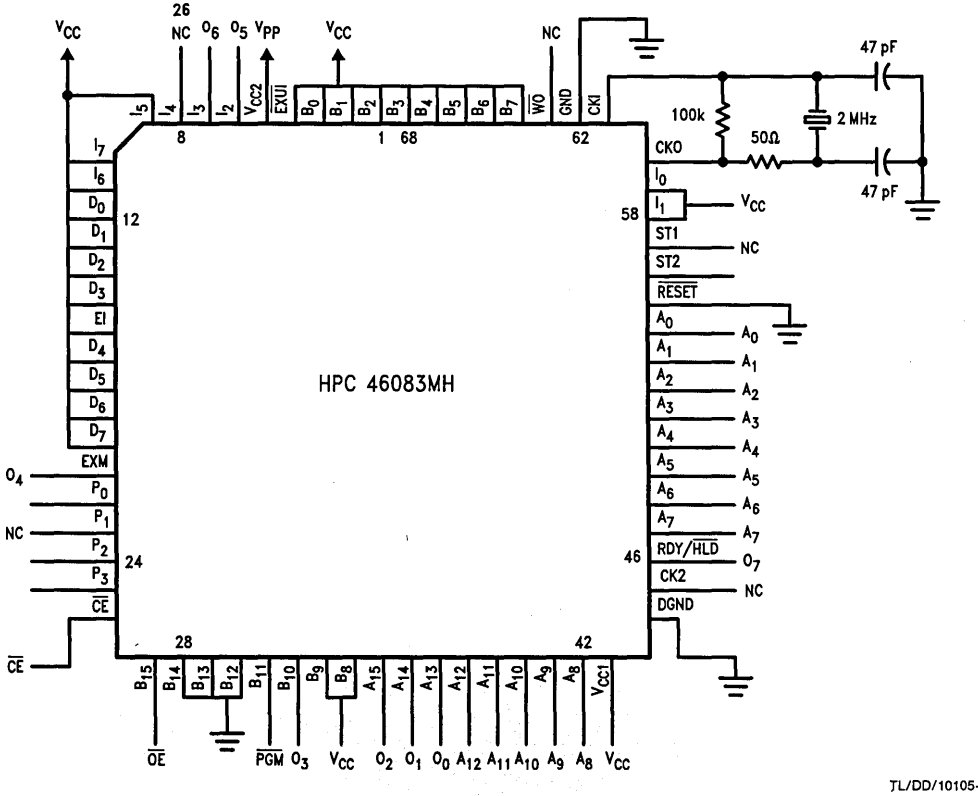
The following is the pin-connection list for programming the HPC Emulator.

HPC EMU		27C64	
Pin	Name	Pin	Name
1–4	B0–B2, EXUI	28	V_{CC}
5	V_{PP}	1	V_{PP}
6	I2	17	O5
7	I3	18	O6
8	I4	26	NC
9–20	I5–I7, D0–D7, EI	28	V_{CC}
21	EXM	16	O4
22–25	P0–P3	NC	
26	$\overline{CE}$	20	$\overline{CE}$
27	B15	22	$\overline{OE}$
28–30	B12–B14	14	GND
31	B11	27	$\overline{PGM}$
32	B10	15	O3
33,34	B9,B8	28	V_{CC}
35	A15	13	O2
36	A14	12	O1
37	A13	11	O0

HPC EMU		27C64	
Pin	Name	Pin	Name
38	A12	2	A12
39	A11	23	A11
40	A10	21	A10
41	A9	24	A9
42	A8	25	A8
43	V_{CC}	28	V_{CC}
44	DGND	14	GND
45	CK2	NC	
46	RDY/HLD	19	O7
47–54	A7–A0	3–10	A7–A0
55	RESET	14	GND
56,57	ST1,ST2	NC	
58,59	I0,I1	28	V_{CC}
60,61	CKO,CKI	Clock Circuit	NC
62	GND	14	GND
63	WO		NC
64–68	B3–B7	28	V_{CC}

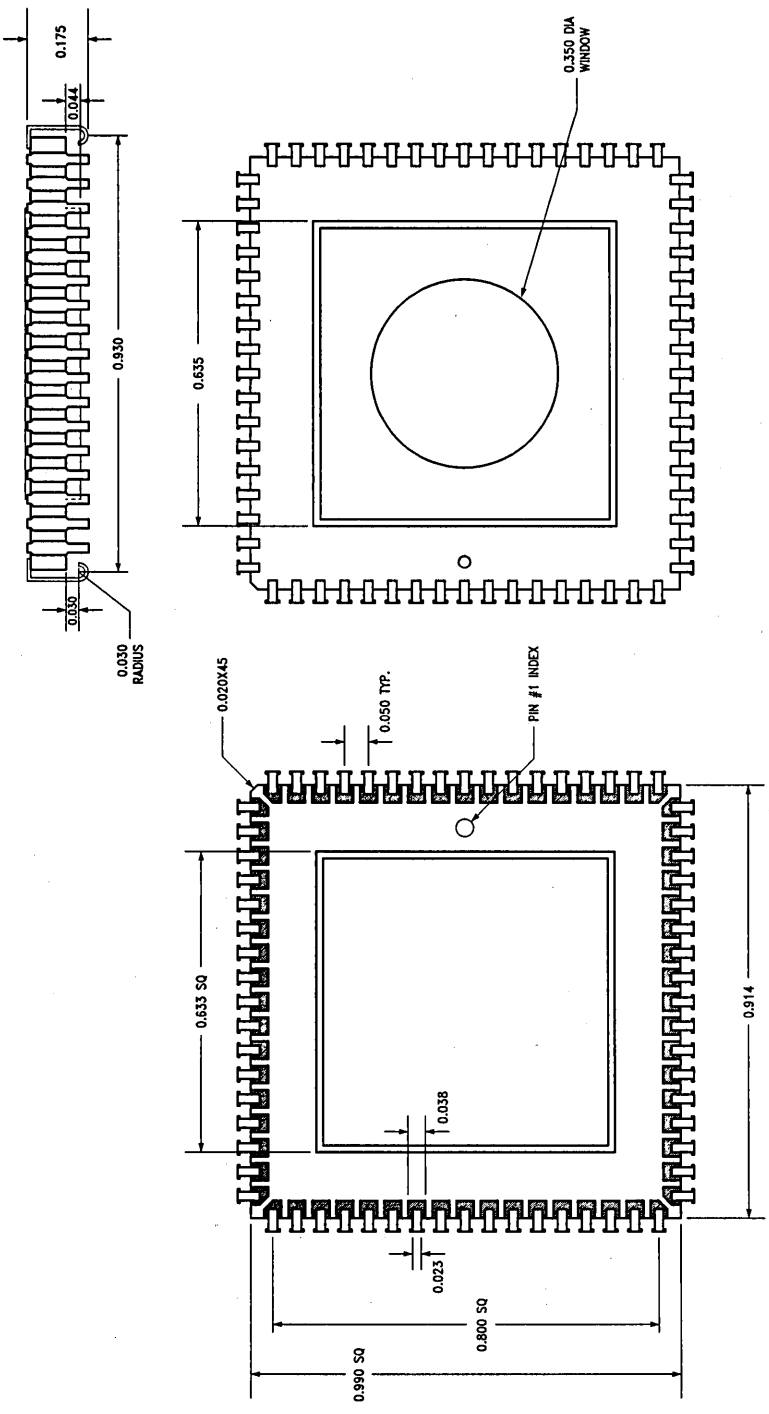
Attach a crystal circuit to CKI & CKO.

Programming Hookup to Program as 27C64



TL/DD/10105–13

Programming Information (Continued)



TL/DD/10105–14