Data Sheet | August 1999 | File Number 4355.1

Rad-Hard 16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

The HS-1840ARH is a radiation hardened, monolithic 16 channel multiplexer constructed with the Intersil Rad-Hard Silicon Gate, bonded wafer, Dielectric Isolation process. It is designed to provide a high input impedance to the analog source if device power fails (open), or the analog signal voltage inadvertently exceeds the supply by up to ±35V, regardless of whether the device is powered on or off. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. More significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All inputs have electrostatic discharge protection.

The HS-1840ARH is processed and screened in full compliance with MIL-PRF-38535 and QML standards. The device is available in a 28 lead SBDIP and a 28 lead Ceramic Flatpack.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95630. A "hot-link" is provided on our homepage for downloading.
http://www.intersil.com/spacedefense/space.htm

Features

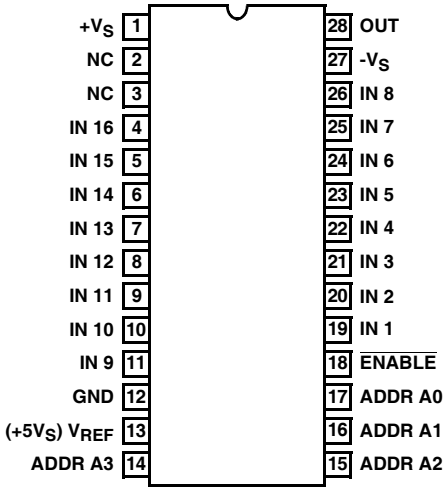
- Electrically Screened to SMD # 5962-95630
- QML Qualified per MIL-PRF-38535 Requirements
- Pin-to-Pin for Intersil's HS-1840RH and HS-1840/883S
- Improved Radiation Performance
  - Gamma Dose (γ) 3 x 10^5RAD(Si)
- Improved $r_{DS(ON)}$ Linearity
- Improved Access Time 1.5µs (Max) Over Temp and Post Rad
- High Analog Input Impedance 500MΩ During Power Loss (Open)
- ±35V Input Over Voltage Protection (Power On or Off)
- Dielectrically Isolated Device Islands
- Excellent in Hi-Rel Redundant Systems
- Break-Before-Make Switching
- No Latch-Up

Ordering Information

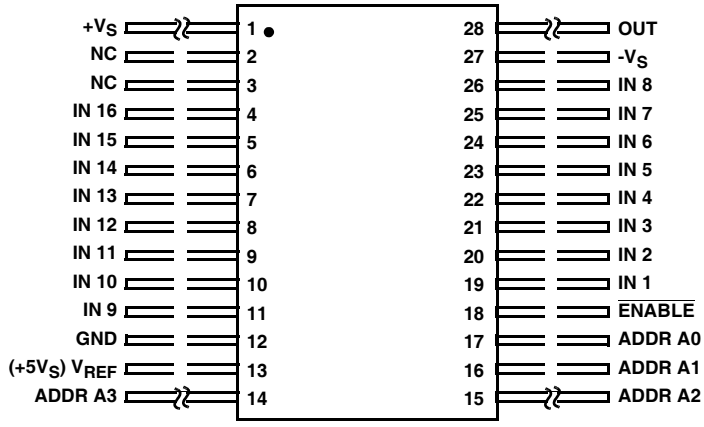
ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^oC)
5962F9563002QXC	HS1-1840ARH-8	-55 to 125
5962F9563002QYC	HS9-1840ARH-8	-55 to 125
5962F9563002V9A	HS0-1840ARH-Q	25
5962F9563002VXC	HS1-1840ARH-Q	-55 to 125
5962F9563002VYC	HS9-1840ARH-Q	-55 to 125
HS1-1840ARH/PROTO	HS1-1840ARH/PROTO	-55 to 125
HS9-1840ARH/PROTO	HS9-1840ARH/PROTO	-55 to 125

Pinouts

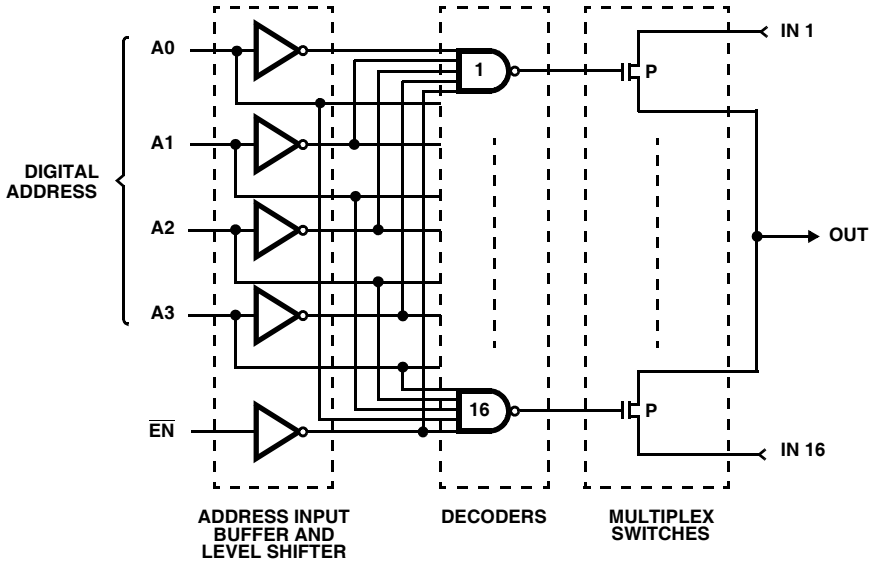
HS1-1840ARH (SBDIP) CDIP2-T28
TOP VIEW



HS9-1840ARH (FLATPACK) CDFP3-F28
TOP VIEW



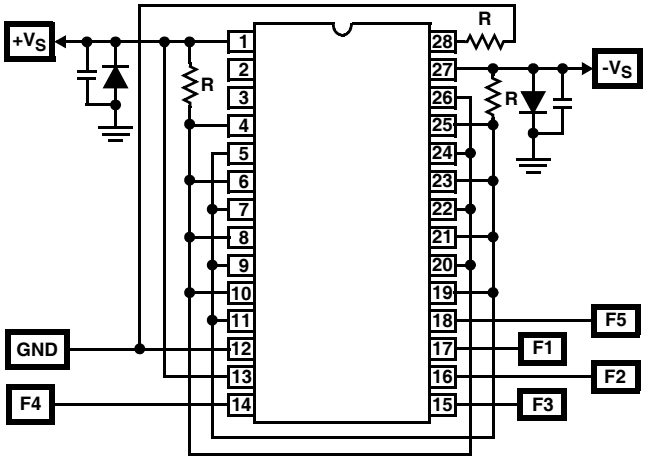
Functional Diagram



TRUTH TABLE

A3	A2	A1	A0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	None
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

Burn-In/Life Test Circuits



NOTES:

V_S+ = +15.5V ±0.5V, V_S- = -15.5V ±0.5V.

R = 1kΩ ±5%.

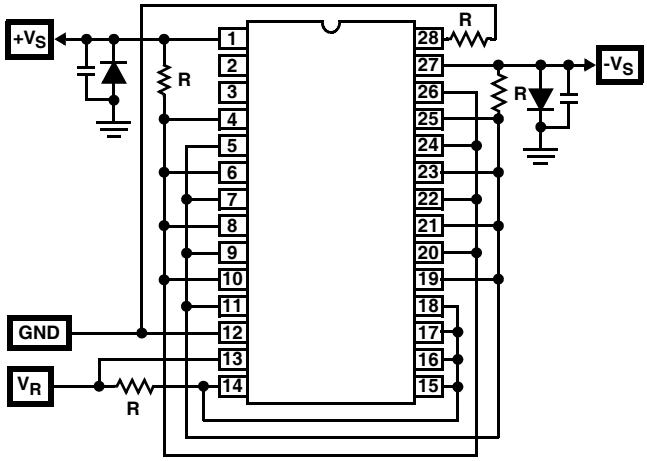
$C_1 = C_2$ = 0.01μF ±10%, 1 each per socket, minimum.

$D_1 = D_2$ = 1N4002, 1 each per board, minimum.

Input Signals: square wave, 50% duty cycle, 0V to 15V peak ±10%.

F1 = 100kHz; F2 = F1/2; F3 = F1/4; F4 = F1/8; F5 = F1/16.

FIGURE 1. DYNAMIC BURN-IN AND LIFE TEST CIRCUIT



NOTES:

R = 1kΩ ±5%, $^1/_4$W.

$C_1 = C_2$ = 0.01μF minimum, 1 each per socket, minimum.

V_S+ = 15.5V ±0.5V, V_S- = -15.5V ±0.5V, V_R = 15.5 ±0.5V.

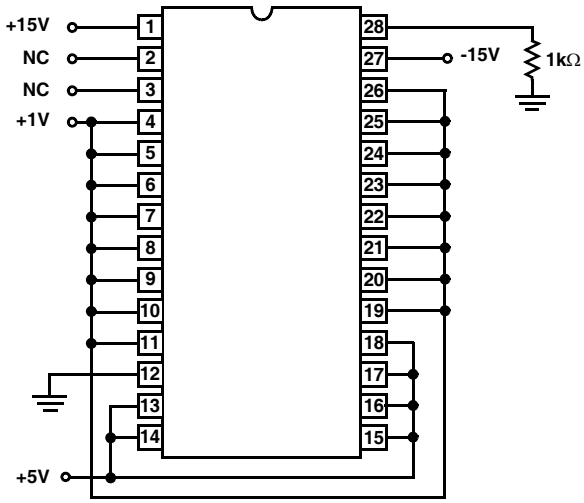
FIGURE 2. STATIC BURN-IN TEST CIRCUIT

NOTES:

1. The above test circuits are utilized for all package types.
2. The Dynamic Test Circuit is utilized for all life testing.

Irradiation Circuit

HS-1840ARH



NOTE:

3. All irradiation testing is performed in the 28 lead CERDIP package.

Die Characteristics

DIE DIMENSIONS:

(2820µm x 4080µm x 483µm ±25.4µm)
111 mils x 161 mils x 19 mils ±1 mil

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorus Silicon Glass)
Thickness: 8.0kÅ ±1kÅ

Top Metallization:

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

Modified SEM

Transistor Count:

407

Process:

Radiation Hardened Silicon Gate,
Bonded Wafer, Dielectric Isolation

Metallization Mask Layout

HS-1840ARH