Accelerating graphics at ultra-low power

i.MX 7ULP Applications Processors

The i.MX 7ULP family is a highly integrated multi-market applications processor designed to enable ultra-low-power and secure, portable applications.

TARGET APPLICATIONS

▸ Smart home controls

▸ Wearables

▸ IoT edge solutions

▸ Portable patient monitoring

▸ Building automation

▸ Portable scanners and printers

The i.MX 7ULP family is built upon the heterogeneous asymmetric architecture utilizing both the ARM® Cortex®-A7 and Cortex-M4 cores, with separate isolated domains. The heterogeneous architecture provides the ultimate flexibility for customers by enabling a single-chip solution that can run sophisticated operating systems and provide real-time responsiveness. The i.MX 7ULP processor is supported by NXP®'s companion power management ICs (PMICs).

FEATURES

▸ **Arm Cortex-A7**—The Arm core enhances the capabilities of portable, connected applications by fulfilling the ever-increasing power efficient MIPS needs of operating systems and applications.

▸ **Dual-core, heterogeneous processing architecture**—The Cortex-A7 and Cortex-M4 cores enable the device to run a rich operating system like Linux® on the Cortex-A7 core and an RTOS like FreeRTOS on the Cortex-M4 core. In addition, the Cortex-M4 core becomes the system master, allowing for control of the boot process as well as power modes.

▸ **Multilevel memory system**—The multilevel memory system of the Cortex-A7 processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including LPDDR2 and LPDDR3, QSPI, and managed NAND, including eMMC rev. 5.0.

▸ **Power efficiency**—Power management implemented throughout the IC enables multimedia features and peripherals to consume minimum power in both active and various low-power modes.

▸ **Advanced security**—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption secure boot, and tamper detection.

- **Multimedia**—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (media processor engine) coprocessor and a programmable smart DMA (SDMA) controller. Each processor provides an integrated graphics processing unit that supports an OpenGL ES 2.0 and OpenVG 1.1 3D and a 2D graphics accelerator.

- **Display interface**—Each processor provides a 2-lane MIPI DSI interface.

- **Interface flexibility**—Each processor supports connections to a variety of interfaces: high-speed USB on-the-go with PHY, high-speed inter-chip USB, multiple expansion card ports (high-speed MMC/SDIO host and other), two single-ended-input 12-bit ADC/DACs, I²S audio interface, and a variety of other popular interfaces (such as UART, I²C).

SOFTWARE AND TOOLS

The i.MX 7ULP processor is supported by an evaluation kit (EVK) and comes with an SD card pre-installed with the Linux operating system. Also offered are the Android™ OS, as well as FreeRTOS for the Cortex-M4 core.

i.MX 7ULP APPLICATIONS PROCESSOR BLOCK DIAGRAM
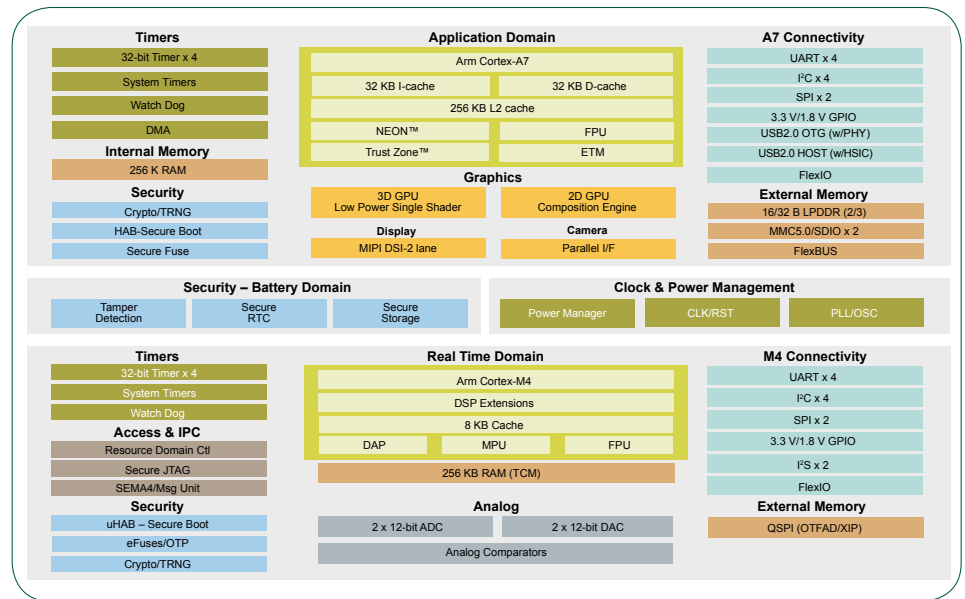
i.MX 7ULP ECOSYSTEM

Leveraging the broad Arm community, the i.MX 7ULP builds technology alliances to enable better customer solutions and faster time-to-market. Partner solutions include:

- Tool chains
- Software
- Codecs
- Middleware/applications
- Embedded board solutions
- Design services
- System integrators
- Training

Join fellow i.MX developers online at **www.imxcommunity.org**

i.MX 7ULP DEVICE HIGHLIGHTS

i.MX 7ULP

- Single Arm Cortex-A7 core
- Cortex-M4 core
- 256 KB L2 cache
- Total of 512 KB of on-chip RAM
- 16-/32-bit LPDDR2/3
- Full security w/ tamper resist
- Separate system power domains with IPC

Consumer Industrial

Product Longevity Energy Efficient Solutions™