EMBEDDED Intel486™ SX PROCESSOR

- **32-Bit RISC Technology Core**
- **8-Kbyte Write-Through Cache**
- **Four Internal Write Buffers**
- **Burst Bus Cycles**
- **Dynamic Bus Sizing for 8- and 16-bit Data Bus Devices**
- **SL Technology**
- **Data Bus Parity Generation and Checking**
- **Boundary Scan (JTAG)**
- **3.3-Volt Processor**
  - **— 208-Lead Shrink Quad Flat Pack (SQFP)**
- **5-Volt Processor**
  - **— 196-Lead Plastic Quad Flat Pack (PQFP)**
- **Binary Compatible with Large Software Base**

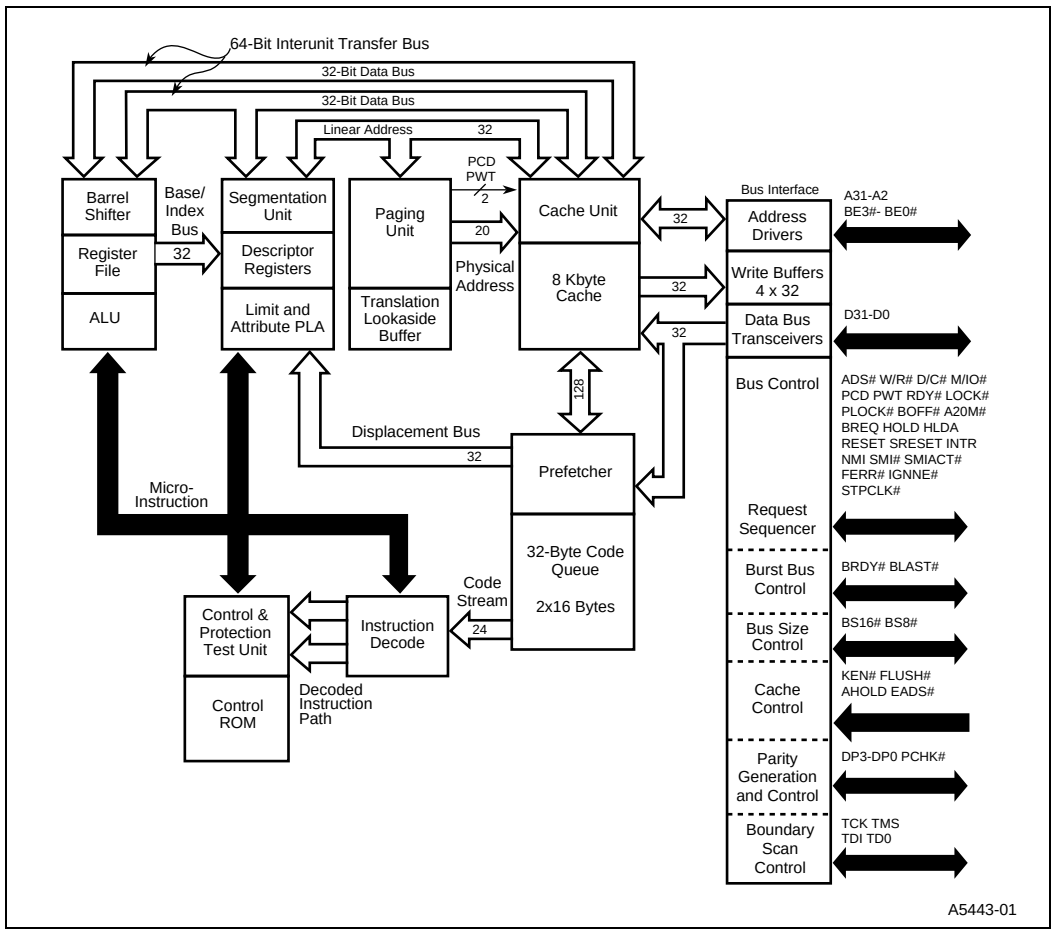


Figure 1. Embedded Intel486™ SX Processor Block Diagram

December 1997 **Order Number:** 272769-002

EMBEDDED Intel486™ SX PROCESSOR

FIGURES

TABLES

1.0 INTRODUCTION

The embedded Intel486™ SX processor provides high performance to 32-bit, embedded applications. Designed for applications that do not need a floating-point unit, the processor is ideal for embedded designs running DOS*, Microsoft Windows*, OS/2*, or UNIX* applications written for the Intel architecture. Projects can be completed quickly by utilizing the wide range of software tools, utilities, assemblers and compilers that are available for desktop computer systems. Also, developers can find advantages in using existing chip sets and peripheral components in their embedded designs.

The embedded Intel486 SX processor is binary compatible with the Intel386™ and earlier Intel processors. Compared with the Intel386 processor, it provides faster execution of many commonly-used instructions. It also provides the benefits of an integrated, 8-Kbyte, write-through cache for code and data. Its data bus can operate in burst mode which provides up to 106-Mbyte-per-second transfers for cache-line fills and instruction prefetches.

Intel's SL technology is incorporated in the embedded Intel486 SX processor. Utilizing Intel's System Management Mode (SMM), it enables designers to develop energy-efficient systems.

Two component packages are available. A 196-lead Plastic Quad Flat Pack (PQFP) is available for 5-Volt designs and a 208-lead Shrink Quad Flat Pack (SQFP) is available for 3.3-Volt designs. Both products operate at CLK frequencies up to 33 MHz.

1.1 Features

The embedded Intel486 SX processor offers these features:

- **32-bit RISC-Technology Core** — The embedded Intel486 SX processor performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general purpose registers.
- **Single Cycle Execution** — Many instructions execute in a single clock cycle.
- **Instruction Pipelining** — Overlapped instruction fetching, decoding, address translation and execution.
- **On-Chip Cache with Cache Consistency Support** — An 8-Kbyte, write-through, internal cache is used for both data and instructions. Cache hits provide zero wait-state access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain cache consistency.
- **External Cache Control** — Write-back and flush controls for an external cache are provided so the processor can maintain cache consistency.
- **On-Chip Memory Management Unit** — Address management and memory space protection mechanisms maintain the integrity of memory in a multitudinous and virtual memory environment. Both memory segmentation and paging are supported.
- **Burst Cycles** — Burst transfers allow a new double-word to be read from memory on each bus clock cycle. This capability is especially useful for instruction prefetch and for filling the internal cache.
- **Write Buffers** — The processor contains four write buffers to enhance the performance of consecutive writes to memory. The processor can continue internal operations after a write to these buffers, without waiting for the write to be completed on the external bus.
- **Bus Backoff** — When another bus master needs control of the bus during a processor initiated bus cycle, the embedded Intel486 SX processor floats its bus signals, then restarts the cycle when the bus becomes available again.
- **Instruction Restart** — Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- **Dynamic Bus Sizing** — External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16, or 32 bits can be used.
- **Boundary Scan (JTAG)** — Boundary Scan provides in-circuit testing of components on printed circuit boards. The Intel Boundary Scan implementation conforms with the IEEE Standard Test Access Port and Boundary Scan Architecture.

Intel's SL technology provides these features:

* Other brands and names are the property of their respective owners.

- **Intel System Management Mode (SMM)** — A unique Intel architecture operating mode provides a dedicated special purpose interrupt and address space that can be used to implement intelligent power management and other enhanced functions in a manner that is completely transparent to the operating system and applications software.
- **I/O Restart** — An I/O instruction interrupted by a System Management Interrupt (SMI#) can automatically be restarted following the execution of the RSM instruction.
- **Stop Clock** — The embedded Intel486 SX processor has a stop clock control mechanism that provides two low-power states: a Stop Grant state (20–40 mA typical, depending on input clock frequency) and a Stop Clock state (~100-200 μA typical, with input clock frequency of 0 MHz).
- **Auto HALT Power Down —** After the execution of a HALT instruction, the embedded Intel486 SX processor issues a normal Halt bus cycle and the clock input to the processor core is automatically stopped, causing the processor to enter the Auto HALT Power Down state (20–40 mA typical, depending on input clock frequency).

1.2 Family Members

Table 1 shows the embedded Intel486 SX processors and briefly describes their characteristics.

Table 1. The Embedded Intel486™ SX Processor Family

Product	Supply Voltage V_{CC}	Maximum Processor Frequency	Package
SB80486SXSC33	3.3 V	33 MHz	208-Lead SQFP
KU80486SXSA33	5.0 V	33 MHz	196-Lead PQFP

2.0 HOW TO USE THIS DOCUMENT

For a complete set of documentation related to the embedded Intel486 SX processor, use this document in conjunction with the following reference documents:

- *Embedded Intel486™ Processor Family Developer's Manual* — Order No. 273021
- *Embedded Intel486™ Processor Hardware Reference Manual* — Order No. 273025
- *Intel486™ Microprocessor Family Programmer's Reference Manual* — Order No. 240486
- Intel Application Note AP-485 — *Intel Processor Identification with the CPUID Instruction* — Order No. 241618

The information in the reference documents for the Intel486 SX processor, 1X Clock (CLK), applies to the embedded Intel486 SX processor. Some of the Intel486 SX processor information is duplicated in this document to minimize the dependence on the reference documents.

3.0 PIN DESCRIPTIONS

3.1 Pin Assignments

The following figures and tables show the pin assignments of each package type for the embedded Intel486 SX processor. Tables are provided showing the pin differences between the embedded Intel486 SX processor and other embedded Intel486 processor products.

208-Lead SQFP - Quad Flat Pack

196-Lead PQFP - Plastic Quad Flat Pack

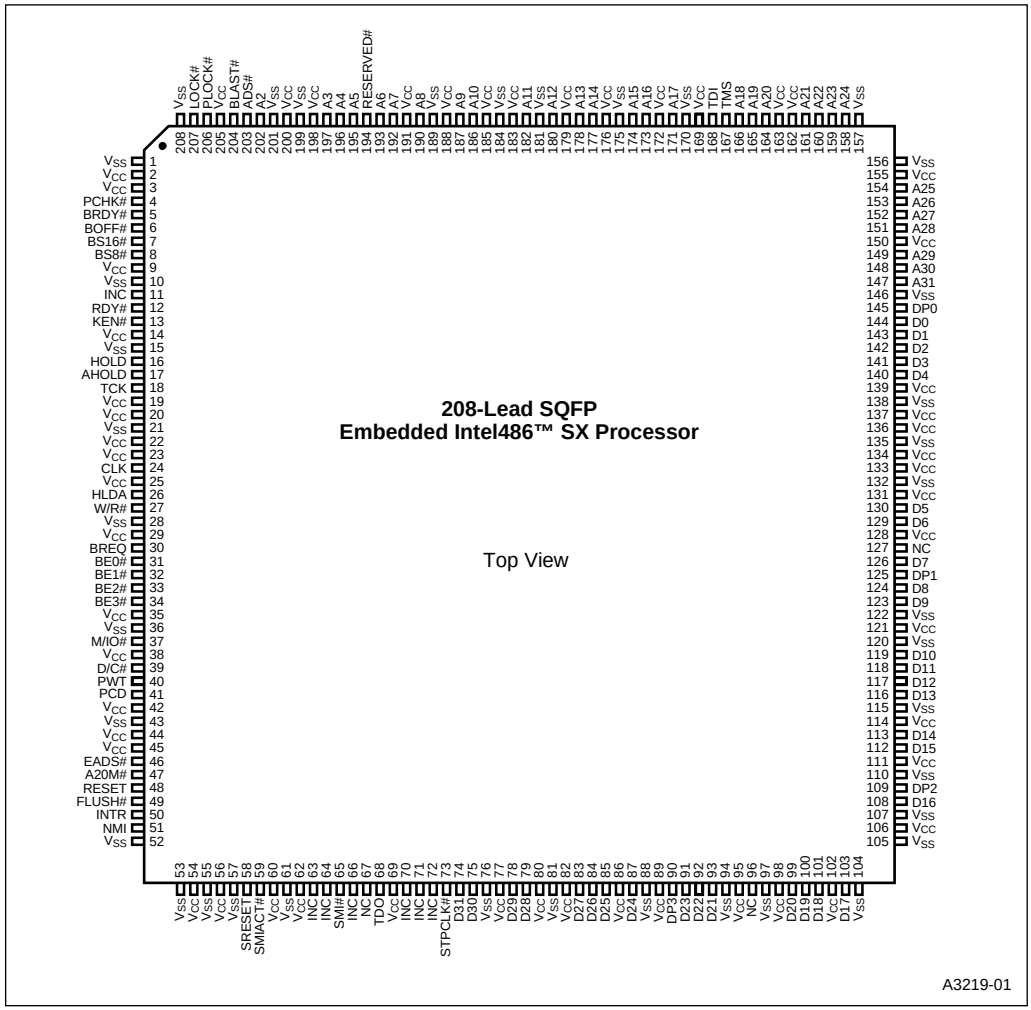


Figure 2. Package Diagram for 208-Lead SQFP Embedded Intel486™ SX Processor

Table 2. Pinout Differences for 208-Lead SQFP Package

Pin #	Embedded Intel486™ SX Processor	Embedded IntelDX2™ Processor	Embedded Write-Back Enhanced IntelDX4™ Processor
3	V_{CC}[1]	V_{CC}	V_{CC5}
11	INC[2]	INC	CLKMUL
63	INC	INC	HITM#
64	INC	INC	WB/WT#
66	INC	FERR#	FERR#
70	INC	INC	CACHE#
71	INC	INC	INV
72	INC	IGNNE#	IGNNE#

NOTES:

1. This pin location is for the V_{CC5} pin on the embedded IntelDX4 processor. For compatibility with 3.3V processors that have 5V-tolerant input buffers (i.e., embedded IntelDX4 processors), this pin should be connected to a V_{CC} trace, not to the V_{CC} plane.
2. INC. Internal No Connect. These pins are not connected to any internal pad in the embedded Intel486 SX processor. However, new signals are defined for the location of the INC pins in the embedded IntelDX2 and IntelDX4 processors. One system design can accommodate any one of these processors provided the purpose of each INC pin is understood before it is used.

Table 3. Pin Assignment for 208-Lead SQFP Package (Sheet 1 of 2)

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	V_{SS}	53	V_{SS}	105	V_{SS}	157	V_{SS}
2	V_{CC}	54	V_{CC}	106	V_{CC}	158	A24
3	V_{CC}[1]	55	V_{SS}	107	V_{SS}	159	A23
4	PCHK#	56	V_{CC}	108	D16	160	A22
5	BRDY#	57	V_{SS}	109	DP2	161	A21
6	BOFF#	58	SRESET	110	V_{SS}	162	V_{CC}
7	BS16#	59	SMIACT#	111	V_{CC}	163	V_{CC}
8	BS8#	60	V_{CC}	112	D15	164	A20
9	V_{CC}	61	V_{SS}	113	D14	165	A19
10	V_{SS}	62	V_{CC}	114	V_{CC}	166	A18
11	INC[2]	63	INC[2]	115	V_{SS}	167	TMS
12	RDY#	64	INC[2]	116	D13	168	TDI
13	KEN#	65	SMI#	117	D12	169	V_{CC}
14	V_{CC}	66	INC[2]	118	D11	170	V_{SS}
15	V_{SS}	67	NC[3]	119	D10	171	A17
16	HOLD	68	TDO	120	V_{SS}	172	V_{CC}
17	AHOLD	69	V_{CC}	121	V_{CC}	173	A16
18	TCK	70	INC[2]	122	V_{SS}	174	A15
19	V_{CC}	71	INC[2]	123	D9	175	V_{SS}
20	V_{CC}	72	INC[2]	124	D8	176	V_{CC}
21	V_{SS}	73	STPCLK#	125	DP1	177	A14
22	V_{CC}	74	D31	126	D7	178	A13
23	V_{CC}	75	D30	127	NC[3]	179	V_{CC}
24	CLK	76	V_{SS}	128	V_{CC}	180	A12
25	V_{CC}	77	V_{CC}	129	D6	181	V_{SS}
26	HLDA	78	D29	130	D5	182	A11
27	W/R#	79	D28	131	V_{CC}	183	V_{CC}
28	V_{SS}	80	V_{CC}	132	V_{SS}	184	V_{SS}
29	V_{CC}	81	V_{SS}	133	V_{CC}	185	V_{CC}
30	BREQ	82	V_{CC}	134	V_{CC}	186	A10
31	BE0#	83	D27	135	V_{SS}	187	A9
32	BE1#	84	D26	136	V_{CC}	188	V_{CC}
33	BE2#	85	D25	137	V_{CC}	189	V_{SS}

Table 3. Pin Assignment for 208-Lead SQFP Package (Sheet 2 of 2)

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
34	BE3#	86	V_{CC}	138	V_{SS}	190	A8
35	V_{CC}	87	D24	139	V_{CC}	191	V_{CC}
36	V_{SS}	88	V_{SS}	140	D4	192	A7
37	M/IO#	89	V_{CC}	141	D3	193	A6
38	V_{CC}	90	DP3	142	D2	194	RESERVED#
39	D/C#	91	D23	143	D1	195	A5
40	PWT	92	D22	144	D0	196	A4
41	PCD	93	D21	145	DP0	197	A3
42	V_{CC}	94	V_{SS}	146	V_{SS}	198	V_{CC}
43	V_{SS}	95	V_{CC}	147	A31	199	V_{SS}
44	V_{CC}	96	NC[3]	148	A30	200	V_{CC}
45	V_{CC}	97	V_{SS}	149	A29	201	V_{SS}
46	EADS#	98	V_{CC}	150	V_{CC}	202	A2
47	A20M#	99	D20	151	A28	203	ADS#
48	RESET	100	D19	152	A27	204	BLAST#
49	FLUSH#	101	D18	153	A26	205	V_{CC}
50	INTR	102	V_{CC}	154	A25	206	PLOCK#
51	NMI	103	D17	155	V_{CC}	207	LOCK#
52	V_{SS}	104	V_{SS}	156	V_{SS}	208	V_{SS}

NOTES:

1. This pin location is for the V_{CC5} pin on the embedded IntelDX4 processor. For compatibility with 3.3V processors that have 5V-tolerant input buffers (i.e., embedded IntelDX4 processors), this pin should be connected to a V_{CC} trace, not to the V_{CC} plane.
2. INC. Internal No Connect. These pins are not connected to any internal pad in the embedded Intel486 SX processors. However, signals are defined for the location of the INC pins in the embedded IntelDX2 and IntelDX4 processors. One system design can accommodate any one of these processors provided the purpose of each INC pin is understood before it is used.
3. NC. Do Not Connect. These pins should always remain unconnected. Connection of NC pins to V_{CC}, or V_{SS} or to any other signal can result in component malfunction or incompatibility with future steppings of the Intel486 processors.

Table 4. Pin Cross Reference for 208-Lead SQFP Package (Sheet 1 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	NC	V_{CC}	V_{SS}
A2	202	D0	144	A20M#	47	67	11	2	1
A3	197	D1	143	ADS#	203	96	63	3	10
A4	196	D2	142	AHOLD	17	127	64	9	15
A5	195	D3	141	BE0#	31		66	14	21
A6	193	D4	140	BE1#	32		70	19	28
A7	192	D5	130	BE2#	33		71	20	36
A8	190	D6	129	BE3#	34		72	22	43
A9	187	D7	126	BLAST#	204			23	52
A10	186	D8	124	BOFF#	6			25	53
A11	182	D9	123	BRDY#	5			29	55
A12	180	D10	119	BREQ	30			35	57
A13	178	D11	118	BS16#	7			38	61
A14	177	D12	117	BS8#	8			42	76
A15	174	D13	116	CLK	24			44	81
A16	173	D14	113	D/C#	39			45	88
A17	171	D15	112	DP0	145			54	94
A18	166	D16	108	DP1	125			56	97
A19	165	D17	103	DP2	109			60	104
A20	164	D18	101	DP3	90			62	105
A21	161	D19	100	EADS#	46			69	107
A22	160	D20	99	FLUSH#	49			77	110
A23	159	D21	93	HLDA	26			80	115
A24	158	D22	92	HOLD	16			82	120
A25	154	D23	91	INTR	50			86	122
A26	153	D24	87	KEN#	13			89	132
A27	152	D25	85	LOCK#	207			95	135
A28	151	D26	84	M/IO#	37			98	138
A29	149	D27	83	NMI	51			102	146
A30	148	D28	79	PCD	41			106	156
A31	147	D29	78	PCHK#	4			111	157
		D30	75	PLOCK#	206			114	170
		D31	74	PWT	40			121	175
				RDY#	12			128	181
				RESERVED#	194			131	184
				RESET	48			133	189
				SMI#	65			134	199
				SMIACT#	59			136	201
				SRESET	58			137	208
				STPCLK#	73			139	
				TCK	18			150	
				TDI	168			155	

Table 4. Pin Cross Reference for 208-Lead SQFP Package (Sheet 2 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	NC	V_{CC}	V_{SS}
				TDO	68			162	
				TMS	167			163	
				W/R#	27			169	
								172	
								176	
								179	
								183	
								185	
								188	
								191	
								198	
								200	
								205	

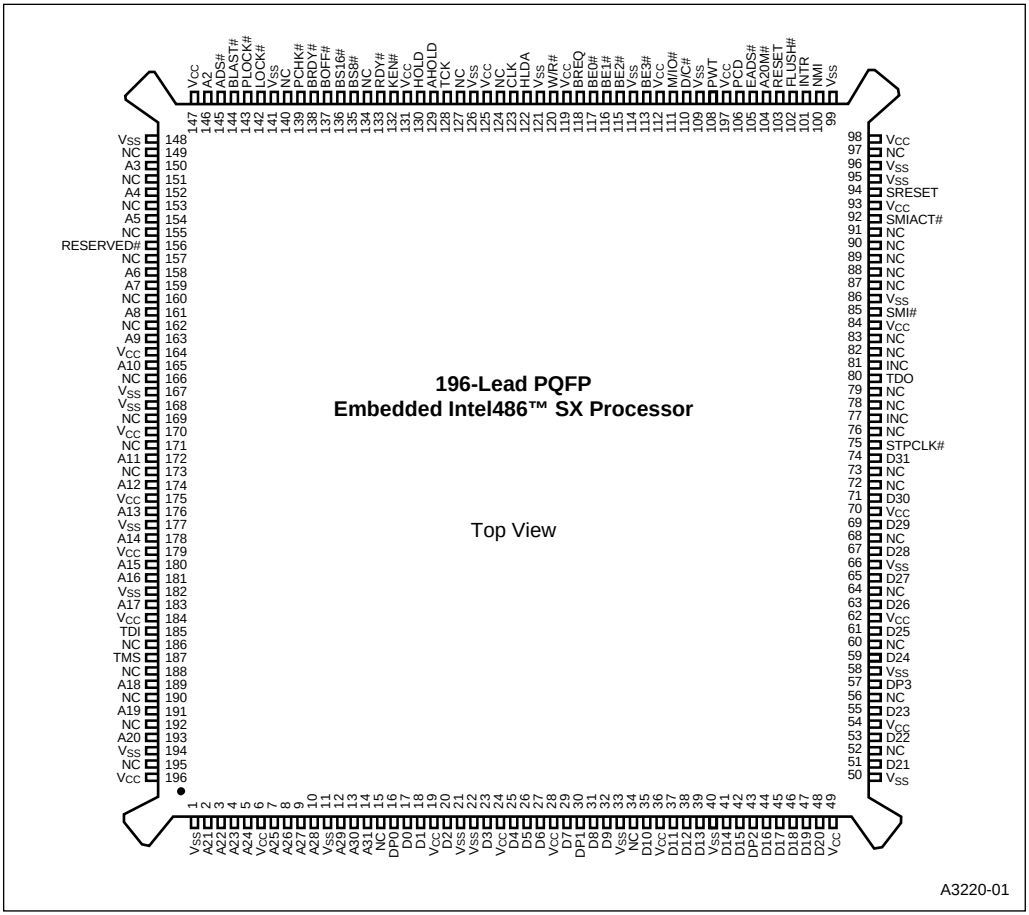


Figure 3. Package Diagram for 196-Lead PQFP Embedded Intel486™ SX Processor

Table 5. Pin Assignment for 196-Lead PQFP Package (Sheet 1 of 2)

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	V_{SS}	50	V_{SS}	99	V_{SS}	148	V_{SS}
2	A21	51	D21	100	NMI	149	NC[1]
3	A22	52	NC[1]	101	INTR	150	A3
4	A23	53	D22	102	FLUSH#	151	NC[1]
5	A24	54	V_{CC}	103	RESET	152	A4
6	V_{CC}	55	D23	104	A20M#	153	NC[1]
7	A25	56	NC[1]	105	EADS#	154	A5
8	A26	57	DP3	106	PCD	155	NC[1]
9	A27	58	V_{SS}	107	V_{CC}	156	RESERVED#
10	A28	59	D24	108	PWT	157	NC[1]
11	V_{SS}	60	NC[1]	109	V_{SS}	158	A6
12	A29	61	D25	110	D/C#	159	A7
13	A30	62	V_{CC}	111	M/IO#	160	NC[1]
14	A31	63	D26	112	V_{CC}	161	A8
15	NC[1]	64	NC[1]	113	BE3#	162	NC[1]
16	DP0	65	D27	114	V_{SS}	163	A9
17	D0	66	V_{SS}	115	BE2#	164	V_{CC}
18	D1	67	D28	116	BE1#	165	A10
19	V_{CC}	68	NC[1]	117	BE0#	166	NC[1]
20	D2	69	D29	118	BREQ	167	V_{SS}
21	V_{SS}	70	V_{CC}	119	V_{CC}	168	V_{SS}
22	V_{SS}	71	D30	120	W/R#	169	NC[1]
23	D3	72	NC[1]	121	V_{SS}	170	V_{CC}
24	V_{CC}	73	NC[1]	122	HLDA	171	NC[1]
25	D4	74	D31	123	CLK	172	A11
26	D5	75	STPCLK#	124	NC[1]	173	NC[1]
27	D6	76	NC[1]	125	V_{CC}	174	A12
28	V_{CC}	77	INC[2]	126	V_{SS}	175	V_{CC}
29	D7	78	NC[1]	127	NC[1]	176	A13
30	DP1	79	NC[1]	128	TCK	177	V_{SS}
31	D8	80	TDO	129	AHOLD	178	A14
32	D9	81	INC[2]	130	HOLD	179	V_{CC}
33	V_{SS}	82	NC[1]	131	V_{CC}	180	A15

Table 5. Pin Assignment for 196-Lead PQFP Package (Sheet 2 of 2)

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
34	NC[1]	83	NC[1]	132	KEN#	181	A16
35	D10	84	V_{CC}	133	RDY#	182	V_{SS}
36	V_{CC}	85	SMI#	134	NC[1]	183	A17
37	D11	86	V_{SS}	135	BS8#	184	V_{CC}
38	D12	87	NC[1]	136	BS16#	185	TDI
39	D13	88	NC[1]	137	BOFF#	186	NC[1]
40	V_{SS}	89	NC[1]	138	BRDY#	187	TMS
41	D14	90	NC[1]	139	PCHK#	188	NC[1]
42	D15	91	NC[1]	140	NC[1]	189	A18
43	DP2	92	SMIACT#	141	V_{SS}	190	NC[1]
44	D16	93	V_{CC}	142	LOCK#	191	A19
45	D17	94	SRESET	143	PLOCK#	192	NC[1]
46	D18	95	V_{SS}	144	BLAST#	193	A20
47	D19	96	V_{SS}	145	ADS#	194	V_{SS}
48	D20	97	NC[1]	146	A2	195	NC[1]
49	V_{CC}	98	V_{CC}	147	V_{CC}	196	V_{CC}

NOTES:

1. NC. Do Not Connect. These pins should always remain unconnected. Connection of NC pins to V_{CC}, or V_{SS} or to any other signal can result in component malfunction or incompatibility with future steppings of the Intel486 processors.
2. INC. Internal No Connect. These pins are not connected to any internal pad in the embedded Intel486 SX processors.

Table 6. Pin Cross Reference for 196-Lead PQFP Package (Sheet 1 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	NC	V_{CC}	V_{SS}
A2	146	D0	17	A20M#	104	15	77	6	1
A3	150	D1	18	ADS#	145	34	81	19	11
A4	152	D2	20	AHOLD	129	52		24	21
A5	154	D3	23	BE0#	117	56		28	22
A6	158	D4	25	BE1#	116	60		36	33
A7	159	D5	26	BE2#	115	64		49	40
A8	161	D6	27	BE3#	113	68		54	50
A9	163	D7	29	BLAST#	144	72		62	58
A10	165	D8	31	BOFF#	137	73		70	66
A11	172	D9	32	BRDY#	138	76		84	86
A12	174	D10	35	BREQ	118	78		93	95
A13	176	D11	37	BS16#	136	79		98	96
A14	178	D12	38	BS8#	135	82		107	99
A15	180	D13	39	CLK	123	83		112	109
A16	181	D14	41	D/C#	110	87		119	114
A17	183	D15	42	DP0	16	88		125	121
A18	189	D16	44	DP1	30	89		131	126
A19	191	D17	45	DP2	43	90		147	141
A20	193	D18	46	DP3	57	91		164	148
A21	2	D19	47	EADS#	105	97		170	167
A22	3	D20	48	FLUSH#	102	124		175	168
A23	4	D21	51	HLDA	122	127		179	177
A24	5	D22	53	HOLD	130	134		184	182
A25	7	D23	55	INTR	101	140		196	194
A26	8	D24	59	KEN#	132	149			
A27	9	D25	61	LOCK#	142	151			
A28	10	D26	63	M/IO#	111	153			
A29	12	D27	65	NMI	100	155			
A30	13	D28	67	PCD	106	157			
A31	14	D29	69	PCHK#	139	160			
		D30	71	PLOCK#	143	162			
		D31	74	PWT	108	166			
				RDY#	133	169			
				RESERVED#	156	171			
				RESET	103	173			
				SMI#	85	186			
				SMIACT#	92	188			
				SRESET	94	190			
				STPCLK#	75	192			

Table 6. Pin Cross Reference for 196-Lead PQFP Package (Sheet 2 of 2)

Address	Pin #	Data	Pin #	Control	Pin #	NC	NC	V_{CC}	V_{SS}
				TCK	128	195			
				TDI	185				
				TDO	80				
				TMS	187				
				W/R#	120				

3.2 Pin Quick Reference

The following is a brief pin description. For detailed signal descriptions refer to Appendix A, “Signal Descriptions,” in the *Embedded Intel486™ Processor Family Developer’s Manual,* order No. 273021.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 1 of 6)

Symbol	Type	Name and Function
CLK	I	**Clock** provides the fundamental timing and internal operating frequency for the embedded Intel486 SX processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31-A4 **A3–A2**	I/O O	**Address Lines** A31–A2, together with the byte enable signals, BE3#–BE0#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the embedded Intel486 SX processor to perform cache line invalidation. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE3# **BE2#** **BE1#** **BE0#**	O O O O	**Byte Enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3#–BE0# are active LOW and are not driven during bus hold. BE3# applies to D31–D24 BE2# applies to D23–D16 BE1# applies to D15–D8 BE0# applies to D7–D0
DATA BUS		
D31–D0	I/O	**Data Lines.** D7–D0 define the least significant byte of the data bus; D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP3–DP0	I/O	There is one **Data Parity** pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the embedded Intel486 SX processor. Even parity information must be driven back into the processor on the data parity pins with the same timing as read information to ensure that the correct parity check status is indicated by the embedded Intel486 SX processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 must be connected to V_{CC} through a pull-up resistor in systems that do not use parity. DP3–DP0 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	**Parity Status** is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the processor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 2 of 6)

Symbol	Type	Name and Function
BUS CYCLE DEFINITION		
M/IO# **D/C#** **W/R#**	O O O	**Memory/Input-Output**, **Data/Control** and **Write/Read** lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. **M/IO# D/C# W/R# Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 HALT/Special Cycle (see details below) 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write **HALT/Special Cycle** **Cycle Name BE3# - BE0# A4-A2** Shutdown 1110 000 HALT 1011 000 Stop Grant bus cycle 1011 100
LOCK#	O	**Bus Lock** indicates that the current bus cycle is locked. The embedded Intel486 SX processor does not allow a bus hold when LOCK# is asserted (address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when Ready is returned. LOCK# is active LOW and not driven during bus hold. Locked read cycles are not transformed into cache fill cycles when KEN# is returned active.
PLOCK#	O	**Pseudo-Lock** indicates that the current bus transaction requires more than one bus cycle to complete. For the embedded Intel486 SX processor, examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). The embedded Intel486 SX processor drives PLOCK# active until the addresses for the last bus cycle of the transaction are driven, regardless of whether RDY# or BRDY# have been returned. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock in which Ready is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	**Address Status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock in which the addresses are driven. ADS# is active LOW and not driven during bus hold.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 3 of 6)

Symbol	Type	Name and Function
RDY#	I	**Non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the embedded Intel486 SX processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the embedded Intel486 SX processor while AHOLD is active. RDY# is active LOW and is not provided with an internal pull-up resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.
BURST CONTROL		
BRDY#	I	**Burst Ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. Data presented on the data bus is strobed into the embedded Intel486 SX processor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	**Burst Last** signal indicates that the next time BRDY# is returned, the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	**Reset** input forces the embedded Intel486 SX processor to begin execution at a known state. The processor cannot begin executing instructions until at least 1 ms after V_{CC}, and CLK have reached their proper DC and AC specifications. The RESET pin must remain active during this time to ensure proper processor operation. However, for warm resets, RESET should remain active for at least 15 CLK periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
INTR	I	**Maskable Interrupt** indicates that an external interrupt has been generated. When the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The embedded Intel486 SX processor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure processor recognition of the interrupt. INTR is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	**Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising-edge sensitive and must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 4 of 6)

Symbol	Type	Name and Function
SRESET	I	**Soft Reset** pin duplicates all functionality of the RESET pin except that the SMBASE register retains its previous value. For soft resets, SRESET must remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SMI#	I	**System Management Interrupt** input invokes System Management Mode (SMM). SMI# is a falling-edge triggered signal which forces the embedded Intel486 SX processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The embedded Intel486 SX processor latches the falling edge of one pending SMI# signal while it is executing an existing SMI#. The nested SMI# is not recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	**System Management Interrupt Active**, an active LOW output, indicates that the embedded Intel486 SX processor is operating in SMM. It is asserted when the processor begins to execute the SMI# state save sequence and remains active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	**Stop Clock Request** input signal indicates a request was made to turn off or change the CLK input frequency. When the embedded Intel486 SX processor recognizes a STPCLK#, it stops execution on the next instruction boundary (unless superseded by a higher priority interrupt), empties all internal pipelines and write buffers, and generates a Stop Grant bus cycle. STPCLK# is active LOW. Though STPCLK# has an internal pull-up resistor, an external 10-KΩ pull-up resistor is needed if the STPCLK# pin is not used. **STPCLK# is an asynchronous signal, but must remain active until the embedded Intel486 SX processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle.**
BUS ARBITRATION		
BREQ	O	**Bus Request** signal indicates that the embedded Intel486 SX processor has internally generated a bus request. BREQ is generated whether or not the processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	**Bus Hold Request** allows another bus master complete control of the embedded Intel486 SX processor bus. In response to HOLD going active, the processor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The embedded Intel486 SX processor remains in this state until HOLD is de-asserted. HOLD is active HIGH and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.
HLDA	O	**Hold Acknowledge** goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the embedded Intel486 SX processor has given the bus to another local bus master. HLDA is driven active in the same clock that the processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 5 of 6)

Symbol	Type	Name and Function
BOFF#	I	**Backoff** input forces the embedded Intel486 SX processor to float its bus in the next clock. The processor floats all pins normally floated during bus hold but HLDA is not asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The embedded Intel486 SX processor remains in bus hold until BOFF# is negated. If a bus cycle is in progress when BOFF# is asserted the cycle is restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	**Address Hold** request allows another bus master access to the embedded Intel486 SX processor's address bus for a cache invalidation cycle. The processor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold, the remainder of the bus remains active. AHOLD is active HIGH and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	**External Address** - This signal indicates that a *valid* external address has been driven onto the embedded Intel486 SX processor address pins. This address is used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	**Cache Enable** pin is used to determine whether the current cycle is cacheable. When the embedded Intel486 SX processor generates a cycle that can be cached and KEN# is active one clock before RDY# or BRDY# during the first transfer of the cycle, the cycle becomes a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill causes the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	**Cache Flush** input forces the embedded Intel486 SX processor to flush its entire internal cache. FLUSH# is active LOW and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock.
PAGE CACHEABILITY		
PWT **PCD**	O O	**Page Write-Through** and **Page Cache Disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3) when paging is enabled. When paging is disabled, the embedded Intel486 SX processor ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.

Table 7. Embedded Intel486™ SX Processor Pin Descriptions (Sheet 6 of 6)

Symbol	Type	Name and Function
BUS SIZE CONTROL		
BS16# **BS8#**	I I	**Bus Size 16** and **Bus Size 8** pins (bus sizing pins) cause the embedded Intel486 SX processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The processor uses the state of these pins in the clock before Ready to determine bus size. These signals are active LOW and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	**Address Bit 20 Mask** pin, when asserted, causes the embedded Intel486 SX processor to mask physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at 1 Mbyte, which occurs on the 8086 processor. A20M# is active LOW and should be asserted only when the embedded Intel486 SX processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled HIGH at the falling edge of RESET.
TEST ACCESS PORT		
TCK	I	**Test Clock**, an input to the embedded Intel486 SX processor, provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information (via TMS) and data (via TDI) into the component on the rising edge of TCK. Data is clocked out of the component (via TDO) on the falling edge of TCK. TCK is provided with an internal pull-up resistor.
TDI	I	**Test Data Input** is the serial input used to shift JTAG instructions and data into the processor. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR Test Access Port (TAP) controller states. During all other TAP controller states, TDI is a “don’t care.” TDI is provided with an internal pull-up resistor.
TDO	O	**Test Data Output** is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	**Test Mode Select** is decoded by the JTAG TAP to select test logic operation. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.
RESERVED PINS		
RESERVED#	I	**Reserved** is reserved for future use. This pin MUST be connected to an external pull-up resistor circuit. The recommended resistor value is 10 kOhms. The pull-up resistor must be connected only to the RESERVED# pin. **Do not share this resistor with other pins requiring pull-ups.**

Table 8. Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States
BREQ	HIGH			Previous State
HLDA	HIGH			As per HOLD
BE3#-BE0#	LOW		•	Previous State
PWT, PCD	HIGH		•	Previous State
W/R#, M/IO#, D/C#	HIGH/LOW		•	Previous State
LOCK#	LOW		•	HIGH (inactive)
PLOCK#	LOW		•	HIGH (inactive)
ADS#	LOW		•	HIGH (inactive)
BLAST#	LOW		•	Previous State
PCHK#	LOW			Previous State
A3-A2	HIGH	•	•	Previous State
SMIACT#	LOW			Previous State

NOTES: The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 9. Input/Output Pins

Name	Active Level	Output Signal		
		Floated During Address Hold	Floated During Bus Hold	During Stop Grant and Stop Clock States
D31-D0	HIGH		•	Floated
DP3–DP0	HIGH		•	Floated
A31-A4	HIGH	•	•	Previous State

NOTES: The term “Previous State” means that the processor maintains the logic level applied to the signal pin just before the processor entered the Stop Grant state. This conserves power by preventing the signal pin from floating.

Table 10. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Failing Edge of TCK
TMS	Input	Rising Edge of TCK

Table 11. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
BS16#, BS8#	LOW	Synchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
RESERVED#	LOW	Asynchronous	Pull-Up
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up[1]
TCK	HIGH		Pull-Up
TDI	HIGH		Pull-Up
TMS	HIGH		Pull-Up

NOTES:

1. Though STPCLK# has an internal pull-up resistor, an external 10-KΩ pull-up resistor is needed if the STPCLK# pin is not used.

4.0 ARCHITECTURAL AND FUNCTIONAL OVERVIEW

The embedded Intel486 SX processor architecture is essentially the same as the Intel486 SX processor with a 1X clock (CLK) input. Refer to the *Embedded Intel486™ Processor Family Developer's Manual,* order No. 273021, for a description of the Intel486 SX processor.

Note that the embedded Intel486 SX processor has one pin reserved for possible future use. This pin, an input signal, is called RESERVED# and must be connected to a 10-KΩ pull-up resistor. The pull-up resistor must be connected only to the RESERVED# pin. **Do not share this resistor with other pins requiring pull-ups.**

4.1 CPUID Instruction

The embedded Intel486 SX processor supports the CPUID instruction (see Table 12). Because not all Intel processors support the CPUID instruction, a simple test can determine if the instruction is supported. The test involves the processor's ID Flag, which is bit 21 of the EFLAGS register. If software can change the value of this flag, the CPUID instruction is available. The actual state of the ID Flag bit is irrelevant and provides no significance to the hardware. This bit is cleared (reset to zero) upon device reset (RESET or SRESET) for compatibility with Intel486 processor designs that do not support the CPUID instruction.

CPUID-instruction details are provided here for the embedded Intel486 SX processor. Refer to Intel Application Note AP-485 *Intel Processor Identification with the CPUID Instruction* (Order No. 241618) for a description that covers all aspects of the CPUID instruction and how it pertains to other Intel processors.

4.1.1 Operation of the CPUID Instruction

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, EDX, and ECX.

Table 12. CPUID Instruction Description

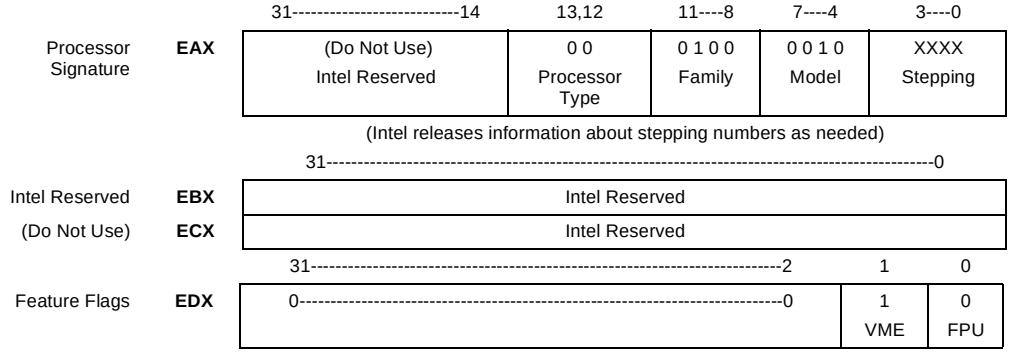
OP CODE	Instruction	Processor Core Clocks	Parameter passed in EAX (Input Value)	Description
0F A2	CPUID	9	0	Vendor (Intel) ID String
		14	1	Processor Identification
		9	> 1	Undefined (Do Not Use)

Vendor ID String - When the parameter passed in EAX is 0 (zero), the register values returned upon instruction execution are shown in the following table.

		31----------24	23----------16	15----------8	7----------0
High Value (= 1)	**EAX**	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1
Vendor ID String	**EBX**	u (75)	n (6E)	e (65)	G (47)
(ASCII	**EDX**	I (49)	e (65)	n (6E)	i (69)
Characters)	**ECX**	l (6C)	e (65)	t (74)	n (6E)

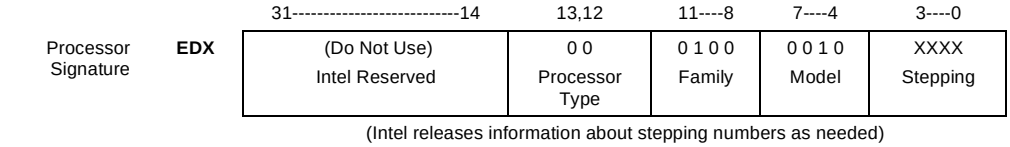
The values in EBX, EDX and ECX indicate an Intel processor. When taken in the proper order, they decode to the string "GenuineIntel."

Processor Identification - When the parameter passed to EAX is 1 (one), the register values returned upon instruction execution are:



4.2 Identification After Reset

Processor Identification - Upon reset, the EDX register contains the processor signature:



4.3 Boundary Scan (JTAG)

4.3.1 Device Identification

Tables 13 and 14 show the 32-bit code for the embedded Intel486 SX processor. This code is loaded into the Device Identification Register.

Table 13. Boundary Scan Component Identification Code (3.3 Volt Processor)

Version	Part Number				Mfg ID	1
	V_{CC} 0=5 V 1=3.3 V	Intel Architecture Type	Family 0100 = Intel486 CPU Family	Model 00010 = embedded Intel486 SX processor	009H = Intel	
31----28	27	26----------21	20----17	16--------12	11----------1	0
XXXX	1	000001	0100	00010	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x828 2013 (Hex)

Table 14. Boundary Scan Component Identification Code (5 Volt Processor)

Version	Part Number				Mfg ID	1
	V_{CC} 0=5 V 1=3.3 V	Intel Architecture Type	Family 0100 = Intel486 CPU Family	Model 00010 = embedded Intel486 SX processor	009H = Intel	
31----28	27	26----------21	20----17	16--------12	11----------1	0
XXXX	0	000001	0100	00010	00000001001	1

(Intel releases information about version numbers as needed)
Boundary Scan Component Identification Code = x028 2013 (Hex)

4.3.2 Boundary Scan Register Bits and Bit Order

The boundary scan register contains a cell for each pin as well as cells for control of bidirectional and three-state pins. There are “Reserved” bits which correspond to no-connect (N/C) signals of the embedded Intel486 SX processor. Control registers WRCTL, ABUSCTL, BUSCTL, and MISCCTL are used to select the direction of bidirectional or three-state output signal pins. A “1” in these cells designates that the associated bus or bits are floated if the pins are three-state, or selected as input if they are bidirectional.

- WRCTL controls D31-D0 and DP3–DP0
- ABUSCTL controls A31-A2
- BUSCTL controls ADS#, BLAST#, PLOCK#, LOCK#, W/R#, BE0#, BE1#, BE2#, BE3#, M/IO#, D/C#, PWT, and PCD
- MISCCTL controls PCHK#, HLDA, and BREQ

The following is the bit order of the embedded Intel486 SX processor boundary scan register:

TDO ← A2, A3, A4, A5, RESERVED#, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, DP0, D0, D1, D2, D3, D4, D5, D6, D7, DP1, D8, D9, D10, D11, D12, D13, D14, D15, DP2, D16, D17, D18, D19, D20, D21, D22, D23, DP3, D24, D25, D26, D27, D28, D29, D30, D31, STPCLK#, Reserved, Reserved, SMI#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3#, BE2#, BE1#, BE0#, BREQ, W/R#, HLDA, CLK, Reserved, AHOLD, HOLD, KEN#, RDY#, BS8#, BS16#, BOFF#, BRDY#, PCHK#, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRCTL ← **TDI**

5.0 ELECTRICAL SPECIFICATIONS

5.1 Maximum Ratings

Table 15 is a stress rating only. Extended exposure to the Maximum Ratings may affect device reliability.

Furthermore, although the embedded Intel486 SX processor contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Functional operating conditions are given in **Section 5.2, DC Specifications** and **Section 5.3, AC Specifications**.

Table 15. Absolute Maximum Ratings

Case Temperature under Bias	-65 °C to +110 °C
Storage Temperature	-65 °C to +150 °C
DC Voltage on Any Pin with Respect to Ground	-0.5 V to V_{CC} + 0.5 V
Supply Voltage VCC with Respect to VSS	-0.5 V to +6.5 V

5.2 DC Specifications

The following tables show the operating supply voltages, DC I/O specifications, and component power consumption for the embedded Intel486 SX processor.

Table 16. Operating Supply Voltages

Product	V_{CC}
SB80486SXSC33	3.3 V ± 0.3 V
KU80486SXSA33	5.0 V ± 0.25 V

Table 17. 3.3 V DC Specifications

Functional Operating Range: V_{CC} = 3.3 V ± 0.3 V, T_{CASE}=0 °C to +85 °C

Symbol	Parameter	Min.	Max.	Unit	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC} +0.3	V	Note 1
V_{IHC}	Input HIGH Voltage of CLK	V_{CC} -0.6	V_{CC} +0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 µA		 0.4 0.2	 V V	
V_{OH}	Output HIGH Voltage I_{OH} = -2.0 mA I_{OH} = -100 µA	 2.4 V_{CC} -0.2		 V V	
I_{LI}	Input Leakage Current		15	µA	Note 2
I_{IH}	Input Leakage Current SRESET		200 300	µA µA	Note 3 Note 3
I_{IL}	Input Leakage Current		400	µA	Note 4
I_{LO}	Output Leakage Current		15	µA	
C_{IN}	Input Capacitance		10	pF	Note 5
C_{OUT}	I/O or Output Capacitance		10	pF	Note 5
C_{CLK}	CLK Capacitance		6	pF	Note 5

NOTES:

1. All inputs except CLK.
2. This parameter is for inputs without pull-up or pull-down resistors and $0V \le V_{IN} \le V_{CC}$.
3. This parameter is for inputs with pull-down resistors and V_{IH} = 2.4V.
4. This parameter is for inputs with pull-up resistors and V_{IL} = 0.4V.
5. F_C=1 MHz. Not 100% tested.

Table 18. 3.3 V I_{CC} Values
Functional Operating Range: V_{CC} = 3.3 V ±0.3 V; T_{CASE} = 0°C to +85°C

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	25 MHz 33 MHz		315 mA 415 mA	Note 1
I_{CC} Active (Thermal Design)	25 MHz 33 MHz	220 mA 289 mA	292 mA 356 mA	Notes 2, 3, 4
I_{CC} Stop Grant	25 MHz 33 MHz	20 mA 25 mA	40 mA 50 mA	Note 5
I_{CC} Stop Clock	0 MHz	100 µA	1 mA	Note 6

NOTES:

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V_{CC} = 3.6V.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V_{CC} = 3.3V.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V_{CC} = 3.3V, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the embedded Intel486 SX processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the embedded Intel486 SX processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0 V, respectively, in order to meet the I_{CC} Stop Clock specifications.

Table 19. 5 V DC Specifications
Functional operating range: V_{CC} = 5V ± 0.25V; T_{CASE} = 0°C to +85°C

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input LOW Voltage	-0.3	+0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}+0.3	V	
V_{OL}	Output LOW Voltage		0.45	V	Note 1
V_{OH}	Output HIGH Voltage	2.4		V	Note 2
I_{LI}	Input Leakage Current		15	µA	Note 3
I_{IH}	Input Leakage Current SRESET		200 300	µA µA	Note 4 Note 4
I_{IL}	Input Leakage Current		400	µA	Note 5
I_{LO}	Output Leakage Current		15	µA	
C_{IN}	Input Capacitance		20	pF	Note 6
C_{OUT}	Output or I/O Capacitance		20	pF	Note 6
C_{CLK}	CLK Capacitance		20	pF	Note 6

NOTES:

1. This parameter is measured at:
   Address, Data, BE*n*# 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data, BE*n*# -1.0 mA
   Definition, Control -0.9 mA
3. This parameter is for inputs without pull-ups or pull-downs and $0V \le V_{IN} \le V_{CC}$.
4. This parameter is for inputs with pull-downs and V_{IH} = 2.4V.
5. This parameter is for inputs with pull-ups and V_{IL} = 0.45V.
6. F_C=1 MHz; Not 100% tested.

Table 20. 5 V I_{CC} Values
Functional Operating Range: V_{CC} = 5V ±0.25V; T_{CASE} = 0°C to +85°C

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	25 MHz 33 MHz		560 mA 685 mA	Note 1
I_{CC} Active (Thermal Design)	25 MHz 33 MHz	378 mA 497 mA	535 mA 654 mA	Notes 2, 3, 4
I_{CC} Stop Grant	25 MHz 33 MHz	35 mA 40 mA	65 mA 80 mA	Note 5
I_{CC} Stop Clock	0 MHz	200 µA	2 mA	Note 6

NOTES:

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at V_{CC} = 5.25V.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at V_{CC} = 5V.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at V_{CC} = 5V, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the embedded Intel486 SX processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.

5.3 AC Specifications

The AC specifications for the embedded Intel486 SX processor are given in this section.

Table 21. AC Characteristics

T_{CASE} = 0°C to +85°C; C_L = 50pF, unless otherwise specified. (Sheet 1 of 2)

	CLK Frequency	8	33	8	33	MHz		Note 1
t_1	CLK Period	30	125	30	125	ns	4	
t_{1a}	CLK Period Stability		±250		±250	ps	4	Adjacent clocks
t_2	CLK High Time	11		11		ns	4	at 2V
t_3	CLK Low Time	11		11		ns	4	at 0.8V
t_4	CLK Fall Time		3		3	ns	4	2V to 0.8V
t_5	CLK Rise Time		3		3	ns	4	0.8V to 2V
t_6	A31–A2, PWT, PCD, BE3–BE0#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT# Valid Delay	3	16	3	16	ns	8	
t_7	A31–A2, PWT, PCD, BE3–BE0#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA Float Delay		20		20	ns	9	Note 2
t_8	PCHK# Valid Delay	3	22	3	22	ns	7	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	20	3	20	ns	8	
t_9	BLAST#, PLOCK# Float Delay		20		20	ns	9	Note 2
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay	3	19	3	18	ns	8	
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay		20		20	ns	9	Note 2
t_{12}	EADS# Setup Time	6		5		ns	5	
t_{13}	EADS# Hold Time	3		3		ns	5	
t_{14}	KEN#, BS16#, BS8# Setup Time	6		5		ns	5	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		3		ns	5	
t_{16}	RDY#, BRDY# Setup Time	6		5		ns	6	
t_{17}	RDY#, BRDY# Hold Time	3		3		ns	6	
t_{18}	HOLD, AHOLD Setup Time	6		6		ns	5	
t_{18a}	BOFF# Setup Time	9		8		ns	5	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	5	

Table 21. AC Characteristics

T_{CASE} = 0°C to +85°C; C_L = 50pF, unless otherwise specified. (Sheet 2 of 2)

t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Setup Time	6		5		ns	5	Note 3
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET Hold Time	3		3		ns	5	Note 3
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time	6		5		ns	6 5	
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time	3		3		ns	6 5	

NOTES:

1. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
2. Not 100% tested, guaranteed by design characterization.
3. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 22. AC Specifications for the Test Access Port
(Both 3.3V SQFP and 5V PQFP Processors)
T_{CASE} = 0°C to +85°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	TCK Frequency		8	MHz		Note 1
t_{25}	TCK Period	125		ns	10	
t_{26}	TCK High Time	40		ns	10	@ 2.0V
t_{27}	TCK Low Time	40		ns	10	@ 0.8V
t_{28}	TCK Rise Time		8	ns	10	Note 2
t_{29}	TCK Fall Time		8	ns	10	Note 2
t_{30}	TDI, TMS Setup Time	8		ns	11	Note 3
t_{31}	TDI, TMS Hold Time	10		ns	11	Note 3
t_{32}	TDO Valid Delay	3	30	ns	11	Note 3
t_{33}	TDO Float Delay		36	ns	11	Note 3
t_{34}	All Outputs (except TDO) Valid Delay	3	30	ns	11	Note 3
t_{35}	All Outputs (except TDO) Float Delay		36	ns	11	Note 3
t_{36}	All Inputs (except TDI, TMS, TCK) Setup Time	8		ns	11	Note 3
t_{37}	All Inputs (except TDI, TMS, TCK) Hold Time	10		ns	11	Note 3

NOTES:

1. TCK period ≤ CLK period.
2. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
3. Parameters t_{30} – t_{37} are measured from TCK.

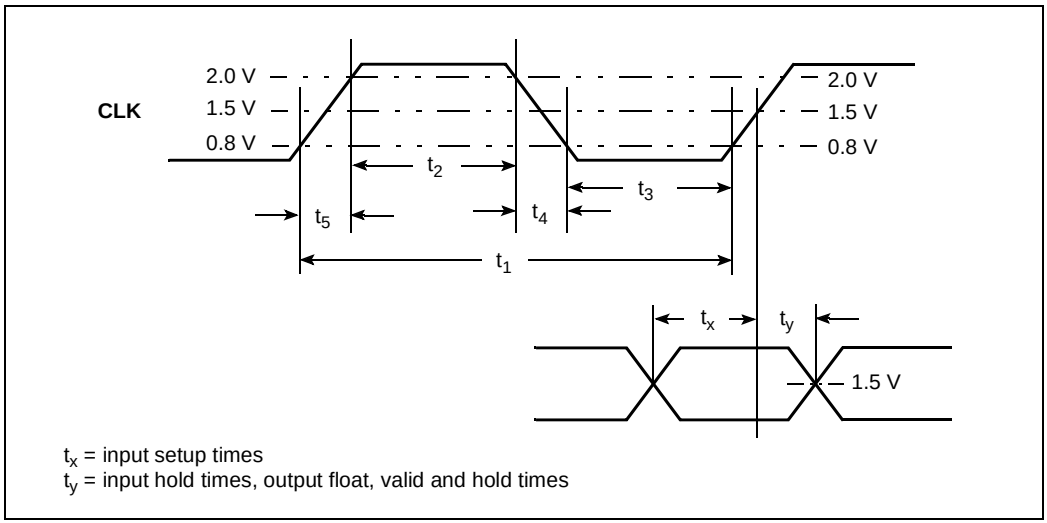


Figure 4. CLK Waveform

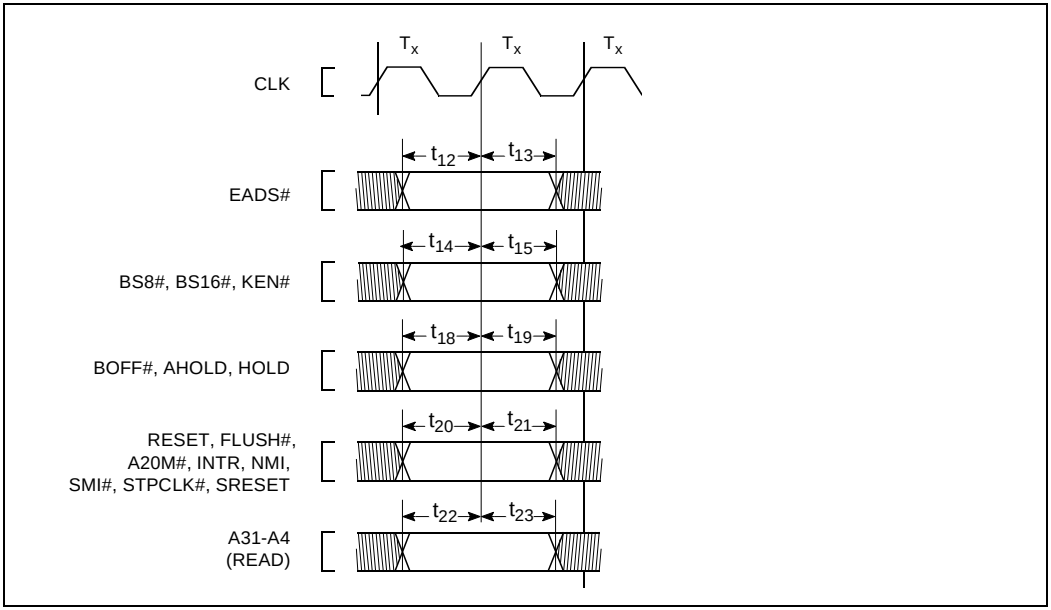


Figure 5. Input Setup and Hold Timing

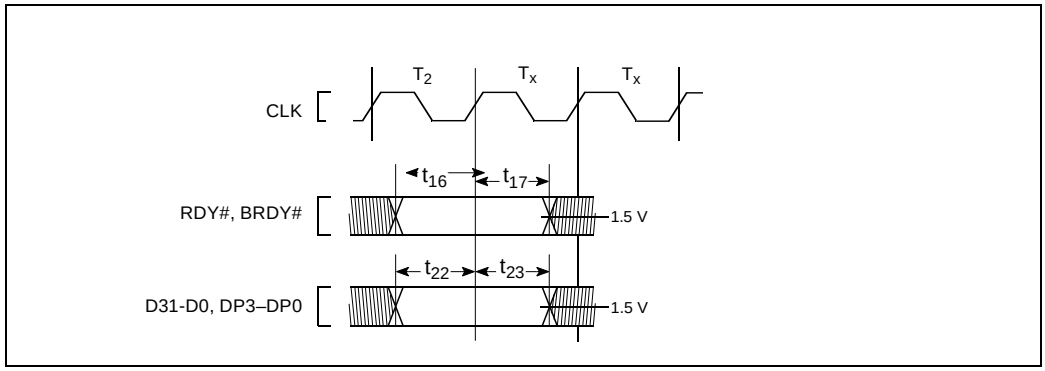


Figure 6. Input Setup and Hold Timing

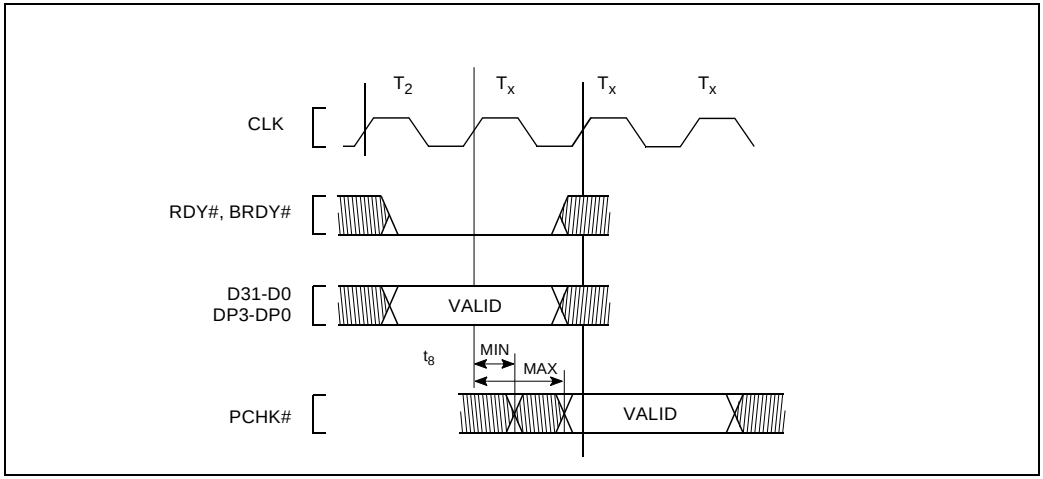


Figure 7. PCHK# Valid Delay Timing

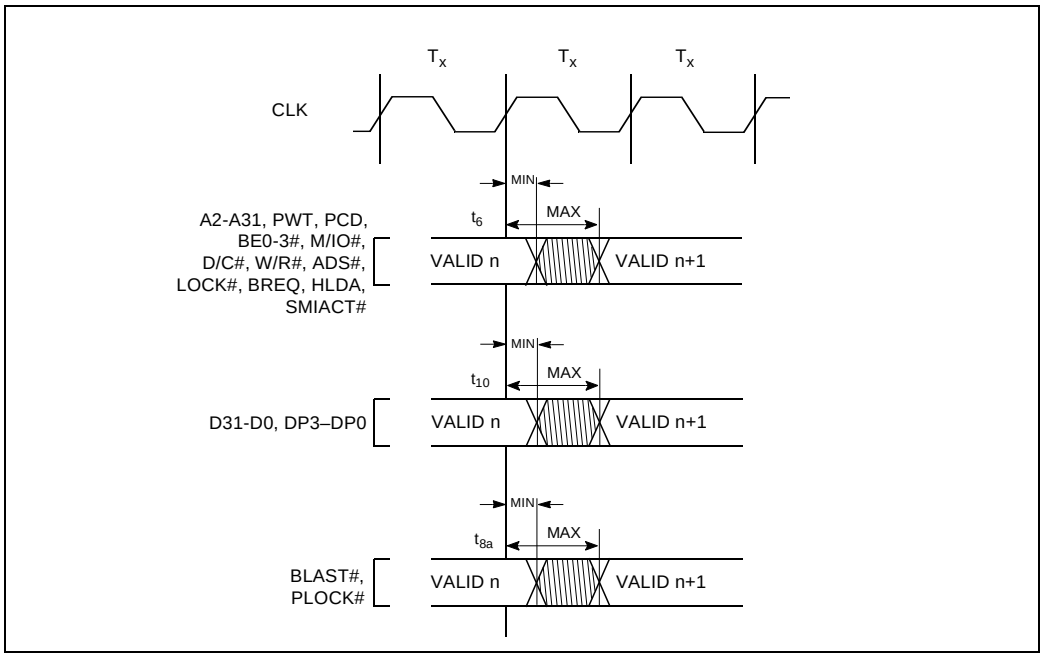


Figure 8. Output Valid Delay Timing

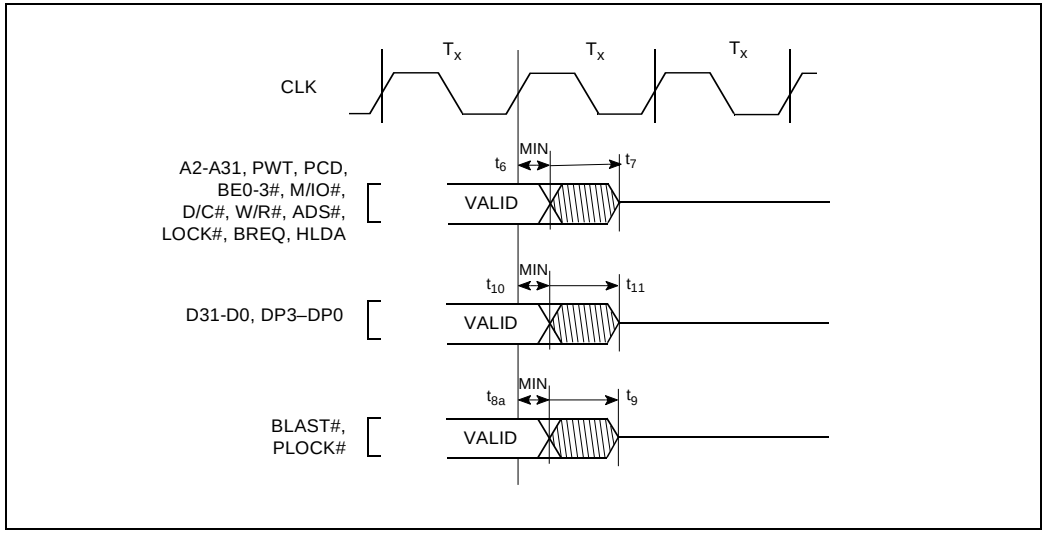


Figure 9. Maximum Float Delay Timing

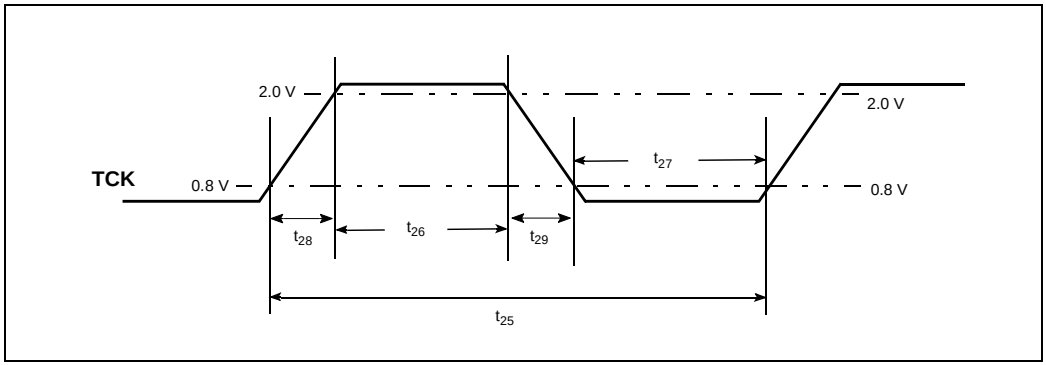


Figure 10. TCK Waveform

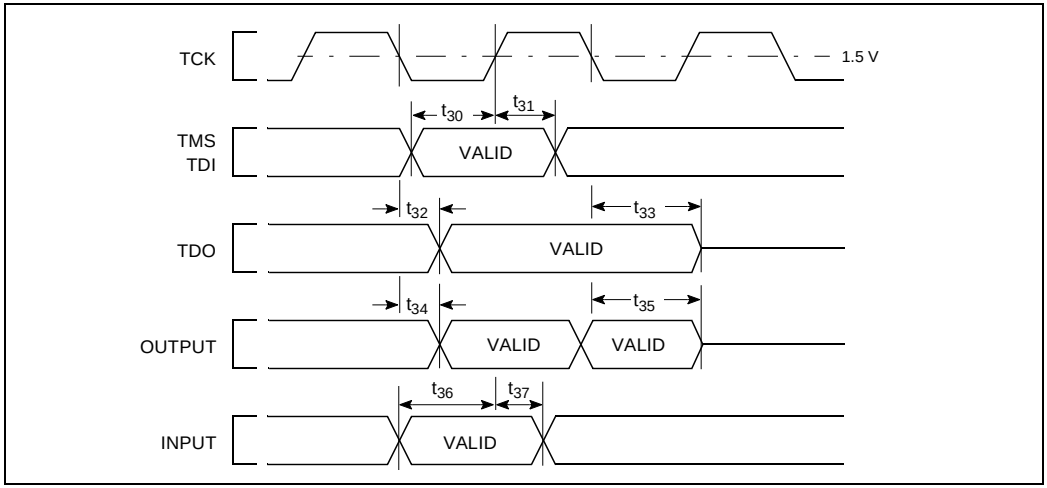
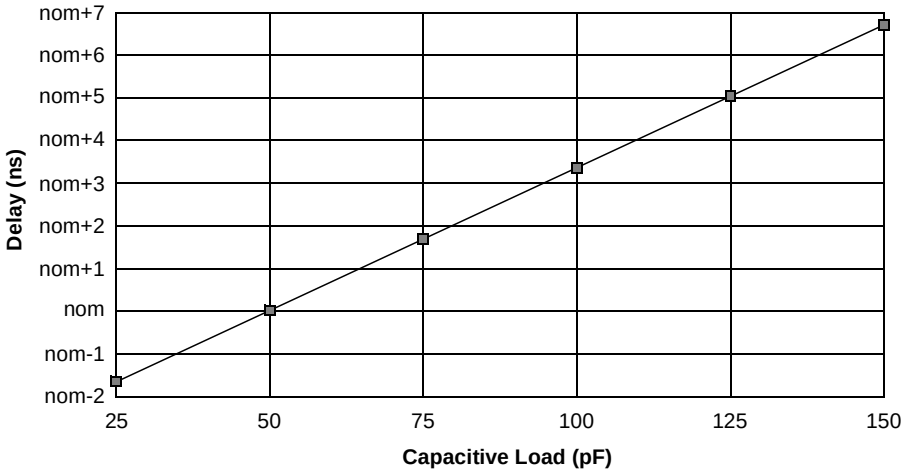


Figure 11. Test Signal Timing Diagram

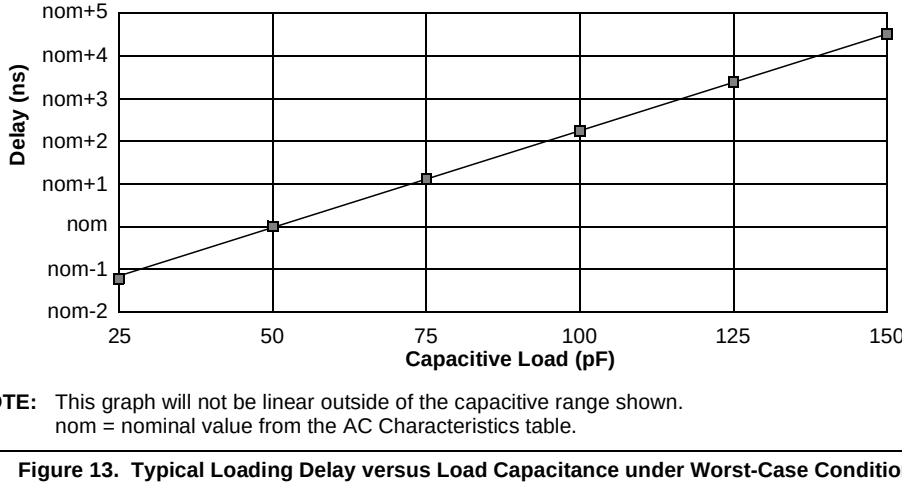
5.4 Capacitive Derating Curves

The following graphs are the capacitive derating curves for the embedded Intel486 SX processor.



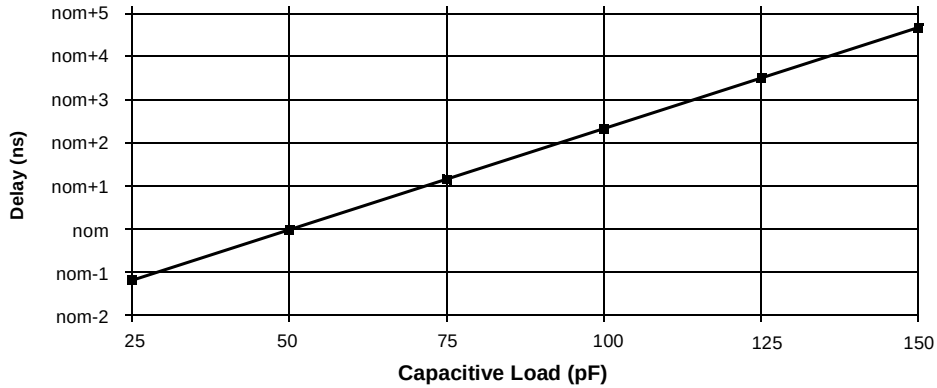
NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 12. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition, 3.3 V Processor



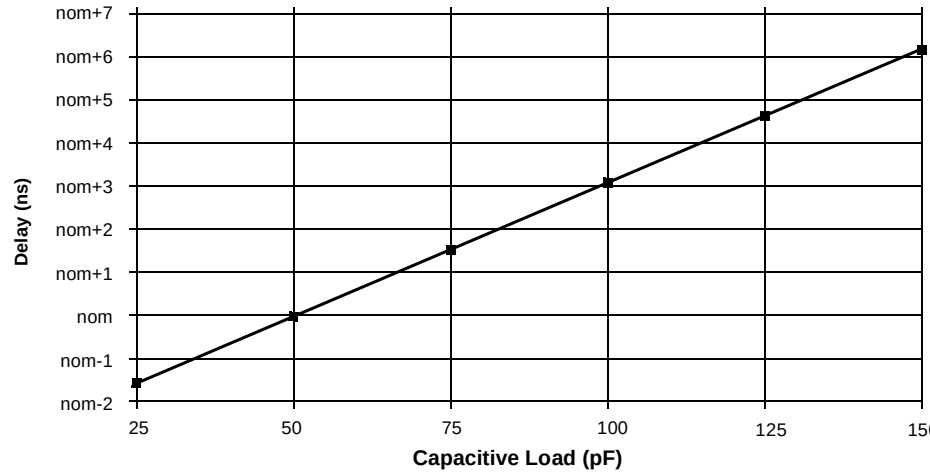
NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 13. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition, 3.3 V Processor



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 14. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition, 5 V Processor



NOTE: This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 15. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition, 5 V Processor

6.0 MECHANICAL DATA

This section describes the packaging dimensions and thermal specifications for the embedded Intel486 SX processor.

6.1 Package Dimensions

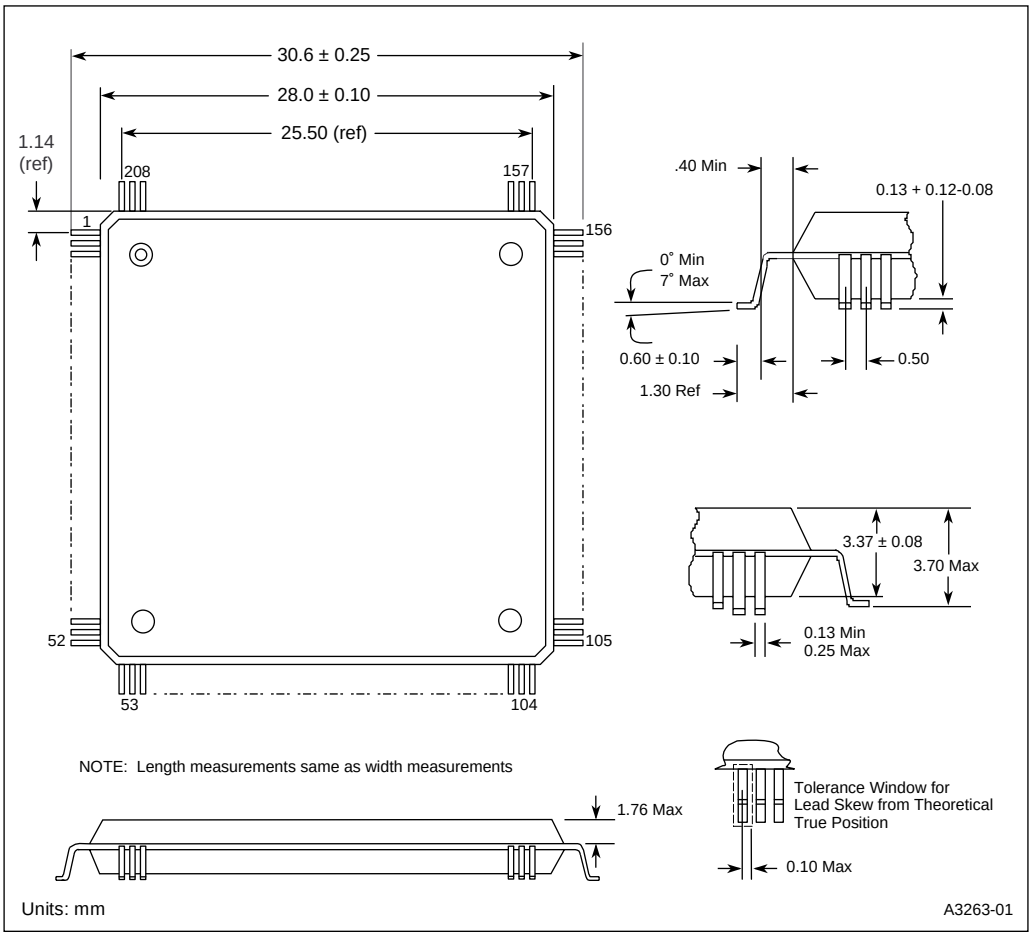
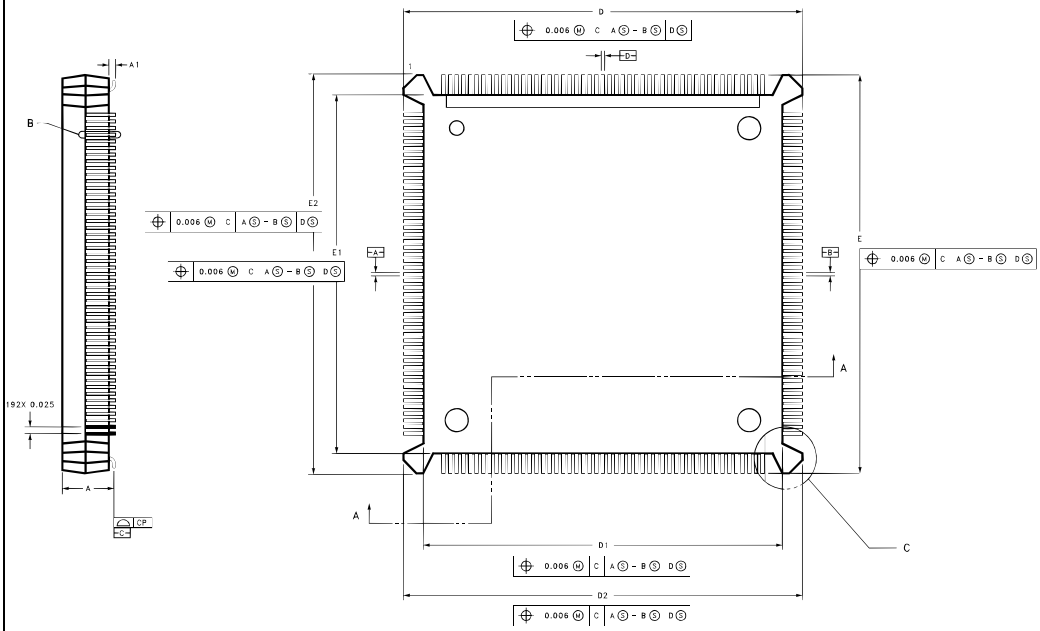


Figure 16. 208-Lead SQFP Package Dimensions



NOTE:
Interpret dimensions and tolerances in accordance with ANSI Y14.5M-1982.

Figure 17. Principal Dimensions and Data for 196-Lead Plastic Quad Flat Pack Package

Table 23. Symbol List and Dimensions for 196-Lead PQFP Package

Symbol	Description of Dimensions	Min	Max
A	**Package Height:** Distance from the seating plane to the highest point of body.	0.160	0.175
A1	**Standoff:** The distance from the seating plane to the base plane.	0.020	0.035
D, E	**Overall Package Dimension:** Lead tip to lead tip.	1.470	1.485
D1, E1	Plastic Body Dimension	1.347	1.353
D2, E2	Bumper Distance		
	Without FLASH	1.497	1.503
	With FLASH	1.497	1.510
CP	Seating Plane Coplanarity	0.000	0.004

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions are in inches.

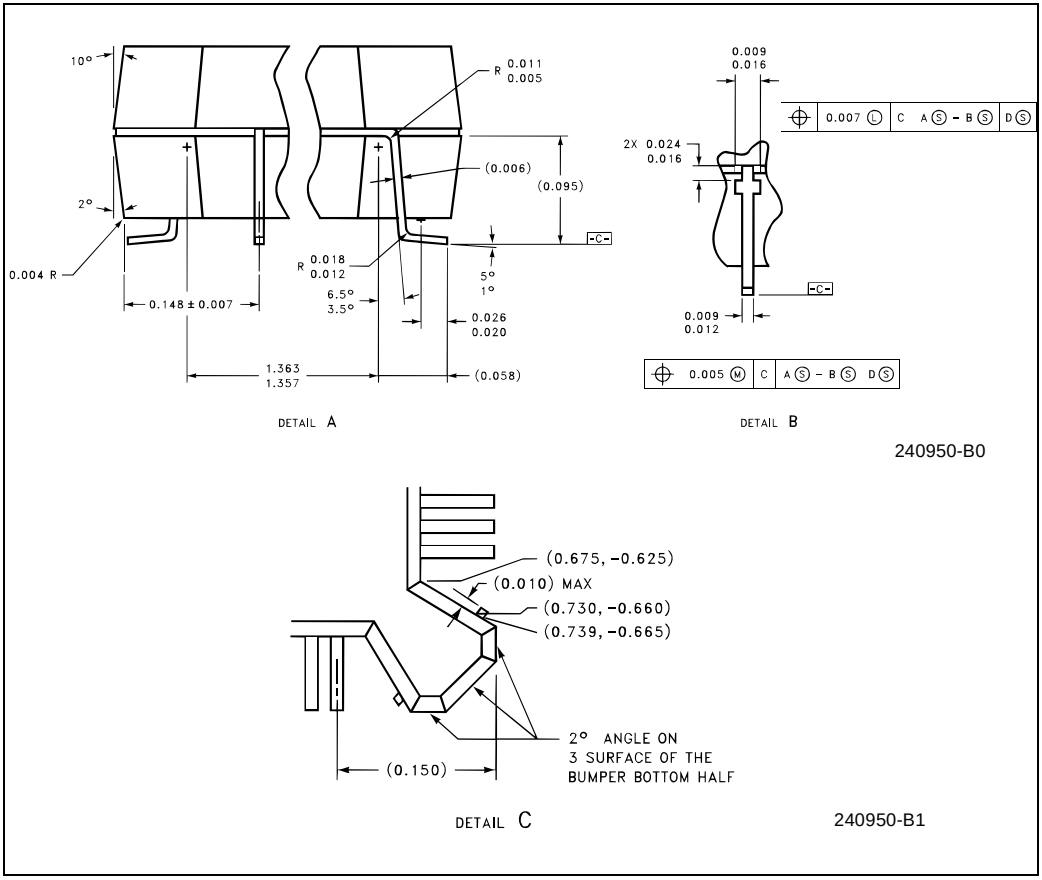


Figure 18. Typical Lead for 196-Lead PQFP Package

6.2 Package Thermal Specifications

The embedded Intel486 SX processor is specified for operation when the case temperature (T_C) is within the range of 0°C to 85°C. T_C may be measured in any environment to determine whether the processor is within the specified operating range.

The ambient temperature (T_A) can be calculated from θ_{JC} and θ_{JA} from the following equations:

$$T_J = T_C + P * \theta_{JC}$$
$$T_A = T_J - P * \theta_{JA}$$

$$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$$
$$T_A = T_C - P * [\theta_{JA} - \theta_{JC}]$$

Where T_J, T_A, T_C equals Junction, Ambient and Case Temperature respectively. θ_{JC}, θ_{JA} equals Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively. P is defined as Maximum Power Consumption.

Values for θ_{JA} and θ_{JC} are given in the following tables for each product operating at 33 MHz. Maximum T_A is shown for each product operating at 25 MHz and 33 MHz.

Table 24. Thermal Resistance, θ_{JA} (°C/W)

	θ_{JA} vs. Airflow — ft/min. (m/sec)			
	0 (0)	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**
208-Lead SQFP (3.3V) - Without Heat Sink	36.0	27.5	25.0	22.5
196-Lead PQFP (5V) - Without Heat Sink	20.5	16.5	14.0	12.5
196-Lead PQFP (5V) - With Heat Sink*	17.0	10.5	8.5	8.0

*0.350" high omnidirectional heat sink.

Table 25. Thermal Resistance, θ_{JC} (°C/W)

	θ_{JC} vs. Airflow — ft/min. (m/sec)			
	0 (0)	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**
	0	200	400	600
208-Lead SQFP (3.3V)	4.0	7.5	8.0	8.5
196-Lead PQFP (5V)	3.5	-	-	-

Table 26. Maximum $T_{ambient}$, T_A max (°C)

	Airflow — ft/min. (m/sec)				
	Freq. (MHz)	**0 (0)**	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**
208-Lead SQFP (3.3V)	25	54	66	69	72
Without Heat Sink	33	47	62	65	69
196-Lead PQFP (5V)	25	40	50	57	61
Without Heat Sink	33	29	42	51	56
196-Lead PQFP (5V)	25	49	66	72	73
With Heat Sink	33	41	62	69	70