

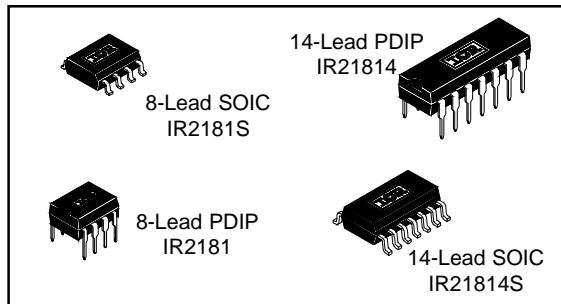
IR2181(4)(S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
 - Fully operational to +600V
 - Tolerant to negative transient voltage
 - dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A

Packages



Description

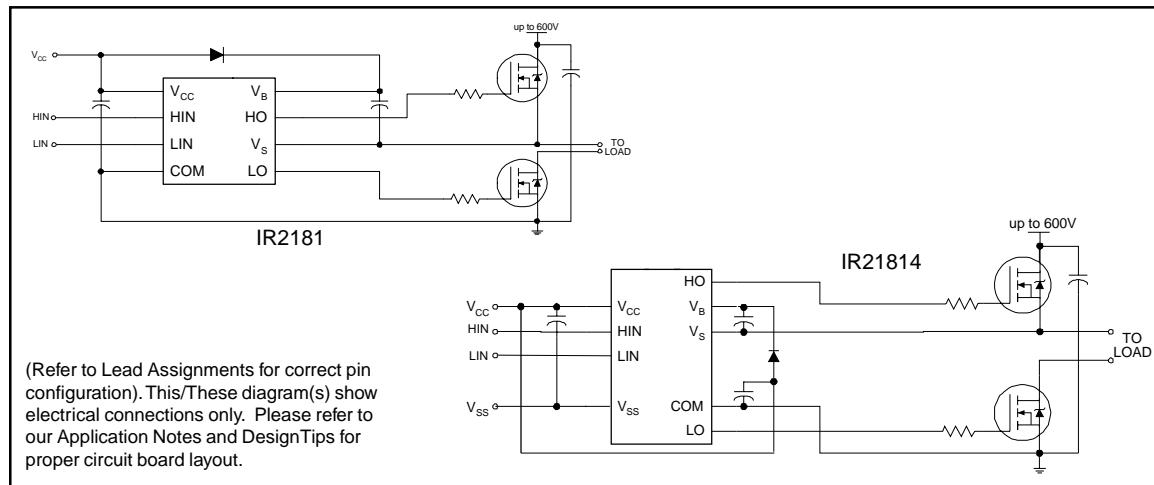
The IR2181(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard

IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/LIN	yes	Internal 500ns	COM	180/220 ns
21834			Program 0.4 ~ 5 us	VSS/COM	
2184	IN/SD	yes	Internal 500ns	COM	680/270 ns
21844			Program 0.4 ~ 5 us	VSS/COM	

CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Typical Connection



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating absolute voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	$V_{SS} - 0.3$	$V_{SS} + 10$	
V_{SS}	Logic ground (IR21814 only)	$V_{CC} - 25$	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	(8-lead PDIP)	—	1.0
		(8-lead SOIC)	—	0.625
		(14-lead PDIP)	—	1.6
		(14-lead SOIC)	—	1.0
R_{thJA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125
		(8-lead SOIC)	—	200
		(14-lead PDIP)	—	75
		(14-lead SOIC)	—	120
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-50	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN - IR2181/IR21814)	V_{SS}	$V_{SS} + 5$	
V_{SS}	Logic ground (IR21814/IR21824 only)	-5	5	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Note 2: HIN and LIN pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

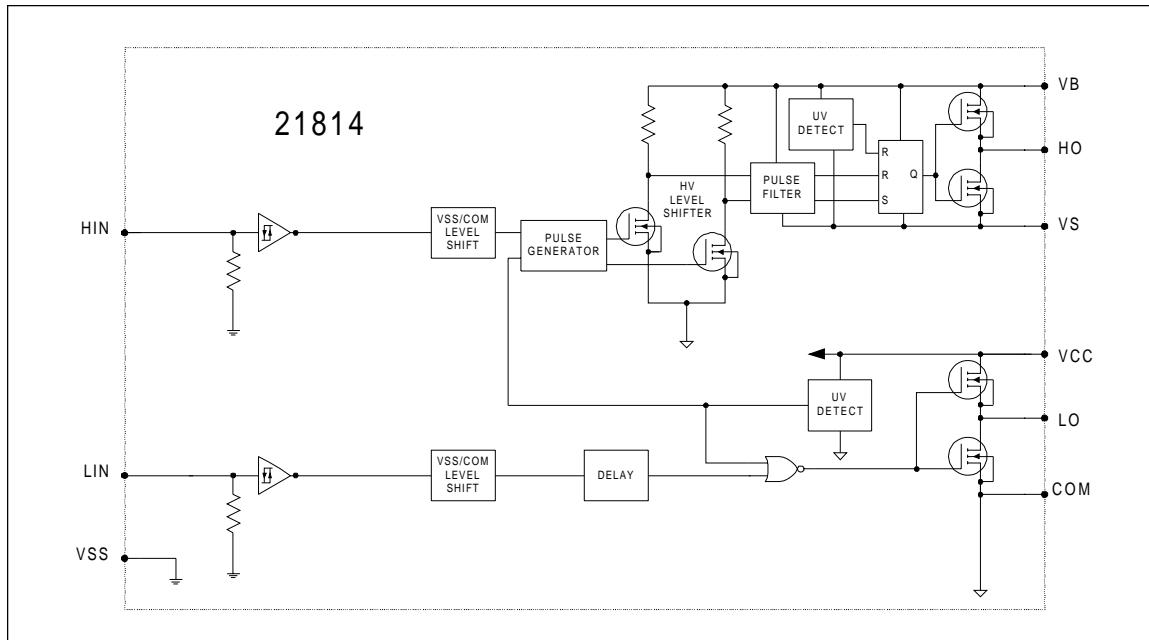
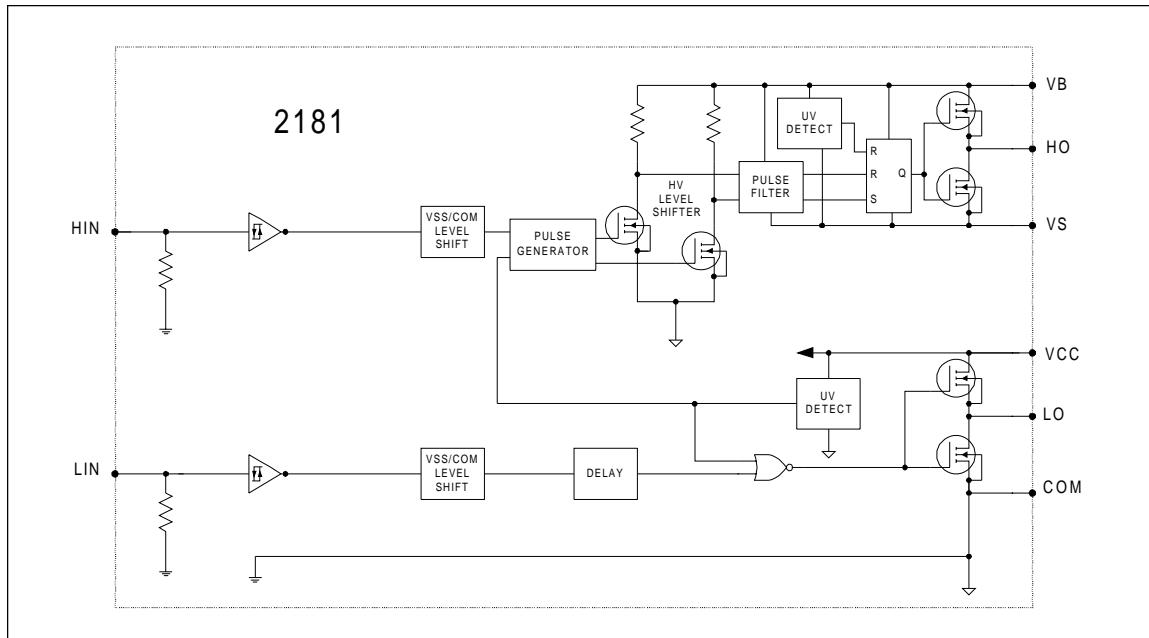
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t _{on}	Turn-on propagation delay	—	180	270	nsec	V _S = 0V
t _{off}	Turn-off propagation delay	—	220	330		V _S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	35		
t _r	Turn-on rise time	—	40	60		V _S = 0V
t _f	Turn-off fall time	—	20	35		V _S = 0V

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM and T_A = 25°C unless otherwise specified. The V_{IH}, V_{IL} and I_{IN} parameters are referenced to V_{SS}/COM and are applicable to the respective input leads HIN and LIN. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V _{IH}	Logic "1" input voltage (IR2181/IR21814)	2.7	—	—	V	V _{CC} = 10V to 20V
V _{IL}	Logic "0" input voltage (IR2181/IR21814)	—	—	0.8		V _{CC} = 10V to 20V
V _{OH}	High level output voltage, V _{BIAS} - V _O	—	—	1.2		I _O = 0A
V _{OL}	Low level output voltage, V _O	—	—	0.1		I _O = 0A
I _{LK}	Offset supply leakage current	—	—	50		V _B = V _S = 600V
I _{QBS}	Quiescent V _{BS} supply current	20	60	150	μA	V _{IN} = 0V or 5V
I _{QCC}	Quiescent V _{CC} supply current	50	120	240		V _{IN} = 0V or 5V
I _{IN+}	Logic "1" input bias current	—	25	60		V _{IN} = 5V
I _{IN-}	Logic "0" input bias current	—	—	1.0		V _{IN} = 0V
V _{CCUV+} V _{BSUV+}	V _{CC} and V _{BS} supply undervoltage positive going threshold	8.0	8.9	9.8		
V _{CCUV-} V _{BSUV-}	V _{CC} and V _{BS} supply undervoltage negative going threshold	7.4	8.2	9.0	V	
V _{CCUVH} V _{BSUVH}	Hysteresis	0.3	0.7	—		
I _{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V _O = 0V, PW ≤ 10 μs
I _{O-}	Output low short circuit pulsed current	1.8	2.3	—		V _O = 15V, PW ≤ 10 μs

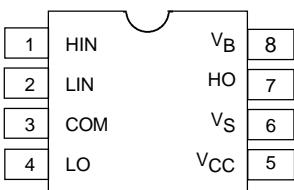
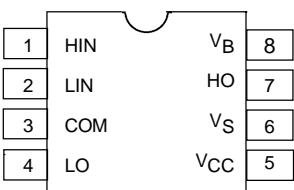
Functional Block Diagrams

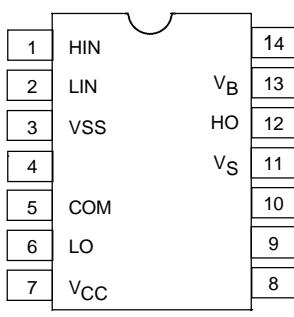
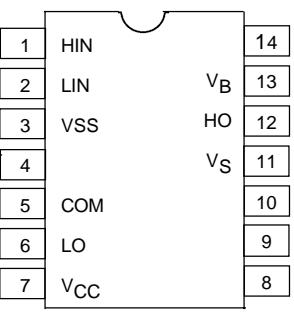


Lead Definitions

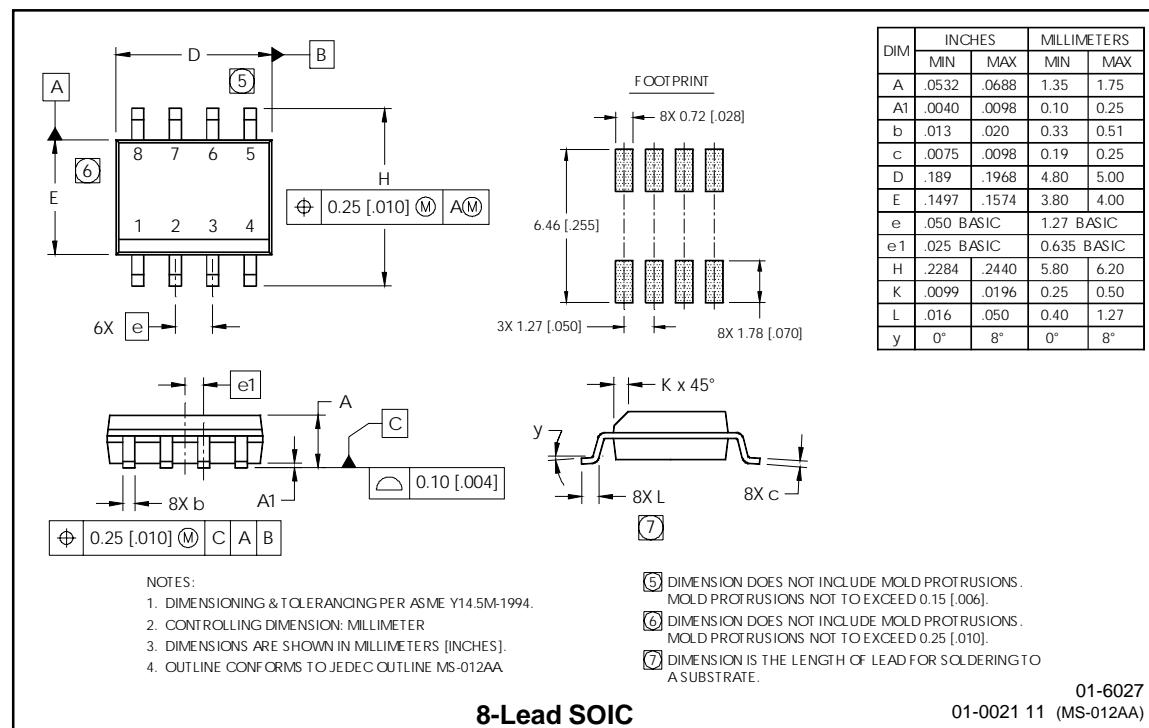
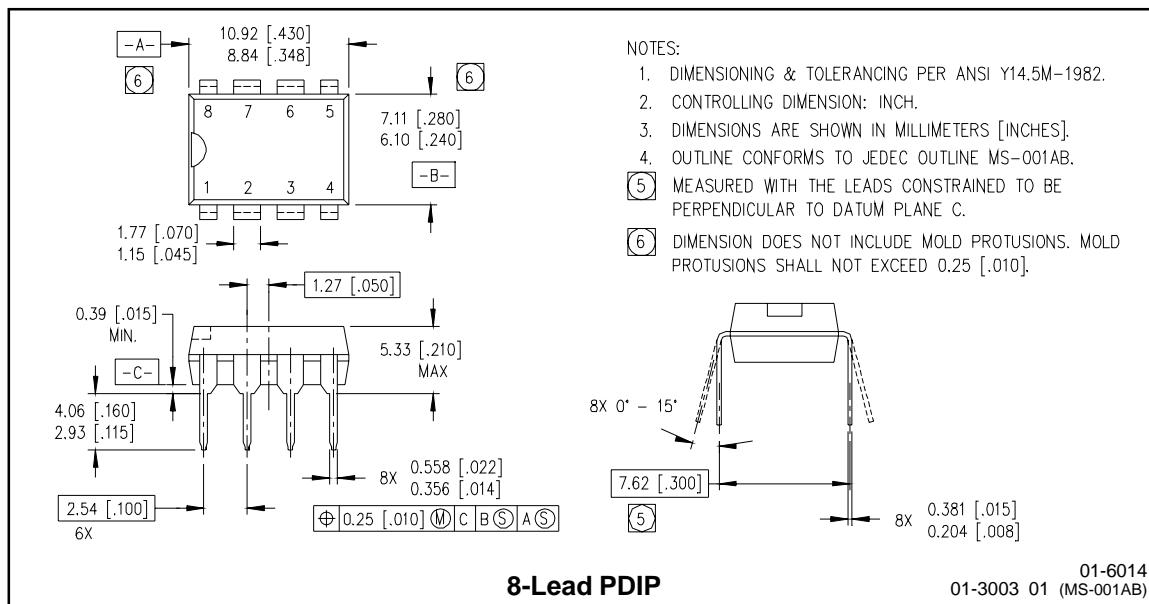
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase (IR2181/IR21814)
LIN	Logic input for low side gate driver output (LO), in phase (IR2181/IR21814)
VSS	Logic Ground (IR21814 only)
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

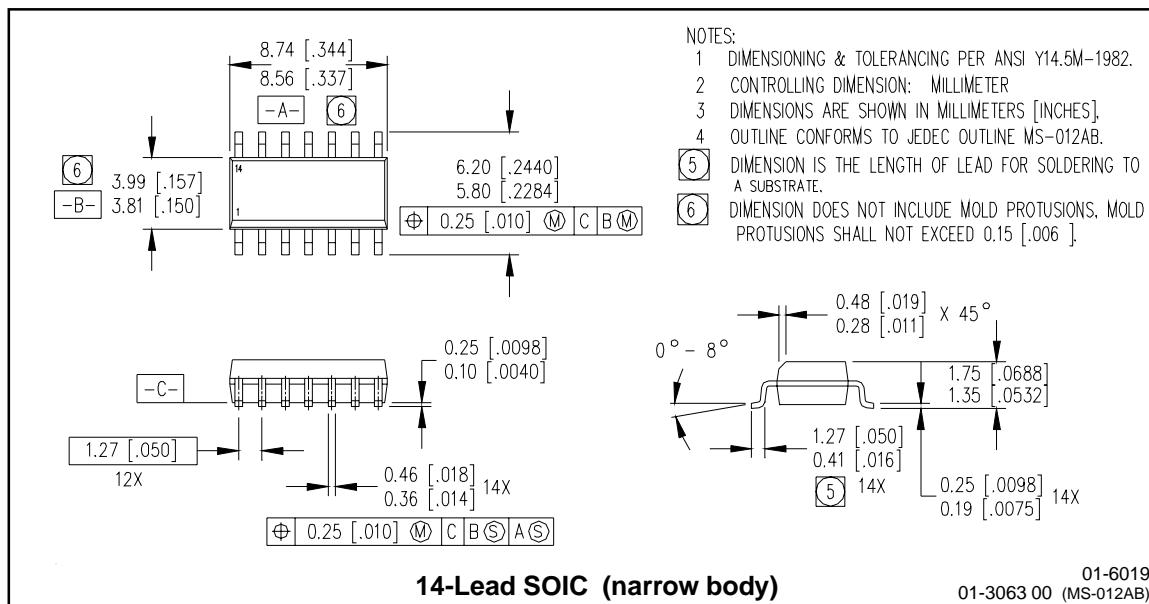
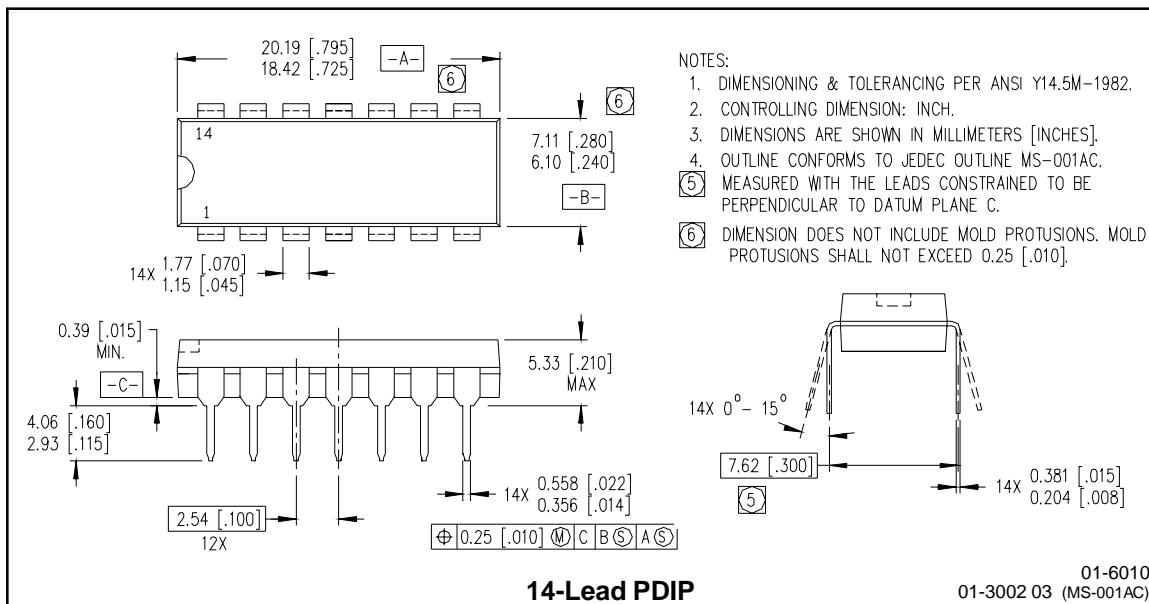
Lead Assignments

 <p>8-Lead PDIP</p>	 <p>8-Lead SOIC</p>
IR2181	IR2181S

 <p>14-Lead PDIP</p>	 <p>14-Lead SOIC</p>
IR21814	IR21814S

Case outlines





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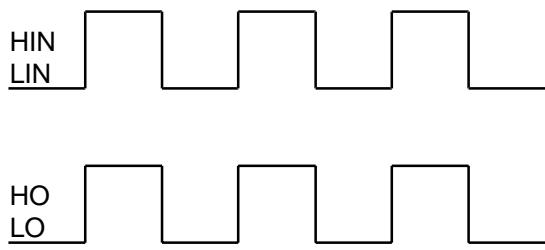


Figure 1. Input/Output Timing Diagram

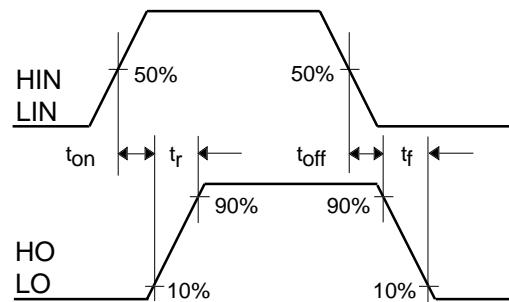


Figure 2. Switching Time Waveform Definitions

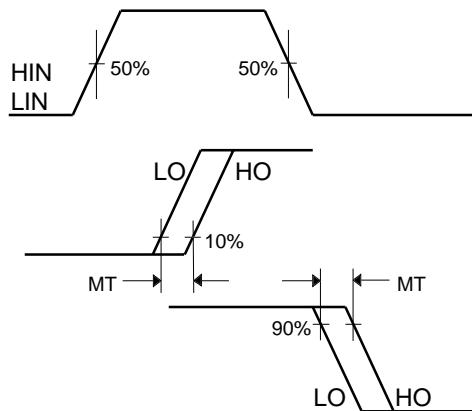


Figure 3. Delay Matching Waveform Definitions

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