International
IOR Rectifier

Data Sheet No. PD60107-P

IR2133(5) (J&S)
IR2233(5) (J&S)

3-PHASE BRIDGE DRIVER

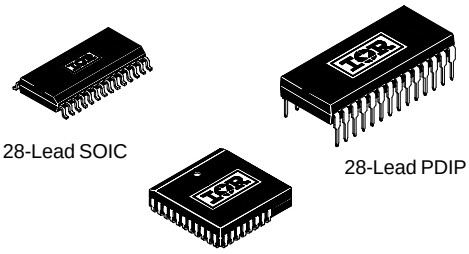
Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V or+1200V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10V/12V to 20V DC and up to 25V for transient
- Undervoltage lockout for all channels
- Over-current shut down turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs

Product Summary

V_{OFFSET}	600V or 1200V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V or 12 - 20V
$t_{on/off}$ (typ.)	750/700 ns
Deadtime (typ.)	250 ns

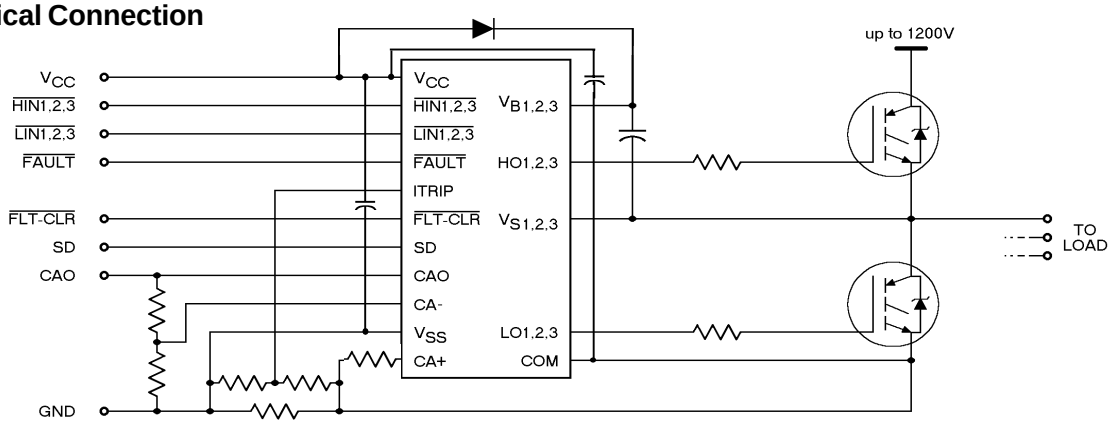
Packages



Description

The IR21333(5)/IR2233(5) (J)(S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. An independent operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also be derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain $\overline{\text{FAULT}}$ signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the $\overline{\text{FLT-CLR}}$ lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts or 1200 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only.
Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage (IR2133/IR2135)	-0.3	625	V
	(IR2233/IR2235)	-0.3	1225	
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$ - 0.3	$V_{B1,2,3}$ + 0.3	
V_{CC}	Fixed supply voltage	-0.3	25	
V_{SS}	Logic ground	V_{CC} - 25	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, SD & $\overline{FLT\text{-}CLR}$)	V_{SS} - 0.3	V_{SS} + 15	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS} - 0.3	V_{CC} + 0.3	
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS} - 0.3	V_{CC} + 0.3	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS} - 0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq 25^oC$ (28 Lead PDIP)	—	1.5	W
	(28 Lead SOIC)	—	1.6	
	(44 lead PLCC)	—	2.0	
Rth_{JA}	Thermal resistance, junction to ambient (28 Lead PDIP)	—	83	°C/W
	(28 Lead SOIC)	—	78	
	(44 lead PLCC)	—	63	
T_J	Junction temperature	—	125	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Min.	Max.	Units
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3}$ + 10/12	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High side floating supply offset voltage (IR2133/IR2135)	Note 1	600	
	(IR2233/IR2235)	Note 1	1200	
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Fixed supply voltage	10 or 12	20	
V_{SS}	Low side driver return	-5	5	
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, SD & $\overline{FLT\text{-}CLR}$)	V_{SS}	V_{SS} + 5	
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS}	V_{SS} + 5	
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS}	V_{SS} + 5	
V_{FLT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	

Note 1: Logic operational for V_S of COM - 5V to COM + 600V/1200V. Logic state held for V_S of COM -5V to COM -V_{BS}. (Please refer to the Design Tip DT97-3 for more details).
Note 2: All input pins, op amp input and output pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS}, T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	500	750	1000	ns	V_{IN} = 0 & 5V $V_{S1,2,3}$ = 0 to 600V or 1200V
t_{off}	Turn-off propagation delay	450	700	950		
t_r	Turn-on rise time	—	90	150		
t_f	Turn-off fall time	—	40	70		
t_{sd}	SD to output shutdown propagation delay	500	750	1000		V_{IN},V_{SD} = 0 & 5V
t_{itrip}	ITRIP to output shutdown propagation delay	600	850	1100		V_{IN},V_{ITRIP} = 0 & 5V
t_{bl}	ITRIP blanking time	—	400	—		ITRIP = 1V
t_{flt}	ITRIP to $\overline{FAULT}$ propagation delay	400	650	900		V_{IN},V_{ITRIP} = 0 & 5V
$t_{fil,in}$	Input filter time ($\overline{HIN}$, $\overline{LIN}$ and SD)	—	310	—		V_{IN} = 0 & 5V
t_{fltclr}	$\overline{FLT\text{-}CLR}$ to $\overline{FAULT}$ clear time	600	850	1100		V_{IN},V_{ITRIP} = 0 & 5V
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	100	250	400		V_{IN} = 0 & 5V
SR+	Amplifier slew rate (positive)	5	10	—	V/µs	
SR-	Amplifier slew rate (negative)	2	2.5	—		

NOTE: For high side PWM, HIN pulse width must be ≥ 1µ sec

Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V unless otherwise specified and T_A = 25°C. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ & $L_{S1,2,3}$). The VO and IO parameters are referenced to V_{SS} and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ or $L_{O1,2,3}$.

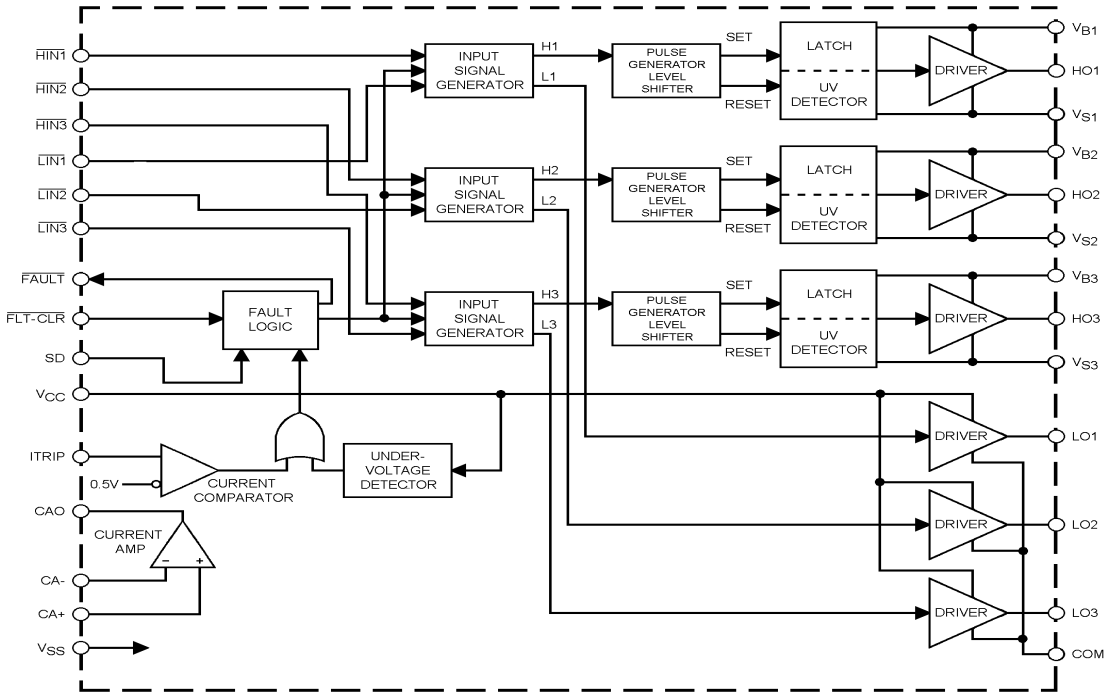
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
V_{SD,TH^+}	SD Input Positive Going Threshold	1.2	1.65	2.1		
V_{SD,TH^-}	SD Input Negative Going Threshold	0.9	1.35	1.8		
V_{IT,TH^+}	I_{ITRIP} Input Positive Going Threshold	420	520	620	mV	
V_{IT,TH^-}	I_{ITRIP} Input Negative Going Threshold	340	440	540		
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	—	—	100		V_{IN} = 0V, I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	—	—	100		V_{IN} = 5V, I_O = 0A
I_{LK}	Offset Supply Leakage Current (IR2133/IR2135)	—	—	50	µA	$V_{B1,2,3}$=$V_{S1,2,3}$ = 600V
	(IR2233/IR2235)	—	—	50		$V_{B1,2,3}$=$V_{S1,2,3}$ = 1200V
I_{QBS}	Quiescent V_{BS} Supply Current	—	50	100		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	4	8	mA	V_{IN} = 0V or 5V
I_{IN^+}	Logic "1" Input Bias Current (OUT = HI)	—	200	350	µA	V_{IN} = 0V
I_{IN^-}	Logic "0" Input Bias Current (OUT = LO)	—	100	250		V_{IN} = 5V
I_{SD^+}	"High" Shutdown Bias Current	—	30	100		SD = 5V
I_{SD^-}	"Low" Shutdown Bias Current	—	—	100	nA	SD = 0V
I_{ITRIP^+}	"High" I_{ITRIP} Bias Current	—	30	100	µA	I_{ITRIP} = 5V
I_{ITRIP^-}	"Low" I_{ITRIP} Bias Current	—	—	100	nA	I_{ITRIP} = 0V

Static Electrical Characteristics — Continued

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to V_{SS} and $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
$I_{FLTCLR+}$	"High" Fault Clear Input Bias Current	—	200	350	µA	$\overline{\text{FLT-CLR}}$ = 0V
$I_{FLTCLR-}$	"Low" Fault Clear Input Bias Current	—	100	250		$\overline{\text{FLT-CLR}}$ = 5V
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold				V	
	(for IR2133/IR2233)	7.6	8.6	9.6		
	(for IR2135/IR2235)	9.2	10.4	11.6		
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold					
	(for IR2133/IR2233)	7.2	8.2	9.2		
	(for IR2135/IR2235)	8.3	9.4	10.5		
V_{BSUVH}	V_{BS} Supply Undervoltage Lockout Hysteresis					
	(for IR2133/IR2233)	—	0.4	—		
	(for IR2135/IR2235)	—	1	—		
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold					
	(for IR2133/IR2233)	7.6	8.6	9.6		
	(for IR2135/IR2235)	9.2	10.4	11.6		
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold					
	(for IR2133/IR2233)	7.2	8.2	9.2		
	(for IR2135/IR2235)	8.3	9.4	10.5		
V_{CCUVH}	V_{CC} Supply Undervoltage Lockout Hysteresis					
	(for IR2133/IR2233)	—	0.4	—		
	(for IR2135/IR2235)	—	1	—		
$R_{on,FLT}$	FAULT- Low On Resistance	—	70	100	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	190	250	—	mA	V_{OUT} = 0V, V_{IN} = 0V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	380	500	—		V_{OUT} = 15V, V_{IN} = 5V PW ≤ 10 µs
V_{OS}	Amplifier Input Offset Voltage	—	0	30	mV	CA+=0.2V, CA-=CAO
$I_{IN,AMP}$	Amplifier Input Bias Current	—	—	4	nA	CA+ = CA- = 2.5V
CMRR	Amplifier Common Mode Rejection Ratio	50	70	—	dB	CA+ = 0.1V & 5V, CA- = CAO
PSRR	Amplifier Power Supply Rejection Ratio	50	70	—		CA+=0.2V, CA-=CAO V_{CC} = 10V & 20V
$V_{OH,Amp}$	Amplifier High Level Output Voltage	5	5.2	5.4	V	CA+ = 1V, CA- = 0V
$V_{OL,Amp}$	Amplifier Low Level Output Voltage	—	—	20	mV	CA+ = 0V, CA- = 1V
$I_{SRC,Amp}$	Amplifier Output Source Current	4	7	—	mA	CA+ = 1V, CA- = 0V, CAO = 4V
$I_{SNK,Amp}$	Amplifier Output Sink Current	0.5	1	—		CA+ = 0V, CA- = 1V, CAO = 2V
$I_{O+,Amp}$	Amplifier Output High Short Circuit Current	—	10	—		CA+ = 5V, CA- = 0V, CAO = 0V
$I_{O-,Amp}$	Amplifier Output Low Short Circuit Current	—	4	—		CA+ = 0V, CA- = 5V, CAO = 5V

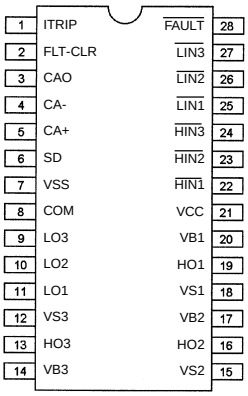
Functional Block Diagram



Lead Definitions

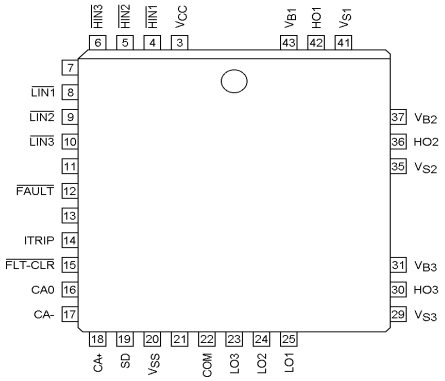
Symbol	Lead Description
$\overline{\text{HIN1,2,3}}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase.
$\overline{\text{LIN1,2,3}}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase.
$\overline{\text{FAULT}}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic.
V_{CC}	Logic and low side fixed supply.
ITRIP	Input for over-current shut down.
$\overline{\text{FLT-CLR}}$	Logic input for fault clear, negative logic.
SD	Logic input for shut down.
CAO	Output of current amplifier.
CA-	Negative input of current amplifier.
CA+	Positive input of current amplifier.
V_{SS}	Logic ground.
COM	Low side return.
$V_{B1,2,3}$	High side floating supplies.
HO1,2,3	High side gate drive outputs.
$V_{S1,2,3}$	High side floating supply returns.
LO1,2,3	Low side gate drive outputs

Lead Assignments



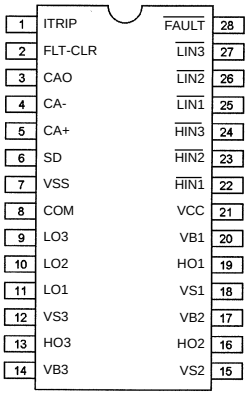
28 Lead DIP

IR2133
IR2135
IR2233
IR2235



44 Lead PLCC w/o 12 Leads

IR2133J
IR2135J
IR2233J
IR2235J



28 Lead SOIC (Wide Body)

IR2133S
IR2135S
IR2233S
IR2235S

Part Number

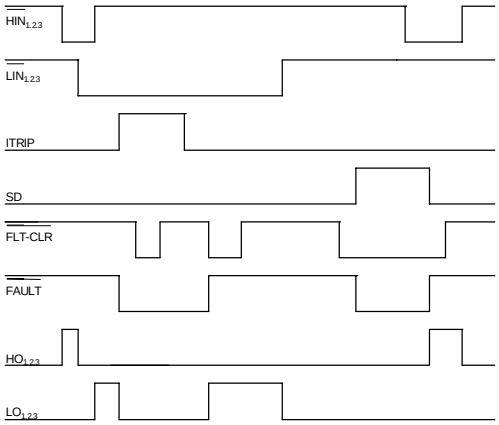


Figure 1. Input/Output Timing Diagram

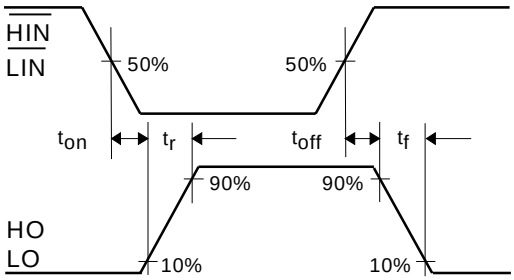


Figure 2. Switching Time Waveform Definitions

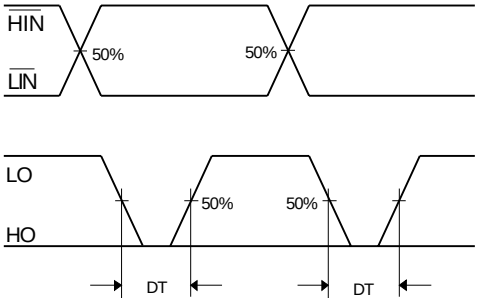


Figure 3. Deadtime Waveform Definitions

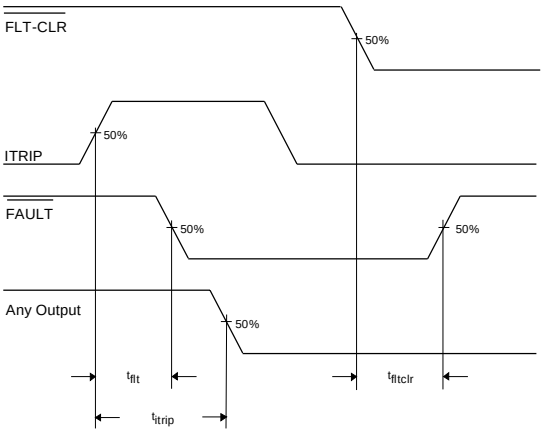


Figure 4. Overcurrent Shutdown Waveform

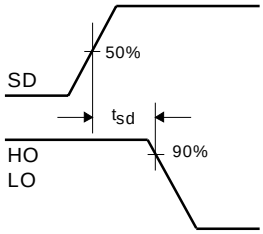


Figure 5. Shutdown Waveform Definitions

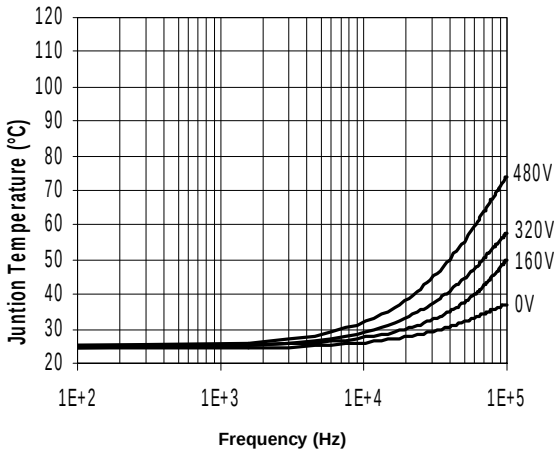


Figure 7. IR2133J Junction Temperature vs Frequency Driving (IRGPC20KD2) Rgate = 5.1Ω @ Vcc = 15V

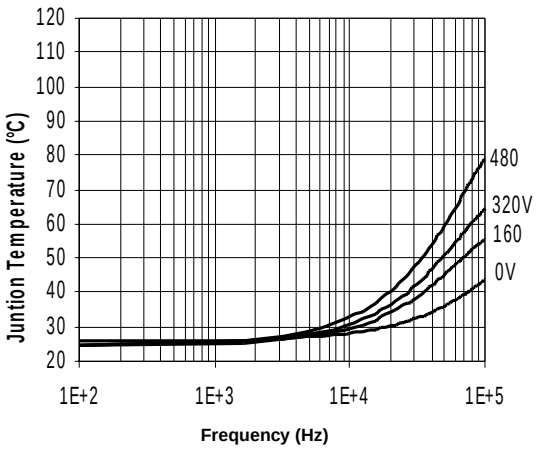


Figure 8. IR2133J Junction Temperature vs Frequency Driving (IRGPC30KD2) Rgate = 5.1Ω @ Vcc = 15V

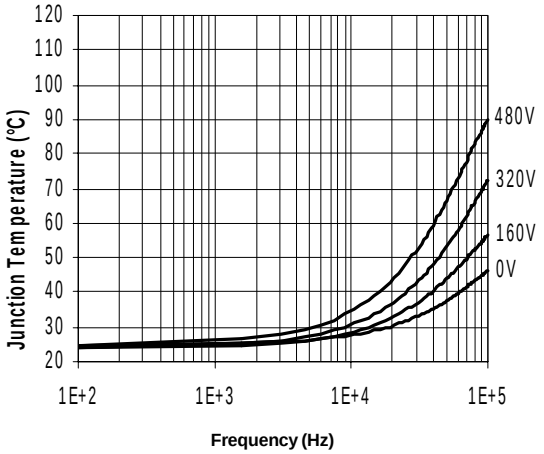


Figure 9. IR2133J Junction Temperature vs Frequency Driving (IRGPC40KD2) Rgate = 5.1Ω @ Vcc = 15V

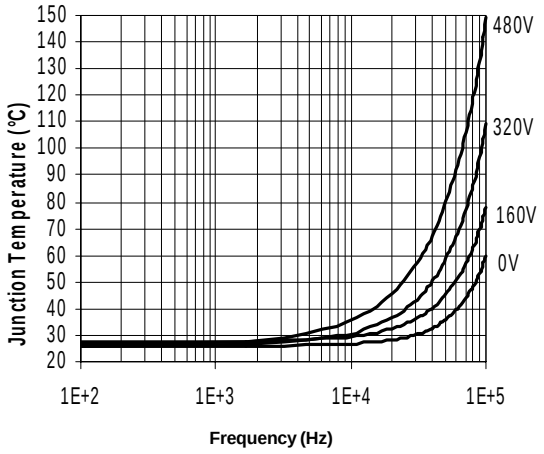


Figure 10. IR2133J Junction Temperature vs Frequency Driving (IRGPC50KD2) Rgate = 5.1Ω @ Vcc = 15V

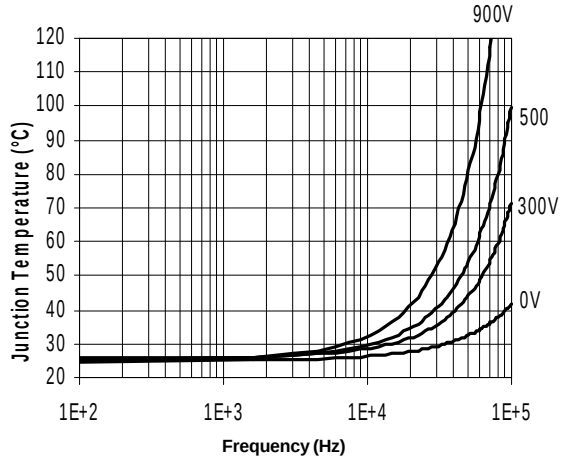


Figure 11. IR2233J Junction Temperature vs Frequency Driving (IRG4PH30KD) Rgate = 20Ω @ Vcc = 15V

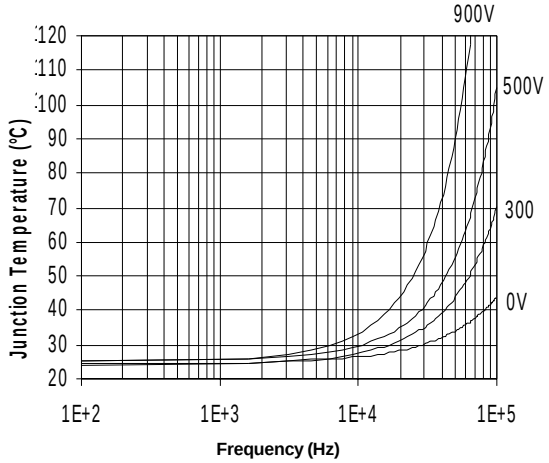


Figure 12. IR2233J Junction Temperature vs Frequency Driving (IRG4PH40KD) Rgate = 15Ω @ Vcc = 15V

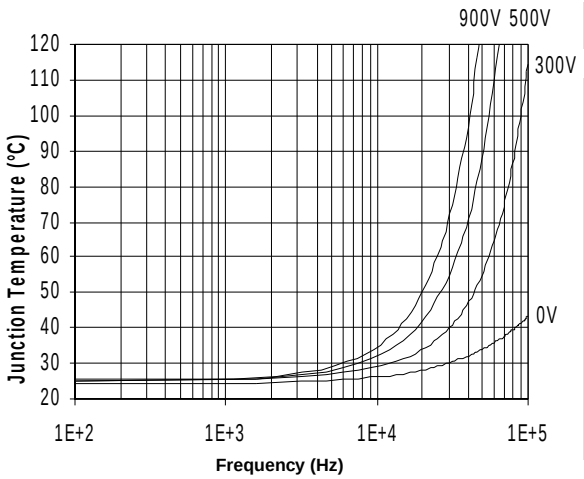


Figure 13. IR2233J Junction Temperature vs Frequency Driving (IRG4PH50KD) Rgate = 10Ω @ Vcc = 15V

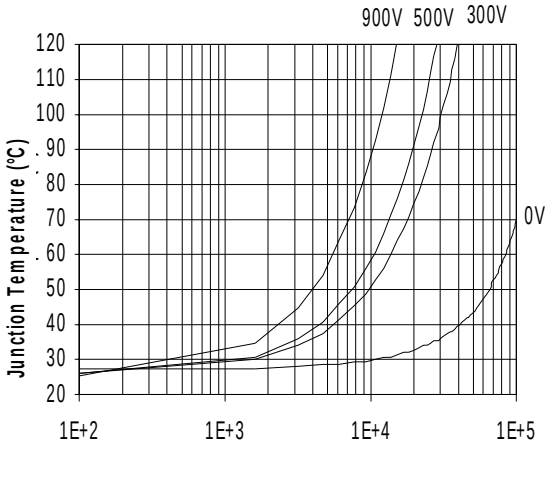
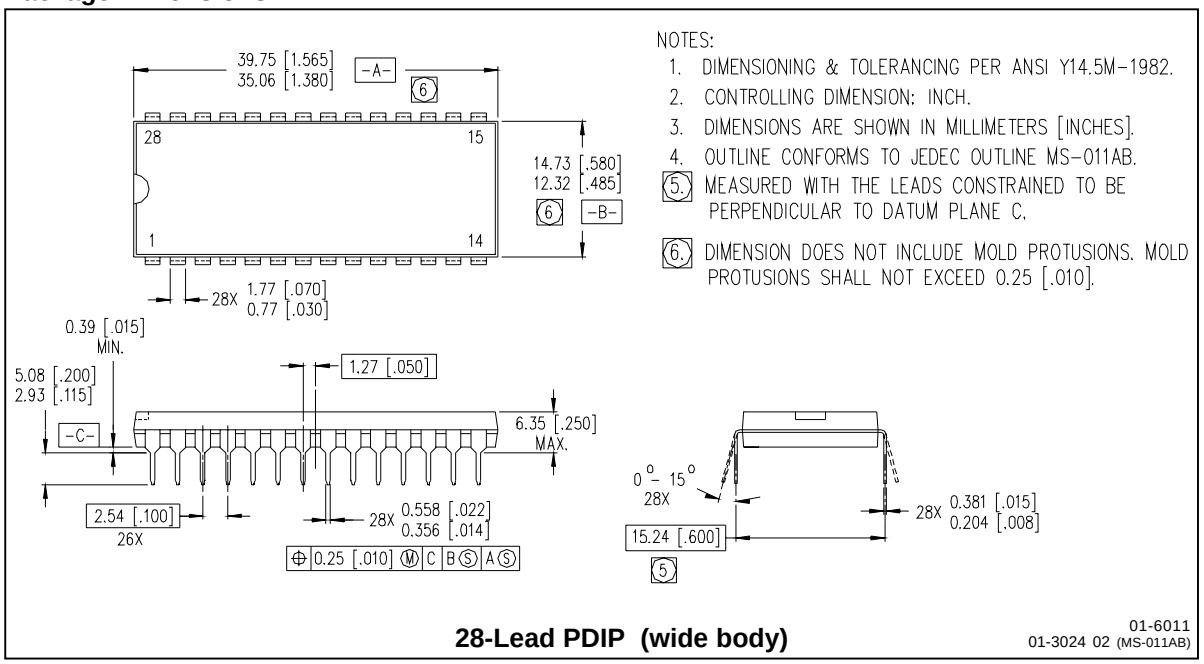
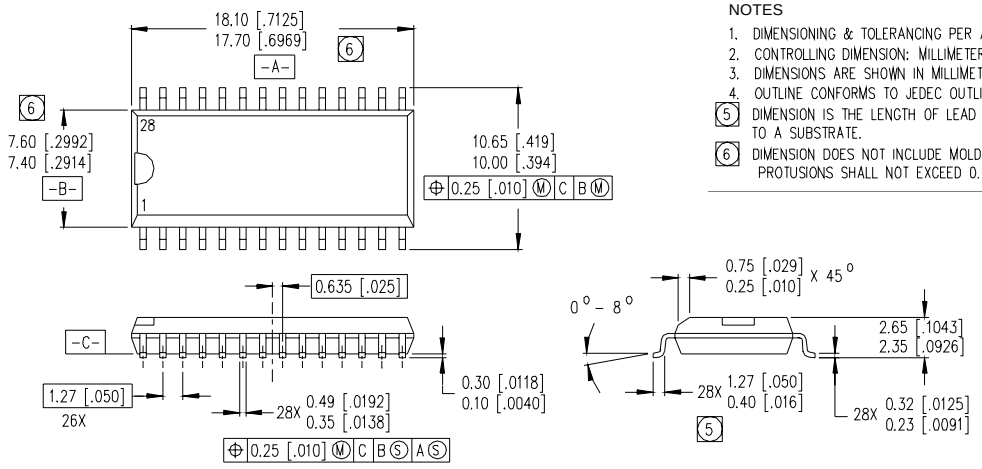


Figure 14. IR2133J Junction Temperature vs Frequency Driving (IRG4ZH71KD) Rgate = 5Ω @ Vcc = 15V

Package Dimensions



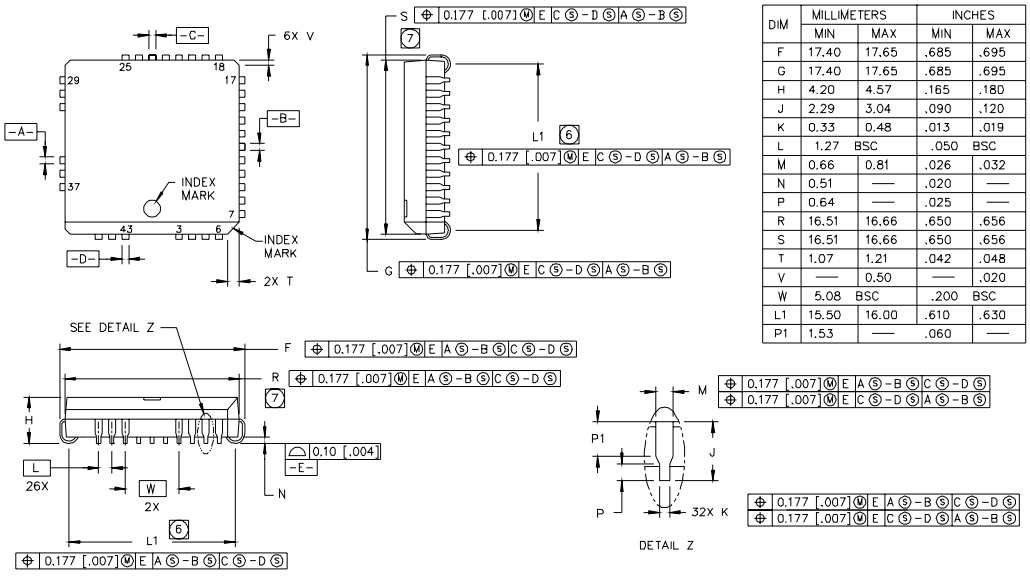


NOTES

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F	17.40	17.65	.685	.695
G	17.40	17.65	.685	.695
H	4.20	4.57	.165	.180
J	2.29	3.04	.090	.120
K	0.33	0.48	.013	.019
L	1.27 BSC		.050 BSC	
M	0.66	0.81	.026	.032
N	0.51	—	.020	—
P	0.64	—	.025	—
R	16.51	16.66	.650	.656
S	16.51	16.66	.650	.656
T	1.07	1.21	.042	.048
V	—	0.50	—	.020
W	5.08 BSC		.200 BSC	
L1	15.50	16.00	.610	.630
P1	1.53	—	.060	—

NOTES:

1. DIMENSIONING & TOLERENCING PER ANSI Y14.5M-1982.
2. DIMENSIONS SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE MS-018AC.
5. DATUMS -A-, -B-, -C-, & -D- ARE DETERMINED BY WHERE THE TOP OF THE LEADS EXIT PLASTIC BODY AT MOLD PARTING LINE.
6. TO BE MEASURED AT -E- SEATING PLANE.
7. DIMENSIONS DO NOT INCLUDE MOLD FLASH, ALLOWABLE FLASH IS 0.254 [.010].

44-Lead PLCC w/o 12 leads

01-6009 00
01-3004 02(mod.) (MS-018AC)

8/17/2001