

#### February 2002

# Single Event and Total Dose Hardened, High-Speed, Dual Output PWM

inter<sub>sil</sub>

The single event and total dose hardened IS-1825ASRH pulse width modulator is designed to be used in high frequency, switching power supplies in either voltage or current-mode configurations. The design includes a precision voltage reference, a low power start-up circuit, a high frequency oscillator, a wide-band error amplifier and a fast current-limit comparator. The use of proprietary process capabilities and unique design techniques results in fast propagation delay times and high output current over a wide range of output voltages.

Constructed with the Intersil Rad-hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide a high level of immunity to single event transients. All specified parameters are guaranteed and tested for 300krad(Si) total dose performance.

Detailed Electrical Specifications for these devices are contained in SMD 5962-02511. A "hot-link" is provided on our website for downloading the SMD.

## Pinout





### Features

- Electrically Screened to DSCC SMD # 5962-02511
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment

-	Total Dose	300krad(SI) (	(max)

- Latch-up Immune ..... Dielectrically Isolated
- SEU immune ..... LET=35MeV/mg/cm<sup>2</sup>(max)
- Oscillator Frequency ......1MHz(max)

- Undervoltage Lockout
  - Start Threshold ......8.8V(max)
- Improved Soft-Start Function Compared with Commercial 1825A Types
- Trimmed Oscillator Discharge Current
- Pulse-by-Pulse Current Limiting
- Latched Overcurrent Comparator with Full Cycle Restart
- Programmable Leading Edge Blanking

# Applications

- Voltage or Current-Mode Switching Power Supplies
- Control of High Current MOSFET Drivers
- Motor Speed and Direction Control

# **Ordering Information**

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE ( <sup>O</sup> C)
5962F0251101QEC	IS1-1825ASRH-8	-50 to 125
5962F0251101QXC	IS9-1825ASRH-8	-50 to 125
5962F0251101VEC	IS1-1825ASRH-Q	-50 to 125
5962F0251101VXC	IS9-1825ASRH-Q	-50 to 125
IS1-1825ASRH/Proto	IS1-1825ASRH/Proto	-50 to 125
IS9-1825ASRH/Proto	IS9-1825ASRH/Proto	-50 to 125

# **Die Characteristics**

#### DIE DIMENSIONS:

4310µm x 5840µm (170 mils x 230 mils) Thickness: 483µm  $\pm$  25.4µm (19 mils  $\pm$  1 mil)

#### INTERFACE MATERIALS

#### Glassivation

Type: Phosphorus Silicon Glass (PSG) Thickness: 8.0kA +/- 1.0kA

#### **Top Metallization**

Type: AlSiCu Thickness: 16.0kA +/- 2kA

#### Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

#### **Backside Finish:**

Silicon

#### ASSEMBLY RELATED INFORMATION

Substrate Potential: Unbiased (DI)

#### ADDITIONAL INFORMATION

# Worst Case Current Density: $<2.0 \times 10^5 \text{ A/cm}^2$

#### Transistor Count:

585



IS-1825ASRH

1. Both the OGND (oscillator ground) and the GND (control circuit ground) pads must be bonded to ground. These pads are both bonded to the GND pin on the packaged devices.

2. All double-sized bond pads must be double bonded for current sharing purposes.

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# Metallization Mask Layout