INTRODUCTION

KS0074 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology.
It can display 1, 2, or 4 lines with 5 × 8 or 6 × 8 dots format.

FUNCTIONS

- Character type dot matrix LCD driver & controller
- Internal driver : 34 common and 80 segment signal output
- Easy interface with 4-bit or 8-bit MPU
- Clock synchronized serial Interface
- 5 × 8 dot matrix possible
- 6 × 8 dot matrix possible
- Bi-directional shift function
- All character reverse display
- Display shift per line
- Voltage converter for LCD drive voltage : 13 V max (2 times / 3 times)
- Various instruction functions
- Automatic power on reset

FEATURES

- Internal Memory
  - Character Generator ROM (CGROM) : 9,600 bits (240 characters × 5 × 8 dot)
  - Character Generator RAM (CGRAM) : 64 × 8 bits (8 characters × 5 × 8 dot)
  - Segment Icon RAM (SEGRAM) : 16 × 8 bits (96 icons max.)
  - Display Data RAM (DDRAM) : 80 × 8 bits (80 characters max.)
- Low power operation
  - Power supply voltage range : 2.7 - 5.5 V (VDD)
  - LCD Drive voltage range : 3.0 - 13.0 V (VDD - V5)
- CMOS process
- Programmable duty cycle : 1/17, 1/33 (refer to Table 1.)
- Internal oscillator with an external resistor
- Low power consumption
- Bare chip available

Table 1. Programmable duty cycles

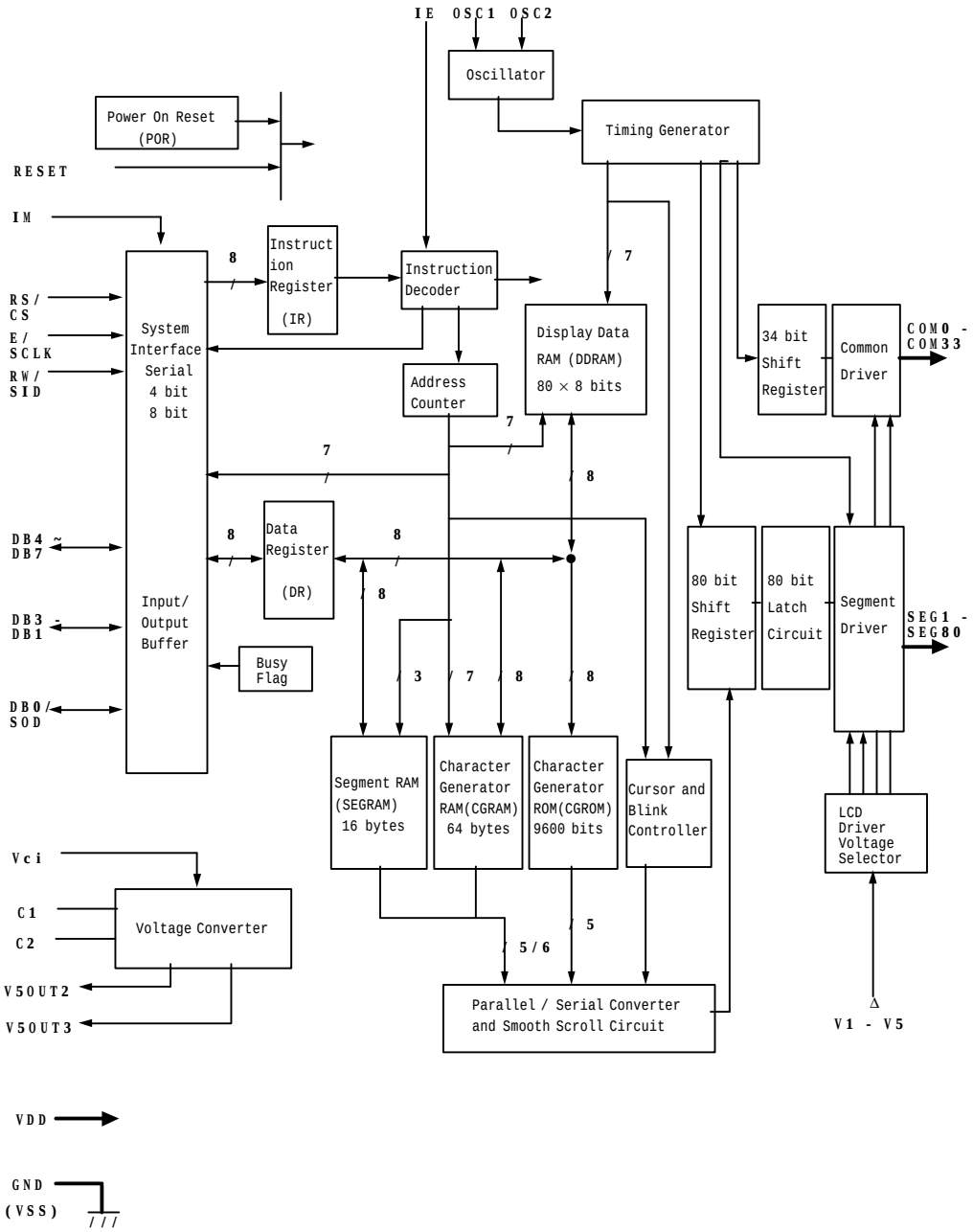
5-dot font width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable characters	Possible icons
1	1/17	1 line of 32 characters	80
2	1/33	2 lines of 32 characters	80
4	1/33	4 lines of 16 characters	80

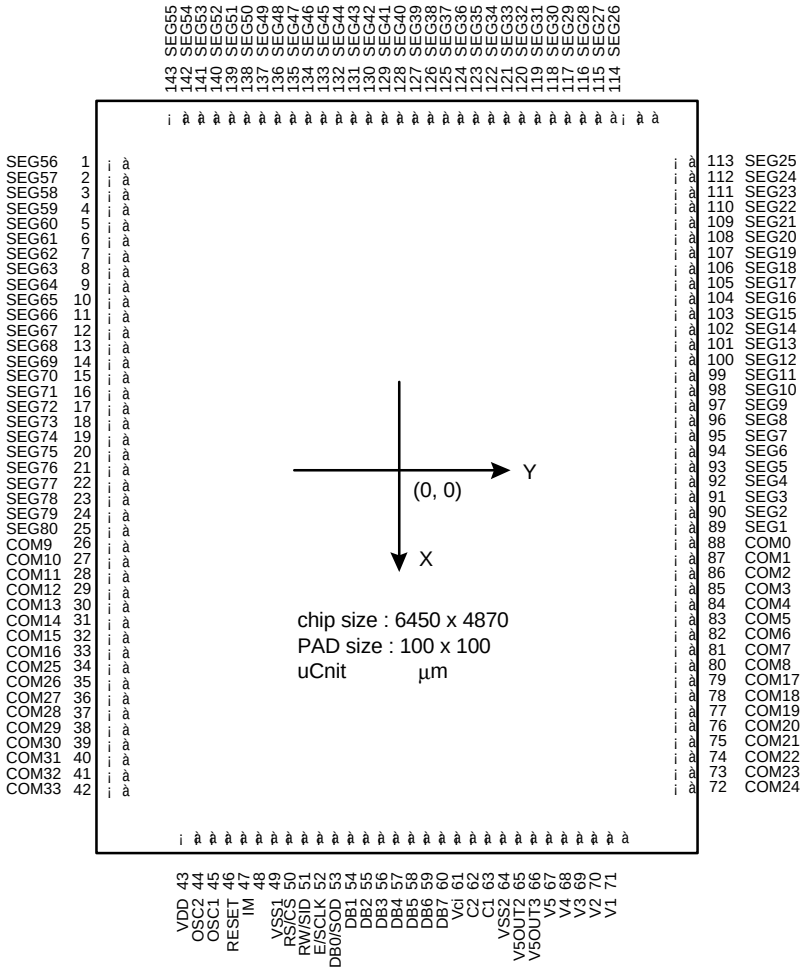
6-dot font width

Display Line Numbers	Duty Ratio	Single-chip Operation	
		Displayable characters	Possible icons
1	1/17	1 line of 26 characters	78
2	1/33	2 lines of 26 characters	78
4	1/33	4 lines of 13 characters	78

BLOCK DIAGRAM



PAD CONFIGURATION



PAD LOCATION [UNIT: μm]

PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y	PAD NUMBER	PAD NAME	COORDINATE X	COORDINATE Y
1	SEG56	-2475	-2269	49	VSS1	3059	-1028	97	SEG9	-475	2269
2	SEG57	-2350	-2269	50	RS/CS	3059	-903	98	SEG10	-600	2269
3	SEG58	-2225	-2269	51	RW/SID	3059	-778	99	SEG11	-725	2269
4	SEG59	-2100	-2269	52	E/SCLK	3059	-653	100	SEG12	-850	2269
5	SEG60	-1975	-2269	53	DB0/SOD	3059	-528	101	SEG13	-975	2269
6	SEG61	-1850	-2269	54	DB1	3059	-403	102	SEG14	-1100	2269
7	SEG62	-1725	-2269	55	DB2	3059	-278	103	SEG15	-1225	2269
8	SEG63	-1600	-2269	56	DB3	3059	-153	104	SEG16	-1350	2269
9	SEG64	-1475	-2269	57	DB4	3059	-28	105	SEG17	-1475	2269
10	SEG65	-1350	-2269	58	DB5	3059	97	106	SEG18	-1600	2269
11	SEG66	-1225	-2269	59	DB6	3059	222	107	SEG19	-1725	2269
12	SEG67	-1100	-2269	60	DB7	3059	347	108	SEG20	-1850	2269
13	SEG68	-975	-2269	61	Vci	3059	472	109	SEG21	-1975	2269
14	SEG69	-850	-2269	62	C2	3059	597	110	SEG22	-2100	2269
15	SEG70	-725	-2269	63	C1	3059	722	111	SEG23	-2225	2269
16	SEG71	-600	-2269	64	VSS2	3059	847	112	SEG24	-2350	2269
17	SEG72	-475	-2269	65	V5OUT2	3059	972	113	SEG25	-2475	2269
18	SEG73	-350	-2269	66	V5OUT3	3059	1097	114	SEG26	-3059	1812
19	SEG74	-225	-2269	67	V5	3059	1222	115	SEG27	-3059	1687
20	SEG75	-100	-2269	68	V4	3059	1347	116	SEG28	-3059	1562
21	SEG76	24	-2269	69	V3	3059	1472	117	SEG29	-3059	1437
22	SEG77	149	-2269	70	V2	3059	1597	118	SEG30	-3059	1312
23	SEG78	274	-2269	71	V1	3059	1722	119	SEG31	-3059	1187
24	SEG79	399	-2269	72	COM24	2762	2269	120	SEG32	-3059	1062
25	SEG80	524	-2269	73	COM23	2637	2269	121	SEG33	-3059	937
26	COM9	762	-2269	74	COM22	2512	2269	122	SEG34	-3059	812
27	COM10	887	-2269	75	COM21	2387	2269	123	SEG35	-3059	687
28	COM11	1012	-2269	76	COM20	2262	2269	124	SEG36	-3059	562
29	COM12	1137	-2269	77	COM19	2137	2269	125	SEG37	-3059	437
30	COM13	1262	-2269	78	COM18	2012	2269	126	SEG38	-3059	312
31	COM14	1387	-2269	79	COM17	1887	2269	127	SEG39	-3059	187
32	COM15	1512	-2269	80	COM8	1762	2269	128	SEG40	-3059	62
33	COM16	1637	-2269	81	COM7	1637	2269	129	SEG41	-3059	-62
34	COM25	1762	-2269	82	COM6	1512	2269	130	SEG42	-3059	-187
35	COM26	1887	-2269	83	COM5	1387	2269	131	SEG43	-3059	-312
36	COM27	2012	-2269	84	COM4	1262	2269	132	SEG44	-3059	-437
37	COM28	2137	-2269	85	COM3	1137	2269	133	SEG45	-3059	-562
38	COM29	2262	-2269	86	COM2	1012	2269	134	SEG46	-3059	-687
39	COM30	2387	-2269	87	COM1	887	2269	135	SEG47	-3059	-812
40	COM31	2512	-2269	88	COM0	762	2269	136	SEG48	-3059	-937
41	COM32	2637	-2269	89	SEG1	524	2269	137	SEG49	-3059	-1062
42	COM33	2762	-2269	90	SEG2	399	2269	138	SEG50	-3059	-1187
43	VDD	3059	-1778	91	SEG3	274	2269	139	SEG51	-3059	-1312
44	OSC2	3059	-1653	92	SEG4	149	2269	140	SEG52	-3059	-1437
45	OSC1	3059	-1528	93	SEG5	24	2269	141	SEG53	-3059	-1562
46	RESET	3059	-1403	94	SEG6	-100	2269	142	SEG54	-3059	-1687
47	IM	3059	-1278	95	SEG7	-225	2269	143	SEG55	-3059	-1812
48	IE	3059	-1153	96	SEG8	-350	2269				

* "KS0074" Marking : easy to find the PAD No.107

PAD DESCRIPTION

PAD (NO)	INPUT/ OUTPUT	NAME	DESCRIPTION	INTERFACE
VDD (43)	-	Power supply	for logical circuit(+3V,+5V)	Power supply
VSS1,VSS2 (49,64)			0V(GND)	
V1-V5 (71-67)			Bias voltage level for LCD driving.	
Vci (61)	Input		Input voltage to the voltage converter to generate LCD drive voltage(Vci = 1.0 -4.5V).	
SEG1-SEG80 (89-143, (1-25)	Output	Segment output	Segment signal output for LCD drive.	LCD
COM0-COM33 (72-88, 26-42)	Output	Common output	Common signal output for LCD drive.	LCD
OSC1,OSC2 (45,44)	Input (OSC1), Output (OSC2)	Oscillator	When use internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1.	External resistor/oscillator (OSC1)
C1,C2 (63,62)	Input	External capacitance input	To use the voltage converter(2 times /3 times), these pins must be connected to the external capacitance.	External capacitance
RESET (46)	Input	Reset pin	Initialized to Low	-
IE (48)	Input	Select pin of instruction set	When IE = "High", Instruction set is selected as Table 6. When IE = "Low", Instruction set is selected as Table 10.	-
V5OUT2(65)	Output	Two times converter output	The value of Vci is converted two times. To use three times converter, the same capacitance as that of C1-C2 should be connected here.	V5 capacitance
V5OUT3(66)		Three times converter output	The value of Vci is converted three times.	V5

PAD DESCRIPTION (continued)

PAD (NO)	INPUT/ OUTPUT	NAME	DESCRIPTION	INTERFACE
IM (47)	Input	Interface mode selection	Select Interface mode with the MPU. When IM = "Low" : Serial mode, When IM = "High" : 4-bit/8-bit bus mode.	-
RS/CS (50)	Input	Register select/ Chip select	In bus mode, used as register selection input. When RS/CS = "High", Data register is selected. When RS/CS = "Low", Instruction register is selected. In serial mode, used as chip selection input. When RS/CS = "Low", selected. When RS/CS = "High", not selected.(Low access enable)	MPU
RW/SID (51)	Input	Read_write/Serial input data	In bus mode, used as read/write selection input. When RW/SID = "High", read operation. When RW/SID = "Low", write operation. In serial mode, used for data input pin.	MPU
E/SCLK (49)	Input	Read_write enable/Serial clock	In bus mode, used as read_write enable signal. In serial mode, used as serial clock input pin.	MPU
DB0/SOD (53)	Input_Output /Output	Data bus 0 bit/Serial output data	In 8-bit bus mode, used as lowest bi-directional data bit. During 4-bit bus mode, Open this pin. In serial mode, used as serial data output pin. If not in read operation, open this pin.	MPU
DB1-DB3 (54 - 56)	Input. Output	Data bus 1 - 7	In 8-bit bus mode, used as low order bi-directional data bus. During 4-bit bus mode or serial mode, open these pins.	MPU
DB4-DB7 (57 - 60)			In 8-bit bus mode, used as high order bi-directional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. During serial mode, open these pins.	MPU

FUNCTION DESCRIPTION

System Interface

This chip has all three kinds interface type with MPU : serial, 4-bit bus and 8-bit bus. Serial and bus(4-bit/8-bit) is selected by IM input, and 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically.
Hence, after MPU reads DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS/CS input pin in 4-bit/8-bit bus mode(IM = "High") or RS bit in serial mode(IM = "Low").

Table 2. Various kinds of operations according to RS and R/W bits.

RS	R/W	Operation
0	0	Instruction Write operation (MPU writes Instruction code into IR)
0	1	Read Busy flag(DB7) and address counter (DB0 - DB6)
1	0	Data Write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data from DR)

Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High(Read Instruction Operation), through DB7 port.
Before executing the next instruction, be sure that BF is not High.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters).
DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Fig-1.)

Fig-1. DDRAM Address

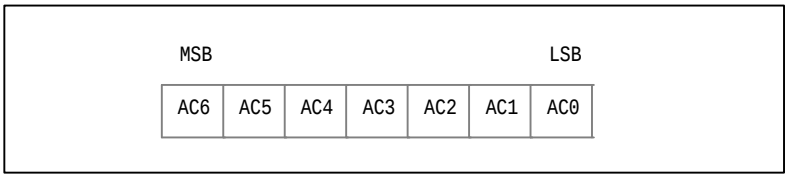


Fig-1. DDRAM Address

1) Display of 5-dot font width character

♦ 5-dot 1 line display
In the case of 1 line display with 5-dot font, the address range of DDRAM is 00H - 4FH. (Refer to Fig-2)

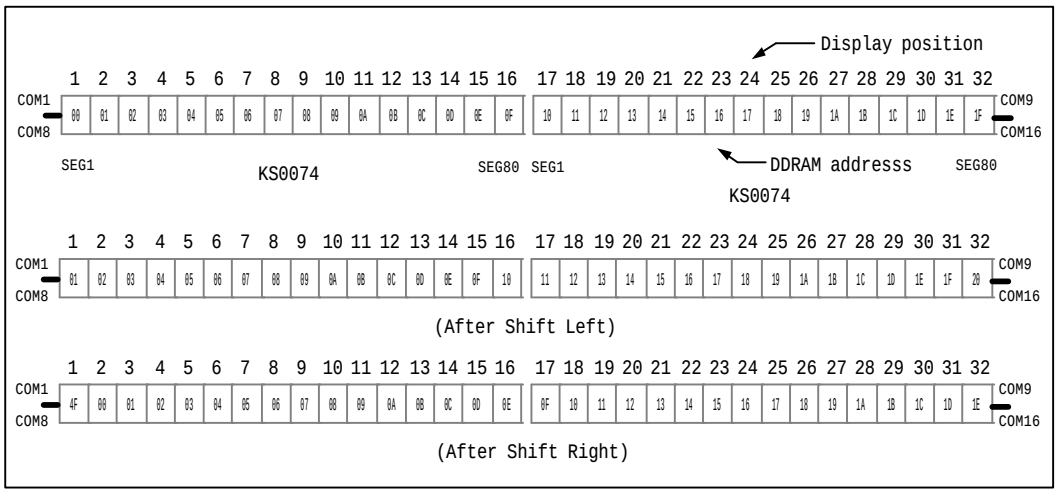


Fig-2. 1-line ´ 32ch. display

♦ 5-dot 2 line display
In the case of 2 line display with 5-dot font, the address range of DDRAM is 00H - 27H, 40H - 67H. (refer to Fig-3)

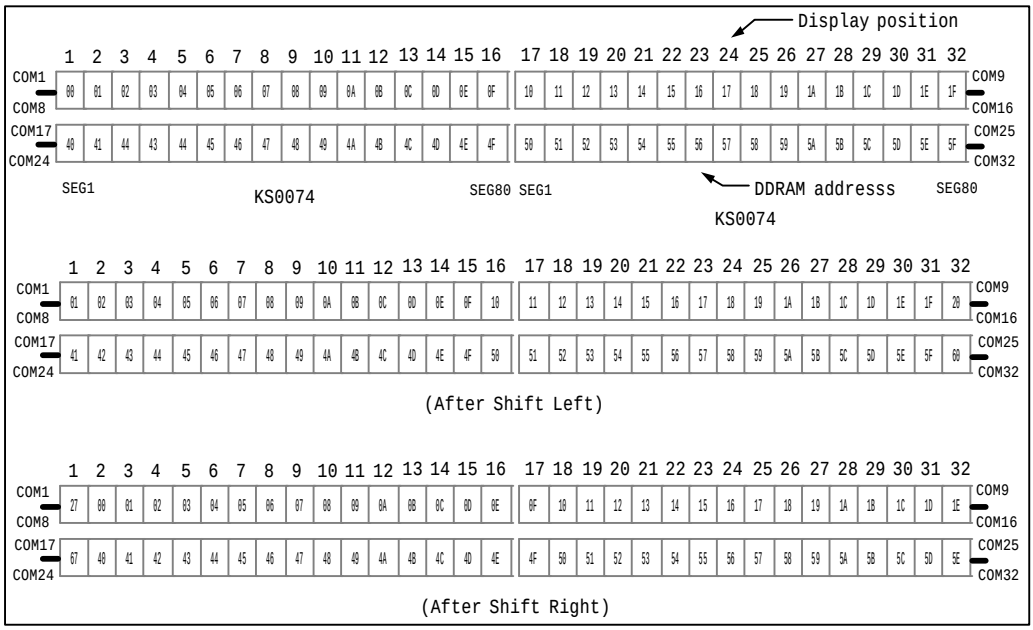


Fig-3. 2-line ´ 32ch. display (5-dot font width)

♦ 5-dot 4 line display
In the case of 4 line display with 5-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H.
(refer to Fig-4)

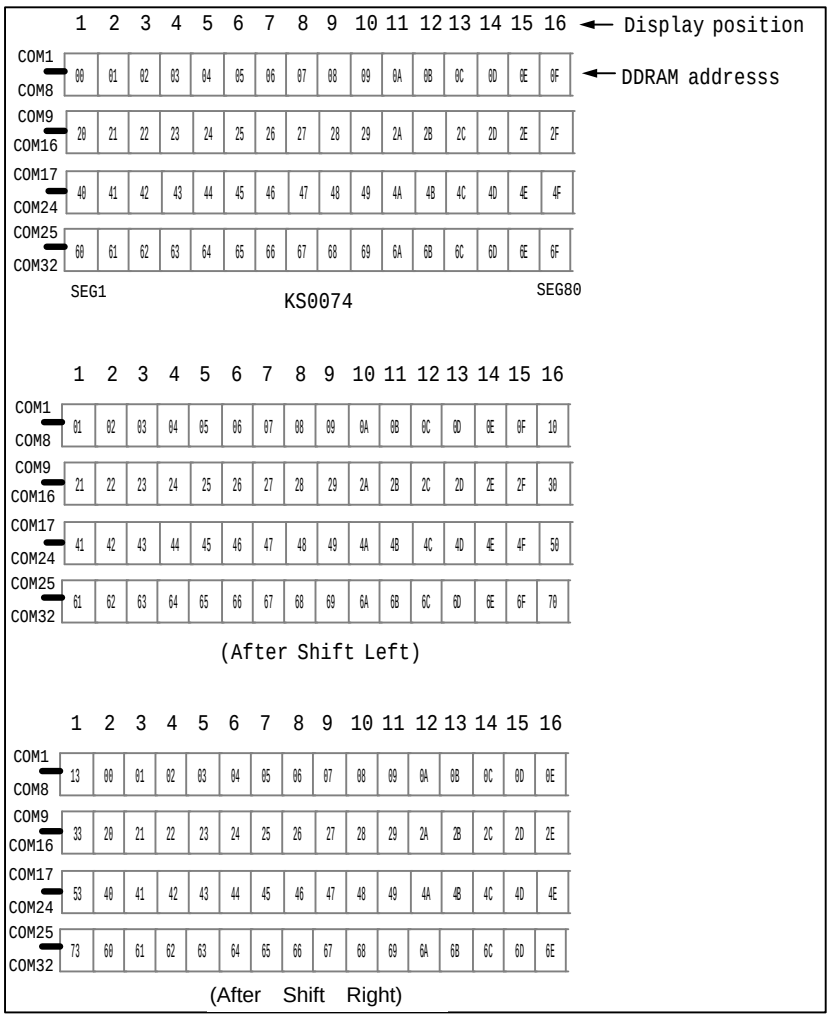


Fig-4. 4-line X 16ch. display (5-dot font width)

2) Display of 6-dot font width character

When this device is used in 6-dot font width mode, SEG79 and SEG80 must be open

① 6-dot 1 line display

In the case of 1 line display with 6-dot font, the address range of DDRAM is 00H-4FH. (Refer to Fig-5)

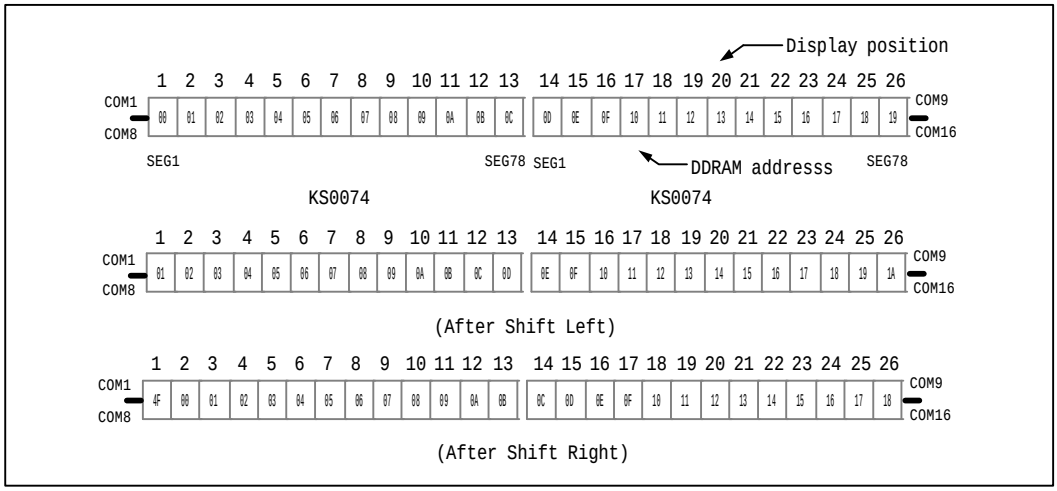


Fig-5. 1-line X 26ch. display

② 6-dot 2 line display

In the case of 2 line display with 6-dot font, the address range of DDRAM is 00H-27H, 40H-67H. (refer to Fig-6)

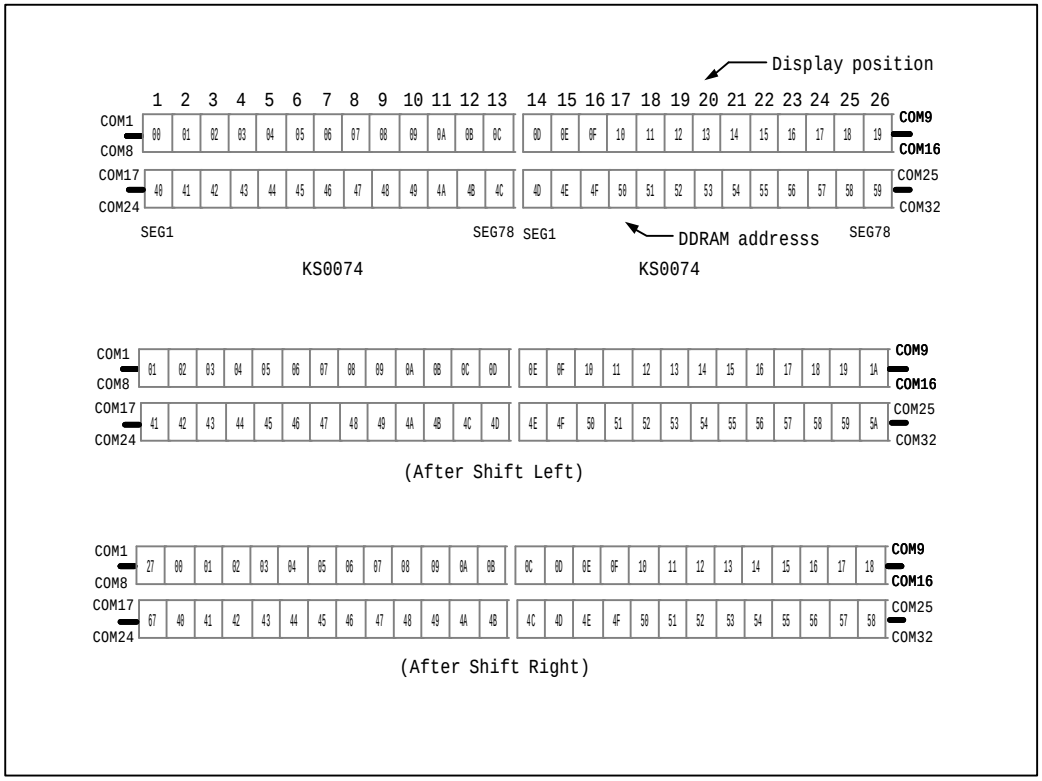


Fig-6. 2-line X 26h. display (6-dot font width)

③ 6-dot 4 line display

In case of 4 line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H. (refer to Fig-7)

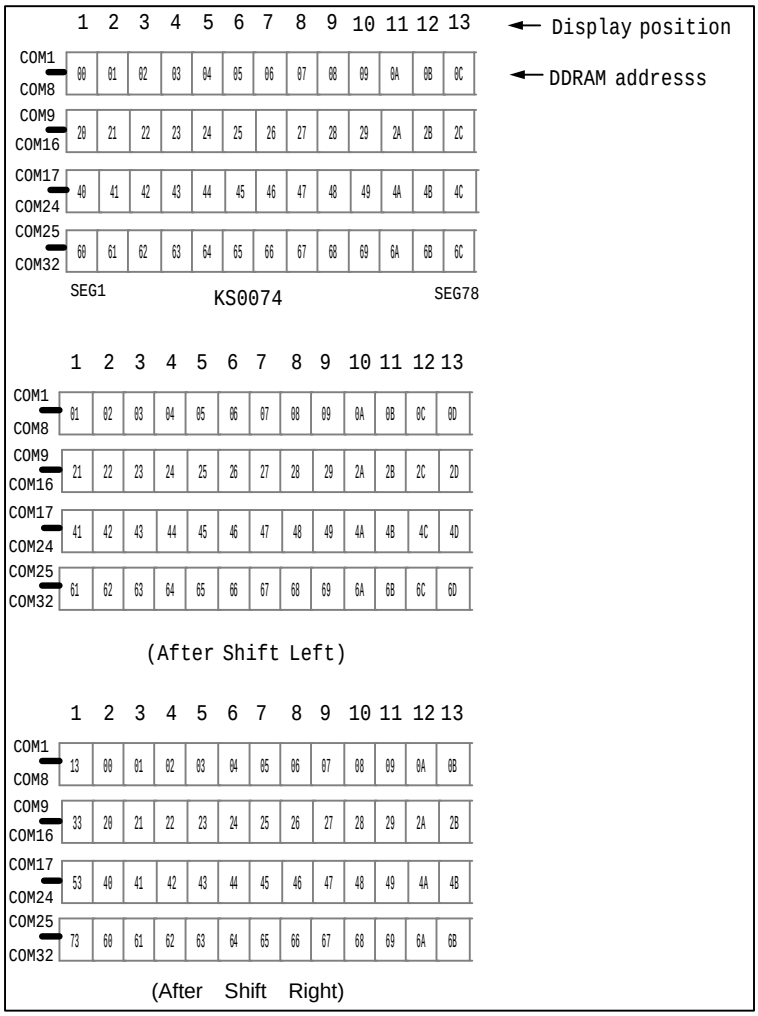


Fig-7. 4-line X 13ch. display (6-dot font width)

Timing Generation Circuit

Timing generation circuit generates clock signals for the internal operations.

Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR.
After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1.
When RS = "Low" and R/W = "High", AC can be read through DB0~DB6 ports.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

LCD Driver Circuit

LCD Driver circuit has 34 common and 80 segment signals for LCD driving.
Data from SEGRAM/CGRAM/CGROM is transferred to 80-bit segment latch serially, which is then stored to 80-bit shift latch. When each common is selected by 34-bit common register, segment data also output through segment driver from 80-bit segment latch.
In 1-line display mode, COM0 - COM17 have 1/17 duty, and in 2-line or 4-line mode, COM0 - COM33 have 1/33 duty ratio.

CGROM (Character Generator ROM)

CGROM has 5 × 8-dot 240 character pattern. (refer to Table 3)

Table 3. CGROM Character Code Table

CGRAM (Character Generator RAM)

CGRAM has up to 5 × 8-dot 8 characters. By writing font data to CGRAM, user defined character can be used.
(Refer to Table 4)

Table 4. Relationship between Character Code(DDRAM) and Character Pattern(CGRAM)

1) 5 × 8 dot Character pattern

Character Code(DDRAM data)								CGRAM address						CGRAM data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	X	0	¨ç	¨ç	¨ç	0	pattern 1
											0	0	1				¨ç	0	0	0	¨ç	
											0	1	0				¨ç	0	0	0	¨ç	
											0	1	1				¨ç	¨ç	¨ç	¨ç	¨ç	
											1	0	0				¨ç	0	0	0	¨ç	
											1	0	1				¨ç	0	0	0	¨ç	
											1	1	0				¨ç	0	0	0	¨ç	
											1	1	1				0	0	0	0	0	
			:						:			:						:					:
0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	X	¨ç	0	0	0	¨ç	pattern 8
											0	0	1				¨ç	0	0	0	¨ç	
											0	1	0				¨ç	0	0	0	¨ç	
											0	1	1				¨ç	¨ç	¨ç	¨ç	¨ç	
											1	0	0				¨ç	0	0	0	¨ç	
											1	0	1				¨ç	0	0	0	¨ç	
											1	1	0				¨ç	0	0	0	¨ç	
											1	1	1				0	0	0	0	0	

2) 6×8 dot Character pattern

Character Code(DDRAM data)								CGRAM address						CGRAM data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	X	0	0	0	0	0	0	0	0	0	B1	B0	0	0	¨ç	¨ç	¨ç	0	pattern 1
											0	0	1			0	¨ç	0	0	0	¨ç	
											0	1	0			0	¨ç	0	0	0	¨ç	
											0	1	1			0	¨ç	¨ç	¨ç	¨ç	¨ç	
											1	0	0			0	¨ç	0	0	0	¨ç	
											1	0	1			0	¨ç	0	0	0	¨ç	
											1	1	0			0	¨ç	0	0	0	¨ç	
											1	1	1			0	0	0	0	0	0	
				:					:			:					:						:
0	0	0	0	X	1	1	1	1	1	1	0	0	0	B1	B0	0	¨ç	0	0	0	¨ç	pattern 8
											0	0	1			0	¨ç	0	0	0	¨ç	
											0	1	0			0	¨ç	0	0	0	¨ç	
											0	1	1			0	¨ç	¨ç	¨ç	¨ç	¨ç	
											1	0	0			0	¨ç	0	0	0	¨ç	
											1	0	1			0	¨ç	0	0	0	¨ç	
											1	1	0			0	¨ç	0	0	0	¨ç	
											1	1	1			0	0	0	0	0	0	

* 1. When BE(Blink Enable bit) = "High", blink is controlled by B1 and B0 bit.
In displaying 5-dot font width, when B1 = "1", enabled dots of P0 - P4 will blink, and when B1 = "0" and B0 = "1", enabled dots in P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.
In displaying 6-dot font width, when B1 = "1", enabled dots of P0 - P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.

2. "X" : Don't care

SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During 1-line display mode, COM0(COM17) makes the data of SEGRAM enable to display icons. When used in 2/4-line display mode COM0(COM33) does that. Its higher 2-bits are blinking control data, and lower 6-bits are pattern data. (refer to Table 5 and Fig-8)

Table 5. Relationship between SEGRAM address and display pattern

SEGRAM address				SEGRAM data display pattern															
				5-dot font width								6-dot font width							
A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	B1	B0	X	S1	S2	S3	S4	S5	B1	B0	S1	S2	S3	S4	S5	S6
0	0	0	1	B1	B0	X	S6	S7	S8	S9	S10	B1	B0	S7	S8	S9	S10	S11	S12
0	0	1	0	B1	B0	X	S11	S12	S13	S14	S15	B1	B0	S13	S14	S15	S16	S17	S18
0	0	1	1	B1	B0	X	S16	S17	S18	S19	S20	B1	B0	S19	S20	S21	S22	S23	S24
0	1	0	0	B1	B0	X	S21	S22	S23	S24	S25	B1	B0	S25	S26	S27	S28	S29	S30
0	1	0	1	B1	B0	X	S26	S27	S28	S29	S30	B1	B0	S31	S32	S33	S34	S35	S36
0	1	1	0	B1	B0	X	S31	S32	S33	S34	S35	B1	B0	S37	S38	S39	S40	S41	S42
0	1	1	1	B1	B0	X	S36	S37	S38	S39	S40	B1	B0	S43	S44	S45	S46	S47	S48
1	0	0	0	B1	B0	X	S41	S42	S43	S44	S45	B1	B0	S49	S50	S51	S52	S53	S54
1	0	0	0	B1	B0	X	S46	S47	S48	S49	S50	B1	B0	S55	S56	S57	S58	S59	S60
1	0	0	1	B1	B0	X	S51	S52	S53	S54	S55	B1	B0	S61	S62	S63	S64	S65	S66
1	0	1	1	B1	B0	X	S56	S57	S58	S59	S60	B1	B0	S67	S68	S69	S70	S71	S72
1	1	0	0	B1	B0	X	S61	S62	S63	S64	S65	B1	B0	S73	S74	S75	S76	S77	S78
1	1	0	1	B1	B0	X	S66	S67	S68	S69	S70	-	-	-	-	-	-	-	-
1	1	1	0	B1	B0	X	S71	S72	S73	S74	S75	-	-	-	-	-	-	-	-
1	1	1	1	B1	B0	X	S76	S77	S78	S79	S80	-	-	-	-	-	-	-	-

* 1. B1, B0 : Blinking control bit

Control Bit			Blinking Port	
BE	B1	B0	5-dot font width	6-dot font width
0	X	X	No blink	No blink
1	0	0	No blink	No blink
1	0	1	D4	D5
1	1	X	D4 ~ D0	D5 ~ D0

2. S1~S80 : Icon pattern ON/OFF in 5-dot font width
   S1~S78 : Icon pattern ON/OFF in 6-dot font width
3. "X" : Don't care

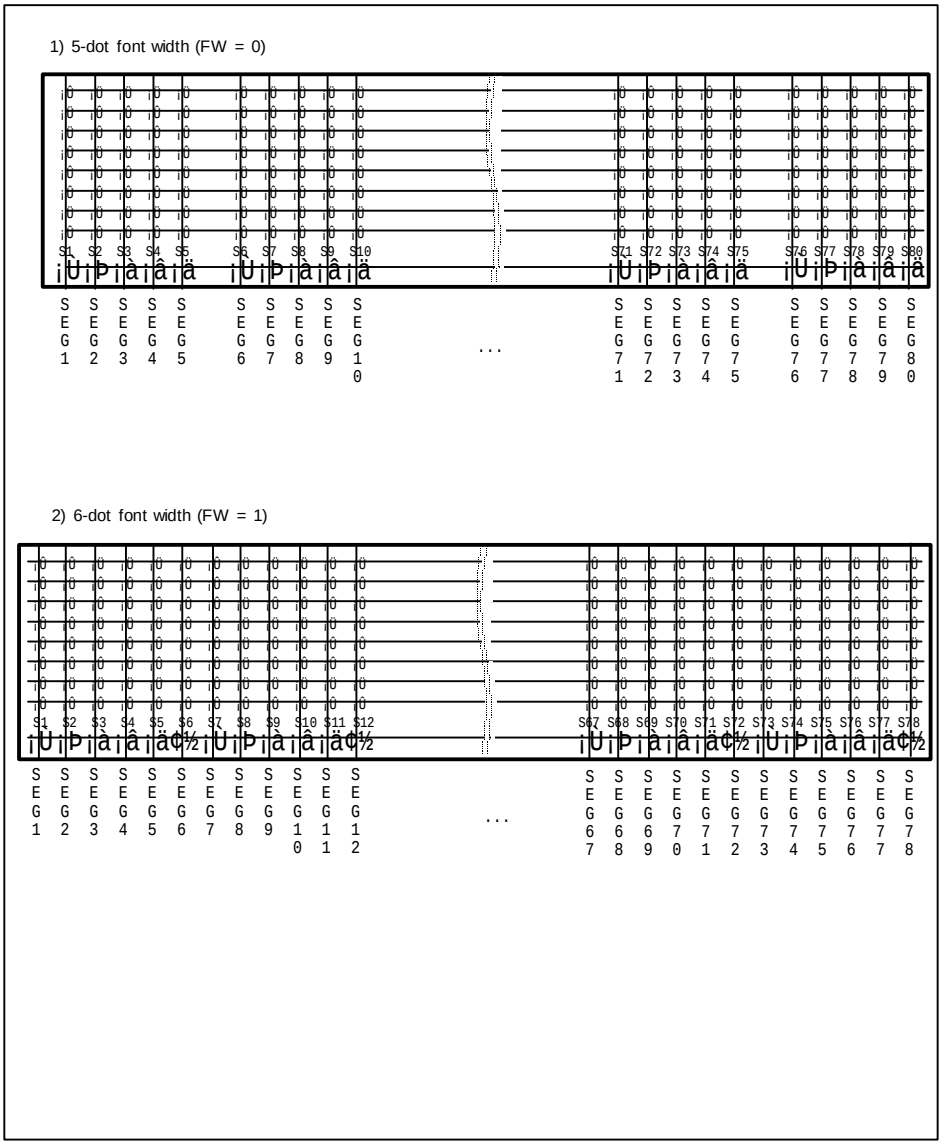


Fig-8. Relationship between SEGRAM and segment display

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of KS0074 and MPU clock, KS0074 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 6/10)

Instruction can be divided largely four kinds,

(1) KS0074 function set instructions (set display methods, set data length, etc.)

(2) address set instructions to internal RAM

(3) data transfer instructions with internal RAM

(4) others .

The address of internal RAM is automatically increased or decreased by 1.

When IE = "High", KS0074 is operated according to Instruction Set 1(Table 6) and when IE = "Low", KS0074 is operated according to Instruction Set 2(Table 10).

* Note : During internal operation, Busy Flag (DB7) is read High.
Busy Flag check must be proceeded the next instruction.
When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”

(1) INSTRUCTION DESCRIPTION 1 (IE = "High")

Table 6. Instruction Set 1

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power Down Mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = "1" :power down mode set, PD = "0" :power down mode disable	39 µs
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1" : increment, I/D = "0" : decrement and display shift enable bit. S = "1" : make display shift of the enabled lines by the DS4 - DS1 bits in the Shift Enable instruction. S = "0":display shift disable	39 µs
	1	0	0	0	0	0	0	0	1	1	BID	Segment bi-direction function. BID = "1" : Seg80 → Seg1, BID = "0" : Seg1 → Seg80.	
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1" : display on, D = "0" : display off, C = "1" : cursor on, C = "0" : cursor off, B = "1" : blink on, B = "0" : blink off.	39 µs
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1" : 6-dot font width, FW = "0" : 5-dot font width, B/W = "1" : black/white inverting of cursor enable, B/W = "0" : black/white inverting of cursor disable NW = "1" : 4-line display mode, NW = "0" : 1-line or 2-line display mode.	39µs

(Table 6. continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. S/C = "1" : display shift, S/C = "0" : cursor shift, R/L = "1" : shift to right, R/L = "0" : shift to left.	39 µs
Shift Enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH = "1") Determine the line for display shift . DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.	39 µs
Scroll Enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH = "0") Determine the line for horizontal smooth scroll. HS1 = "1/0" : 1st line dot scroll enable/disable HS2 = "1/0" : 2nd line dot scroll enable/disable HS3 = "1/0" : 3rd line dot scroll enable/disable HS4 = "1/0" : 4th line dot scroll enable/disable.	39 µs
Function Set	0	0	0	0	0	1	DL	N	RE(0)	DH	REV	Set interface data length (DL = "1" : 8-bit, DL = "0" : 4-bit), numbers of display line when NW = "0", (N = "1" : 2-line, N = "0" : 1-line), extension register, RE("0"), shift/scroll enable DH = "1" : display shift enable DH = "0" : dot scroll enable. reverse bit REV = "1" : reverse display, REV = "0" : normal display.	39 µs
	1	0	0	0	0	1	DL	N	RE(1)	BE	0	Set DL, N, RE("1") and CGRAM/SEGRAM blink enable (BE) BE = " 1/0" : CGRAM/SEGRAM blink enable/disable	39 µs

(Table 6. continued)

Instruction	RE	Instruction Code			Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		
Set CGRAM Address	0	0	0	0 1 AC5 AC4 AC3 AC2 AC1 AC0	Set CGRAM address in address counter.	39 µs
Set SEGRAM Address	1	0	0	0 1 X X AC3 AC2 AC1 AC0	Set SEGRAM address in address counter.	39 µs
Set DDRAM Address	0	0	0	1 AC6 AC5 AC4 AC3 AC2 AC1 AC0	Set DDRAM address in address counter.	39 µs
Set Scroll Quantity	1	0	0	1 X SQ5 SQ4 SQ3 SQ2 SQ1 SQ0	Set the quantity of horizontal dot scroll.	39 µs
Read Busy flag and Address	X	0	1	BF AC6 AC5 AC4 AC3 AC2 AC1 AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = "1" : busy state, BF = "0" : ready state.	0 µs
Write Data	X	1	0	D7 D6 D5 D4 D3 D2 D1 D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).	43 µs
Read Data	X	1	1	D7 D6 D5 D4 D3 D2 D1 D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).	43 µs

* Note : 1. When an MPU program with Busy Flag(DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the "E" signal after the Busy Flag (DB7) goes to "Low".
2. "X" Don't care

1) Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, hence, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

2) Return Home : (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Power Down Mode Set : (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	0	0	0	0	1	PD

Power down mode enable bit set instruction.
PD = "High", it makes KS0074 suppress current consumption except the current needed for data storage by executing next three functions.
1. make the output value of all the COM/SEG ports VDD
2. disable voltage converter to remove the current through the divide resistor of power supply.
This instruction can be used as power sleep mode.
When PD = "Low", power down mode becomes disabled.

4) Entry Mode Set

① (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the Shift Enable instruction is shifted to the right (I/D = "0") or to the left(I/D = "1"). But it will seem as if the cursor does not move.
When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display like this function is not performed.

② (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	BID

Set the data shift direction of segment in the application set.
BID : Data Shift Direction of Segment
When BID = "Low", segment data shift direction is set to normal order from SEG1 to SEG80.
When BID = "High", segment data shift direction is set to reverse from SEG80 to SEG1.
By using this instruction, the efficiency of application board area can be raised.
* The BID setting instruction is recommended to be set at the same time level of function set instruction.
* DB1 bit must be set to "1".

5) Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.
D : Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270 kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

6) Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW : Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width.
The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(refer to Fig-9)
When FW = "Low", 5-dot font width is set.

B/W : Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270 kHz, inversion has 370 ms intervals.

NW : 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

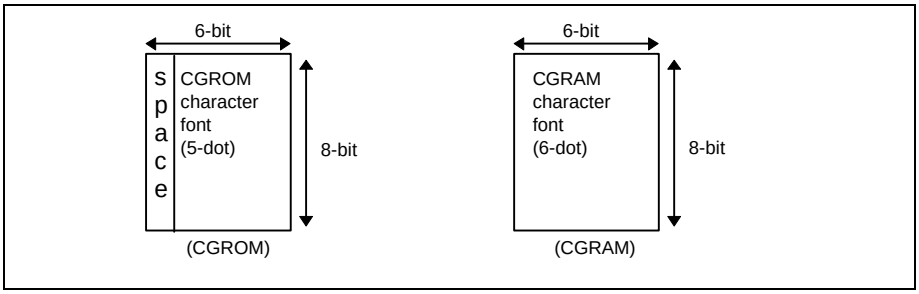


Fig-9. 6-dot font width CGROM/CGRAM

7) Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shift right/left cursor position or display, without writing or reading of display data.
This instruction is used to correct or search display data.(refer to Table 7)
During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously in all the line enabled by DS1-DS4 in the Shift Enable instruction.
When displayed data is shifted repeatedly, each line shifted individually.
When display shift is performed, the contents of address counter are not changed.
During low power consumption mode, display shift may not be performed normally.

Table 7. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by 1
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

8) Shift/Scroll Enable (RE = 1)

① (DH = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS : Horizontal Scroll per Line Enable
This instruction makes valid dot shift by a display line unit.
HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If the line in 1-line display mode or the 1st line in 2-line display mode is to be scrolled, set HS1 and HS2 to "High".
If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High". (refer to Table 8)

② (DH = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	DS4	DS3	DS2	DS1

DS : Display Shift per Line Enable
This instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction.
DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line.
If DS1 and DS2 is set to "High" (enable) in 2 line mode, only the 1st line is shifted and the 2nd line is not shifted.
When only DS1 = "High", only the half of the 1st line is shifted. If all the DS bits
(DS1 to DS4) are set to "Low" (disable), no display is shifted.

Table 8. Relationship between DS and COM signal

Enable bit	Enabled common signals during shift	Description
HS1/DS1	COM1 - COM8	The part of display line that corresponds to enabled common signal can be shifted.
HS2/DS2	COM9 - COM16	
HS3/DS3	COM17 - COM24	
HS4/DS4	COM25 - COM32	

9) Function Set

① (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (0)	DH	REV

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", it means 1-line display mode.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

DH : Display shift enable selection bit.
When DH = "High", enable display shift per line.
When DH = "Low", enable smooth dot scroll.
This bit can be accessed only when IE pin input is "High".

REV : Reverse enable bit
When REV = "High", all the display data are reversed. I.e., all the white dots become black and black dots become white.
When REV = "Low", the display mode set normal display.

② (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (1)	BE	0

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, BID bit, HS/DS bits of shift/scroll enable instruction and BE bits of function set register can be accessed.

BE : CGRAM/SEGRAM data blink enable bit
BE = “High”, makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

10) Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

11) Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	-	-	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

12) Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".
In 4-line display mode (NW = 1), DDRAM address is from "00H" to "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" to "53H" in the 3rd line and from "60H" to "73H" in the 4th line.

13) Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Setting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (Refer to Table 9).
In this case of KS0074 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

Table 9. Scroll quantity according to HDS bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	shift left by 1-dot
0	0	0	0	1	0	shift left by 2-dot
0	0	0	0	1	1	shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	shift left by 47-dot
1	1	X	X	X	X	shift left by 48-dot

14) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0074 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed. In this instruction value of address counter can also be read.

15) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

16) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If RAM data is read several times without RAM address set instruction before read operation, the correct RAM data can be obtained from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

(2) INSTRUCTION DESCRIPTION 2 (IE = "LOW")

Table 10. Instruction Set 2

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	X	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	X	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1" : increment, I/D = "0" : decrement. and display shift enable bit. S = "1" :make entire display shift of all lines during DDRAM write, S = "0":display shift disable	39µs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1" : display on, D = "0" : display off, C = "1" : cursor on, C = "0" : cursor off, B = "1" : blink on, B = "0" : blink off.	39µs
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1" : 6-dot font width, FW = "0" : 5-dot font width, B/W = "1" : black/white inverting of cursor enable, B/W = "0" : black/white inverting of cursor disable NW = "1" : 4-line display mode, NW = "0" : 1-line or 2-line display mode	39µs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	X	X	Cursor or display shift. S/C = “1” : display shift, S/C = “0” : cursor shift, R/L = “1” : shift to right, R/L = “0” : shift to left	39µs

(Table 10. continued)

Instruction	RE	Instruction Code			Description	Execution Time (fosc = 270 kHz)
		RS	R/W	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0		
Scroll Enable	1	0	0	0 0 0 1 HS4 HS3 HS2 HS1	Determine the line for horizontal smooth scroll. HS1 = "1/0" : 1st line dot scroll enable/disable HS2 = "1/0" : 2nd line dot scroll enable/disable HS3 = "1/0" : 3rd line dot scroll enable/disable HS4 = "1/0" : 4th line dot scroll enable/disable	39μs
Function Set	0	0	0	0 0 1 DL N RE(0) X X	Set interface data length DL = "1" : 8-bit, DL = "0" : 4-bit numbers of display line when NW = "0", N = "1" : 2-line, N = "0" : 1-line extension register, RE("0"),	39μs
	1	0	0	0 0 1 DL N RE(1) BE 0	Set DL, N, RE("1") and CGRAM/SEGRAM blink enable (BE) BE = " 1/0" : CGRAM/SEGRAM blink enable/disable	39μs
Set CGRAM Address	0	0	0	0 1 AC5 AC4 AC3 AC2 AC1 AC0	Set CGRAM address in address counter.	39μs
Set SEGRAM Address	1	0	0	0 1 X X AC3 AC2 AC1 AC0	Set SEGRAM address in address counter.	39μs
Set DDRAM Address	0	0	0	1 AC6 AC5 AC4 AC3 AC2 AC1 AC0	Set DDRAM address in address counter.	39μs
Set Scroll Quantity	1	0	0	1 X QC5 QC4 QC3 QC2 QC1 QC0	Set the quantity of horizontal dot scroll.	39μs
Read Busy flag and Address	X	0	1	BF AC6 AC5 AC4 AC3 AC2 AC1 AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = “1” : busy state, BF = “0” : ready state.	0μs
Write Data	X	1	0	D7 D6 D5 D4 D3 D2 D1 D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).	43μs
Read Data	X	1	1	D7 D6 D5 D4 D3 D2 D1 D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).	43μs

* Note : 1. When an MPU program with Busy Flag (DB7) checking is made, 1/2 Fosc (is necessary) for executing the next instruction by the falling edge of the “E” signal after the Busy Flag (DB7) goes to “Low”.

2. “X” don’t care

1) Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, hence, bring the cursor to the left edge on first line of the display. And entry mode is set to increment mode (I/D = "1").

2) Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

Return Home is cursor return home instruction.
Set DDRAM address to "00H" into the address counter.
Return cursor to its original site and return display to its original status, if shifted.
Contents of DDRAM does not change.

3) Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates identically to the DDRAM, when reading from or writing to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the entire display of all lines is shifted to the right (I/D = "0") or to the left(I/D = "1"). But it will seem as if the cursor does not moving.
When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of entire display is not performed.

4) Display ON/OFF Control (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.
D : Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270 kHz frequency, blinking has 370 ms interval.
When B = "Low", blink is off.

5) Extended Function Set (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	FW	B/W	NW

FW : Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width. The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(Refer to Fig-10)
When FW = "Low", 5-dot font width is set.

B/W : Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270 kHz, inversion has 370 ms intervals.

NW : 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

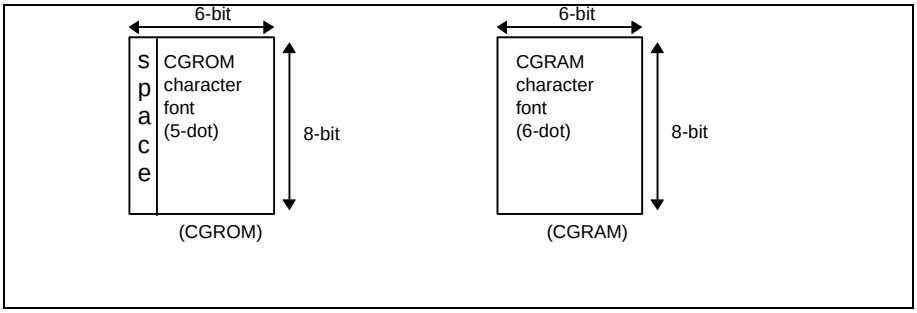


Fig-10. 6-dot font width CGROM/CGRAM

6) Cursor or Display Shift (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shift right/left cursor position or display without writing or reading of display data.
This instruction is used to correct or search display data.(Refer to Table 7) During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.
In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line.
Note that display shift is performed simultaneously in all the line.
When displayed data is shifted repeatedly, each line shifted individually.
When display shift is performed, the contents of address counter are not changed.

Table 11. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, ADDRESS COUNTER is decreased by 1
0	1	Shift cursor to the right, ADDRESS COUNTER is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

7) Scroll Enable (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	HS4	HS3	HS2	HS1

HS : Horizontal Scroll per Line Enable
This instruction makes valid dot shift by a display line unit.
HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If the line in 1-line display mode or the 1st line in 2-line display mode is to be scrolled, set HS1 and HS2 to "High".
If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High". (refer to Table 8)

8) Function Set

① (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (0)	-	-

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

② (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	RE (1)	BE	0

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
In 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, 4-line mode independent of N bit.

RE : Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, HS bits of scroll enable instruction and BE bits of function set register can be accessed.

BE : CGRAM/SEGRAM data blink enable bit
If BE is "High", makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

9) Set CGRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

10) Set SEGRAM Address (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	-	-	AC3	AC2	AC1	AC0

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

11) Set DDRAM Address (RE = 0)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".
In 4-line display mode (NW = 1), DDRAM address is from "00H" to "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" to "53H" in the 3rd line and from "60H" to "73H" in the 4th line.

12) Set Scroll Quantity (RE = 1)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	X	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0

Setting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (Refer to Table 12).
In this case of KS0074 execute dot smooth scroll from 1 to 48 dots.

Table 12. Scroll quantity according to HDS bits

SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Function
0	0	0	0	0	0	No shift
0	0	0	0	0	1	shift left by 1-dot
0	0	0	0	1	0	shift left by 2-dot
0	0	0	0	1	1	shift left by 3-dot
:	:	:	:	:	:	:
1	0	1	1	1	1	shift left by 47-dot
1	1	X	X	X	X	shift left by 48-dot

13) Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0074 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF to become “Low”, which by then the next instruction can be performed. In this instruction value of address counter can also be read.

14) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

15) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined. If the RAM data is read several times without RAM address set instruction before read operation, the correct RAM data from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, AC is increased/decreased by 1 like read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

INTERFACE WITH MPU

KS0074 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. Hence, both types of 4 or 8-bit MPU can be used.
In case of 4-bit bus mode, data transfer is performed by twice to transfer 1 byte data.

(1) When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by twice. Busy Flag outputs "High" after the second transfer is ended.

(2) When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

(3) If IM is set to "Low", serial transfer mode is set.

Interface with MPU in Bus Mode

1) Interface with 8-bits MPU

If 8-bits MPU is used, KS0074 can connect directly with that.
In this case, port E, RS, R/W and DB0 to DB7 need to interface each other.
Example of timing sequence is shown below.

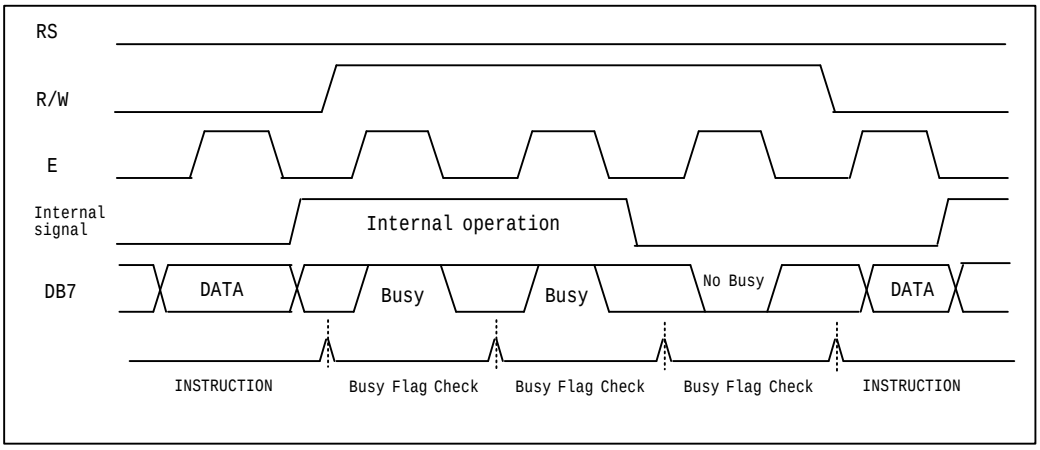


Fig 11. Example of 8-bit Bus Mode Timing Sequence

2) Interface with 4-bits MPU

If 4-bits MPU is used, KS0074 can connect directly with this.
In this case, port E, RS, R/W and DB4 to DB7 need to interface each other. The transfer is performed by twice.
Example of timing sequence is shown below.

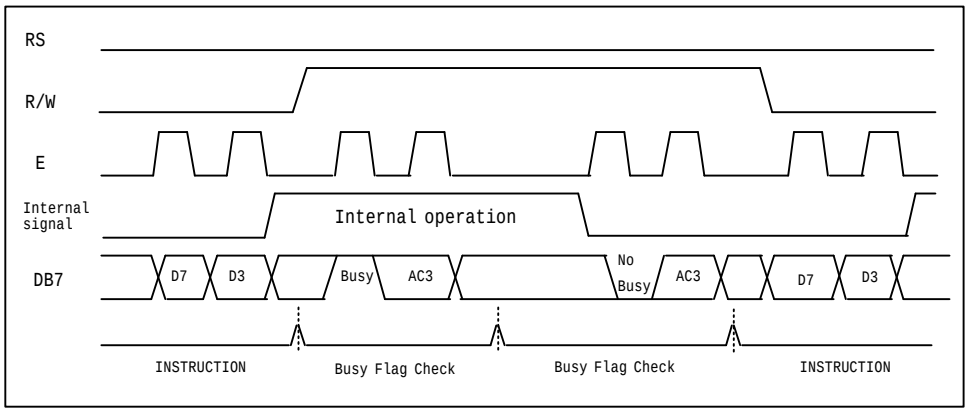


Fig 12. Example of 4-bit Bus Mode Timing Sequence

Interface with MPU in Serial Mode

When IM port input is "Low", serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If KS0074 is to be used with other chips, chip select port (CS) be used.
By setting CS to "Low", KS0074 can receive SCLK input. If CS is set to "High", KS0074 reset the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding 5 "High" bits, read write control bit (R/W), register selection bit (RS), and end bit that indicates the end of start byte. Whenever succeeding 5 "High" bits are detected by KS0074, it resets serial transfer counter and prepares to receive next information.
The next input data are register selection bit which determine which register is to be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (Refer to Fig 13. Fig 14)

(1) Write Operation (R/W = 0)
After start byte is transferred from MPU to KS0074, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer.
To transfer several bytes continuously without changing R/W bit and RS bit, start byte transfer is needed only at first starting time. I.e., after first start byte is transferred, real data succeeding can be transferred.

(2) Read Operation (R/W = 1)
After start byte is transferred to KS0074, MPU can receive 8-bit data through the SOD port at a time from the LSB.
Wait time is needed to insert between start byte and data reading, as internal reading from RAM requires some delay.
Continuous data reading is possible such as serial write operation. It also needs only one start bytes, only if some delay between reading operations of each byte is inserted. During the reading operation, KS0074 observes succeeding 5 "High" from MPU. If detected, KS0074 restarts serial operation at once and prepares to receive RS bit.
So in continuous reading operation, SID port must be “Low”.

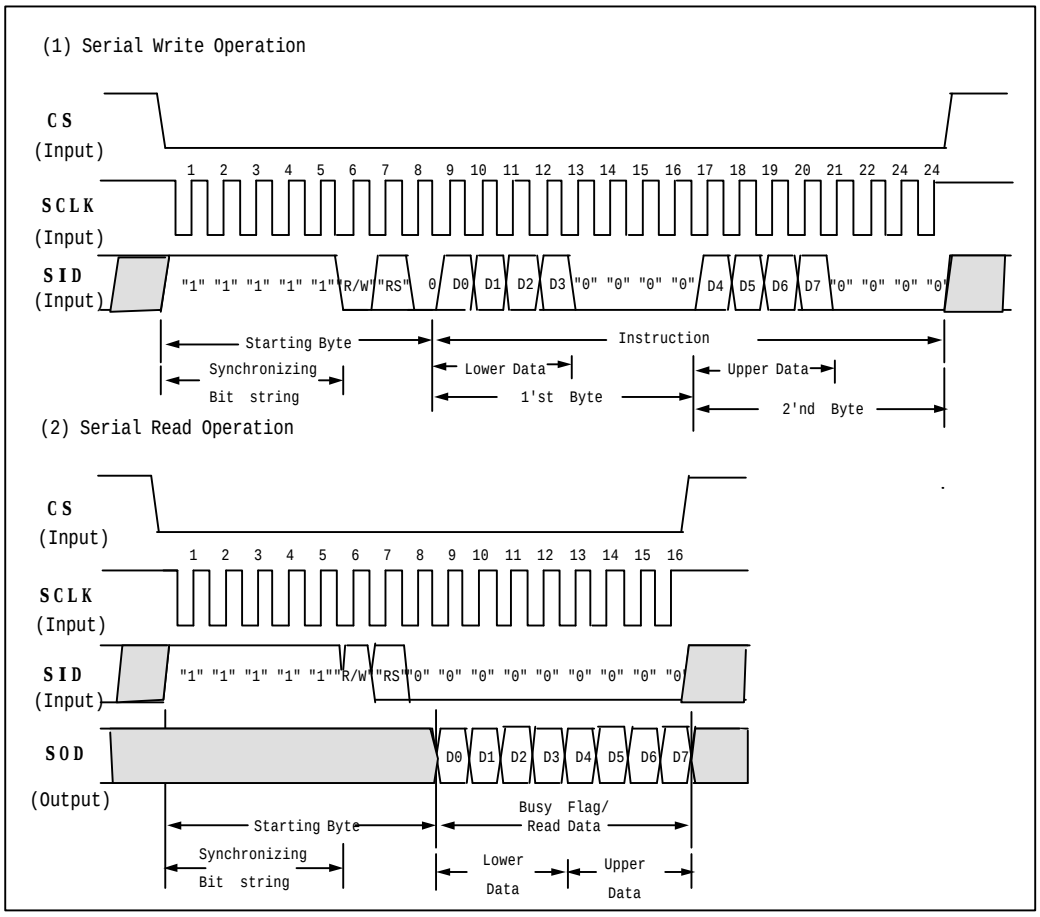


Fig 13. Timing Diagram of Serial Data Transfer

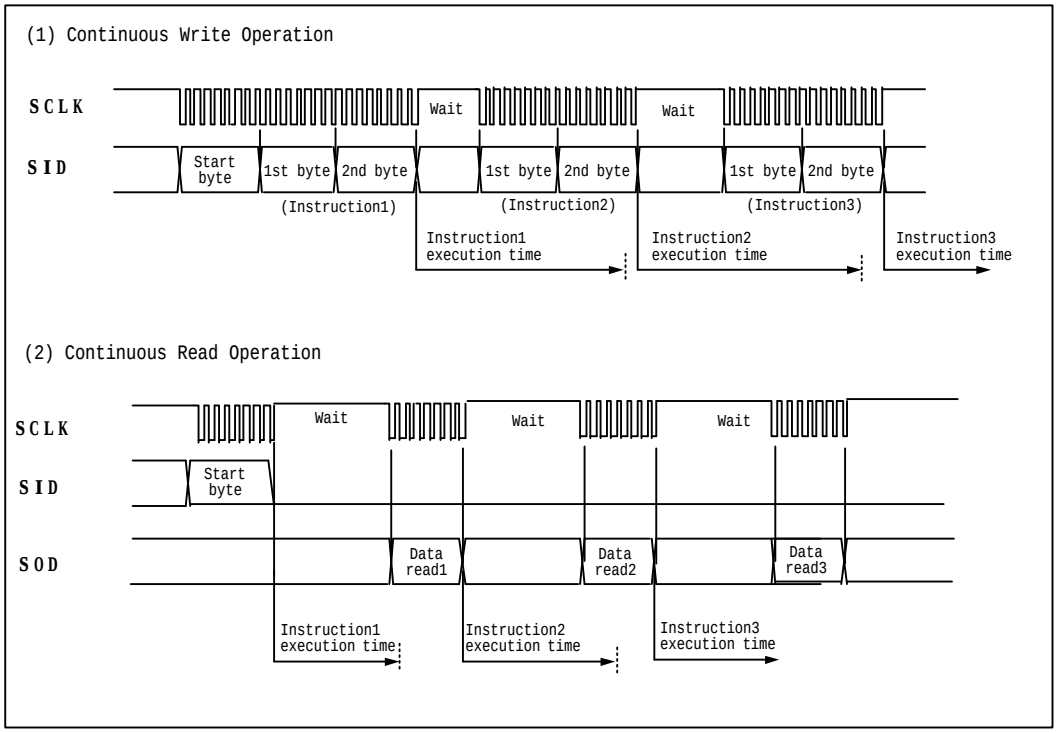
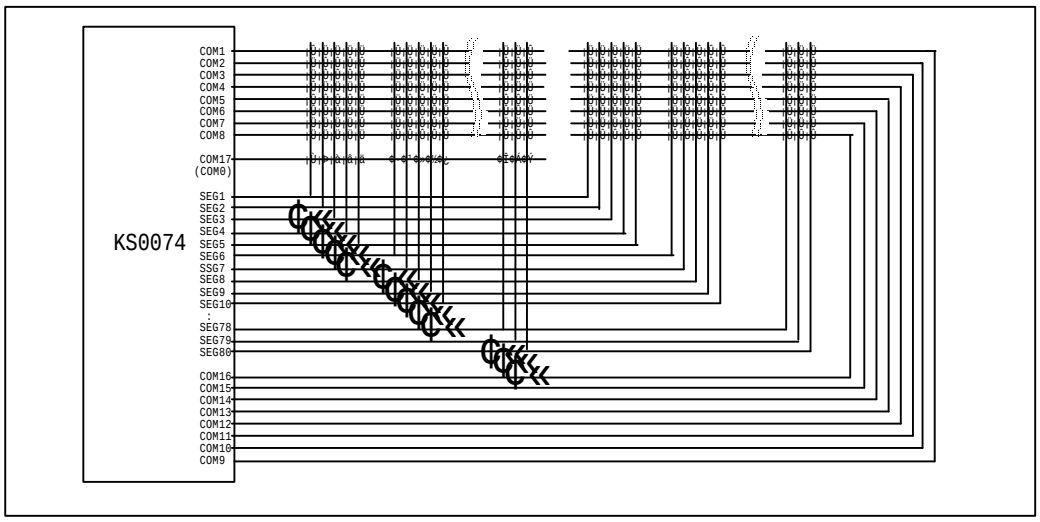


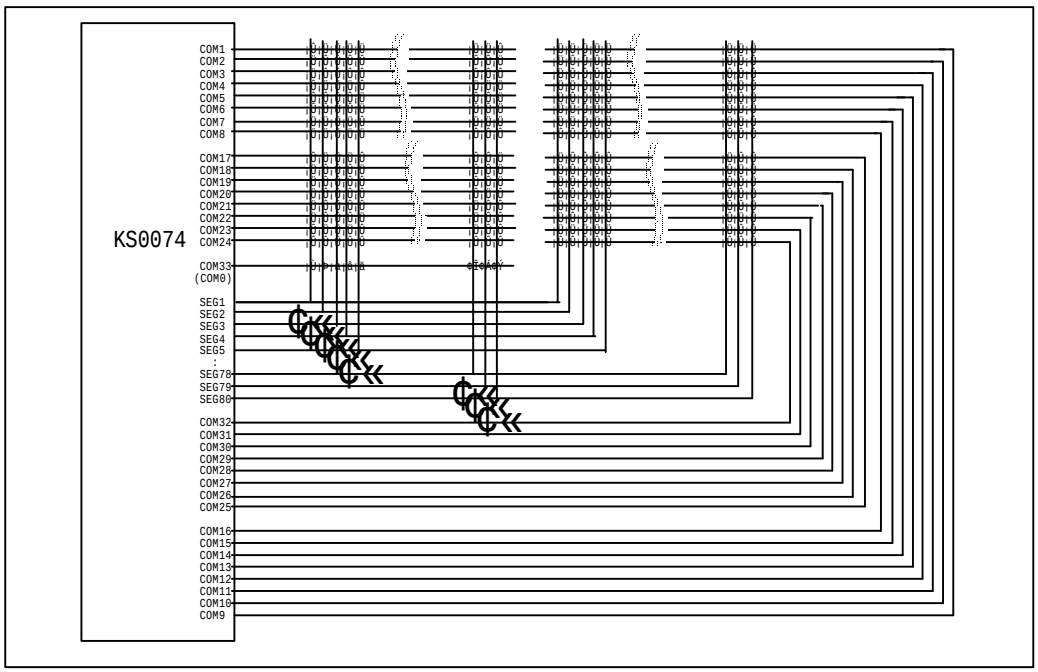
Fig 14. Timing Diagram of Continuous Data Transfer

APPLICATION INFORMATION ACCORDING TO LCD PANEL

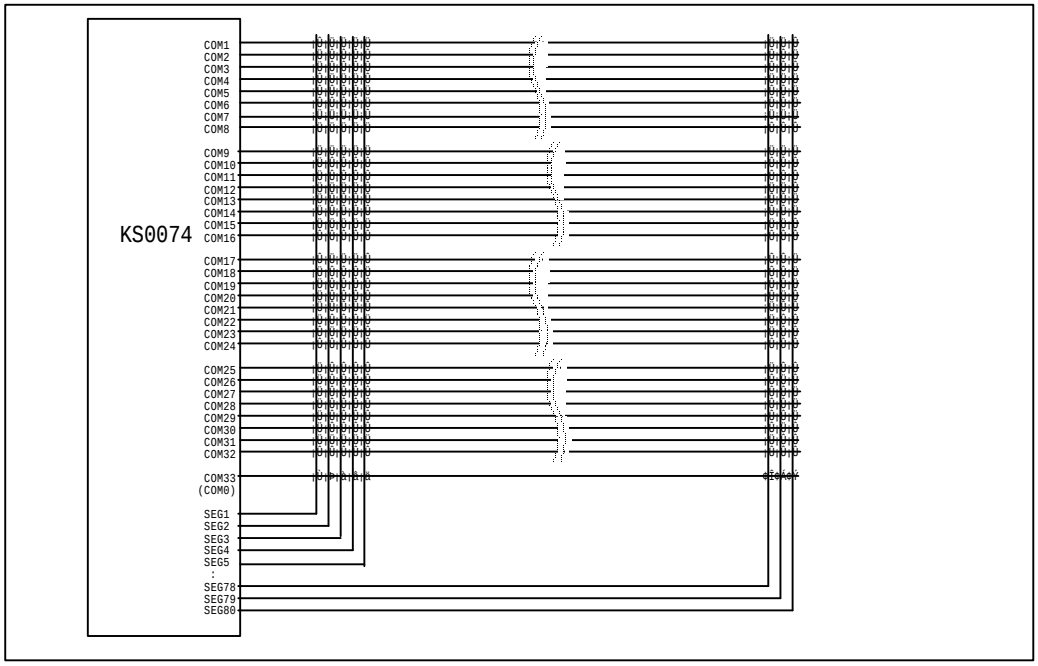
1) LCD Panel : 32 character x 1 line format (5-dot font,1/17 duty)



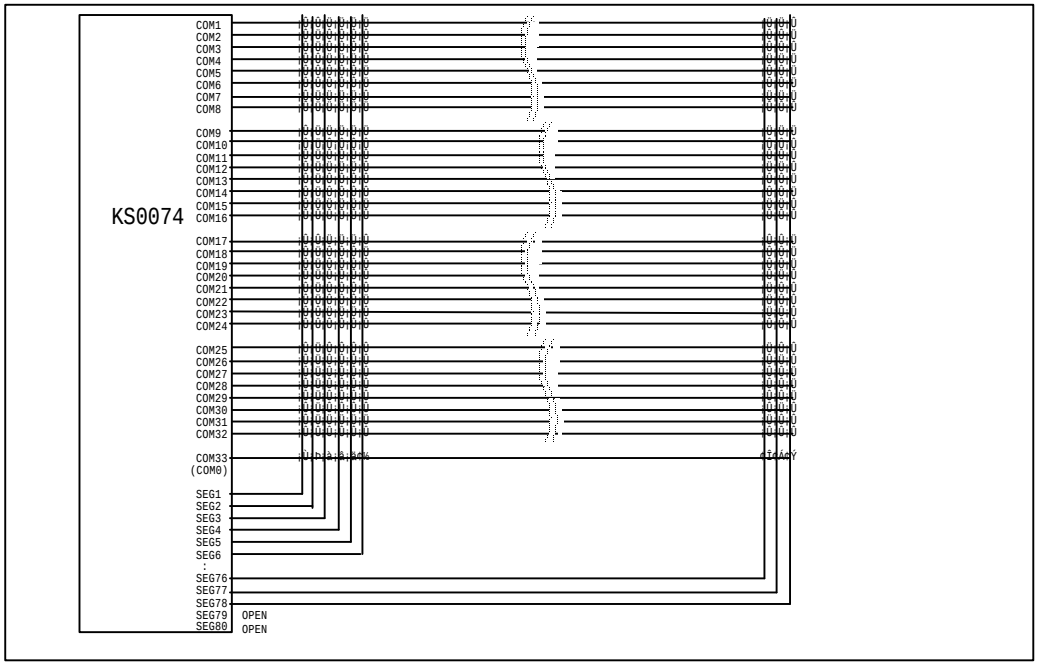
2) LCD Panel : 32 character x 2 line format (5-dot font, 1/33 duty)



3) LCD Panel : 16 character x 4 line format (5-dot font, 1/33 bias)



4) LCD Panel : 13 character x 4 line format (6-dot font, 1/33 bias)



INITIALIZING

1) Initializing by Internal Reset Circuit

When the power is turned on, KS0074 is initialized automatically by power on reset circuit.

During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

i) Display Clear instruction

Write "20H" to all DDRAM

ii) Set Functions instruction

DL = 1 : 8-bit bus mode

N = 1 : 2-line display mode

RE = 0 : Extension register disable

BE = 0 : CGRAM/SEGRAM blink OFF

DH = 0 : Horizontal scroll enable

REV = 0 : Normal display (Not reversed display)

iii) Control Display ON/OFF instruction

D = 0 : Display OFF

C = 0 : Cursor OFF

B = 0 : Blink OFF

iv) Set Entry Mode instruction

I/D = 1 : Increment by 1

S = 0 : No entire display shift

BID = 0 : Normal direction segment port

v) Set Extension Function instruction

FW = 0 : 5-dot font width character display

B/W = 0 : Normal cursor (8th line)

NW = 0 : Not 4-line display mode, 2-line mode is set because of N("1")

vi) Enable Shift instruction

HS = 0000 : Scroll per line disable

DS = 0000 : Shift per line disable

vii) Set scroll Quantity instruction

SQ = 000000 : Not scroll

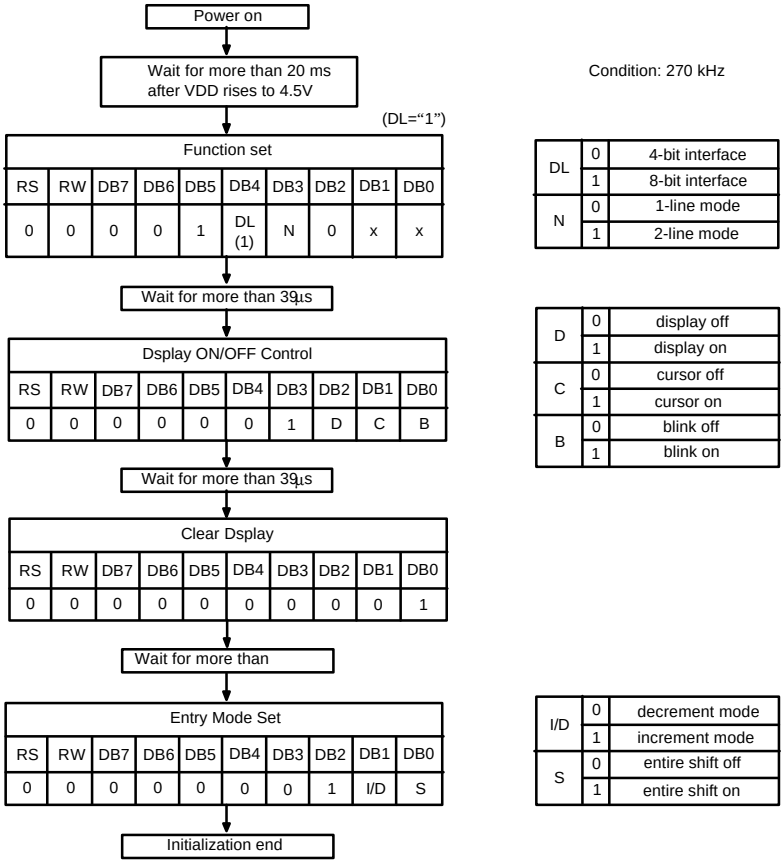
2) Initializing by Hardware RESET input

When RESET pin = "Low", KS0074 can be initialized like the case of power on reset.

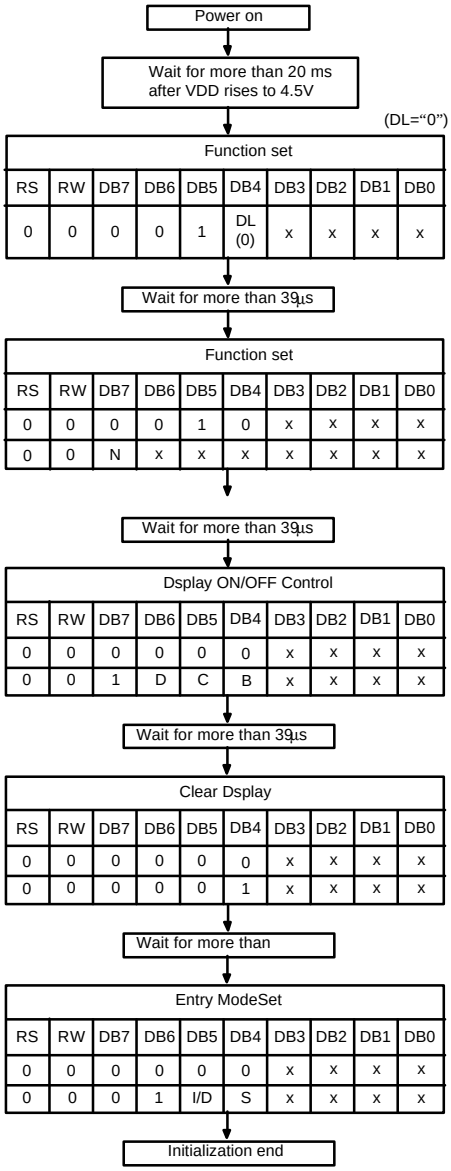
During the power on reset operation, this pin is ignored.

INITIALIZING BY INSTRUCTION

1) 8-bit interface mode



2) 4-bit interface mode



Condition: 270 kHz

DL	0	4-bit interface
	1	8-bit interface
N	0	1-line mode
	1	2-line mode

D	0	display off
	1	display on
C	0	cursor off
	1	cursor on
B	0	blink off
	1	blink on

I/D	0	decrement mode
	1	increment mode
S	0	entire shift off
	1	entire shift on

EXAMPLE OF INSTRUCTION AND DISPLAY CORRESPONDENCE

1) IE = "Low"

1.Power Supply on : Initialized by the internal power on reset circuit.

LCD DISPLAY

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2.Function Set : 8-bit, 1-line, RE(0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	0	0	X	X

3.Display ON/OFF Control : Display/Cursor on

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

_

4.Entry Mode Set : Increment

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	0

_

5.Write Data to DDRAM : Write S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

S_

6.Write Data to DDRAM : Write A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

SA_

7.Write Data to DDRAM : Write M

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	1

SAM_

8. Write data to DDRAM : Write S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

SAMS_

9. Write data to DDRAM : Write U

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	1	0	1

SAMSU_

10. Write data to DDRAM : Write N

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	1	0

SAMSUN_

11. Write data to DDRAM : Write G

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

SAMSUNG_

12. Cursor or Display Shift : Cursor shift to right

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	1	X	X

SAMSUNG _

13. Entry Mode Set : Entire display shift enable

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1

SAMSUNG _

14. Write data to DDRAM : Write K

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

AMSUNG K_

15. Write data to DDRAM : Write S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

MSUNG KS_

16. Write data to DDRAM : Write 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

SUNG KS0_

17. Write data to DDRAM : Write 0

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	0	0

UNG KS00_

18. Write data to DDRAM : Write 7

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	1	1

NG KS007_

19. Write data to DDRAM : Write 3

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	0	1	1

G KS0073_

20. Cursor or Display Shift : Cursor shift left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	0	0	X	X

G KS0073

21. Write Data to DDRAM : Write 4

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	0	0

KS0074_

22. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

SAMSUNG KS0074

23. Clear Display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

_

2) IE = "High"

1. Power Supply on : Initialized by the internal power on reset circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

2. Function Set : 8-bit, RE(1)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

3. Extended Function Set : 5-font, 4-line

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	0	0	1

4. Function Set : RE(0)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

5. Display ON/OFF Control : Display/Cursor on

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	1	1	0

6. Write data to DDRAM : Write S

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	1

7. Write data to DDRAM : Write A

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	0	1

SA_

⋮

12. Write data to DDRAM : Write G

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	1	1

SAMSUNG_

13. Set DDRAM Address 20H

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	0

SAMSUNG
_

14. Write data to DDRAM : Write K

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	1	1

SAMSUNG
K_

⋮

19. Write data to DDRAM : Write 4

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	0	1	1	0	1	0	0

SAMSUNG
KS0074_

20. Set DDRAM Address 40H

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	0	0	0	0

SAMSUNG
KS0074
_

21. Write data to DDRAM : Write L

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	1	0	0

SAMSUNG
KS0074
L_

⋮

30. Write data to DDRAM : Write R

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

SAMSUNG
KS0074
LCD DRIVER_

31. Set DDRAM Address 60H

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

SAMSUNG
KS0074
LCD DRIVER
_

⋮

43. Write data to DDRAM : Write R

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	1	0	0	1	0

SAMSUNG
KS0074
LCD DRIVER
& CONTROLLER_

44. Function Set : RE("0"), DH("1")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0

SAMSUNG
KS0074
LCD DRIVER
& CONTROLLER_

45. Function Set : RE("1")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

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KS0074
LCD DRIVER
& CONTROLLER_

46. Shift/Scroll Enable : DS4("1"),DS3/2/1("0")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	0	0

```
SAMSUNG
KS0074
LCD DRIVER
& CONTROLLER_
```

47. Function Set : RE("0")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	0

```
SAMSUNG
KS0074
LCD DRIVER
& CONTROLLER_
```

48. Cursor or Display Shift : Display shift to left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

```
SAMSUNG
KS0074
LCD DRIVER
 CONTROLLER_
```

49. Cursor or Display Shift : Display shift to left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

```
SAMSUNG
KS0074
LCD DRIVER
CONTROLLER_
```

50. Cursor or Display Shift : Display shift to left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

```
SAMSUNG
KS0074
LCD DRIVER
ONTROLLER_
```

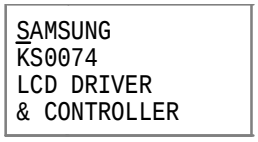
51. Cursor or Display Shift : Display shift to left

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	0	X	X

```
SAMSUNG
KS0074
LCD DRIVER
NTROLLER_
```

52. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X



53. Function Set : RE("0"),REV("1")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	1	1

54. Cursor or Display Shift : Display shift to right

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

55. Cursor or Display Shift : Display shift to right

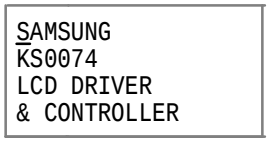
RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	1	1	X	X

56. Return Home

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	X

57. Function Set : RE("0"),REV("0")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	0	0	0

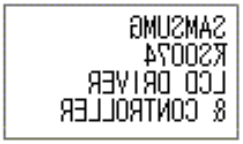


58. Function Set : RE("1")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	0	0

59. Entry Mode Set : BID("1")

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	1	1



60. Clear Display

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

61. Write Data to DDRAM : Write B

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	0	1	0

62. Write Data to DDRAM : Write I

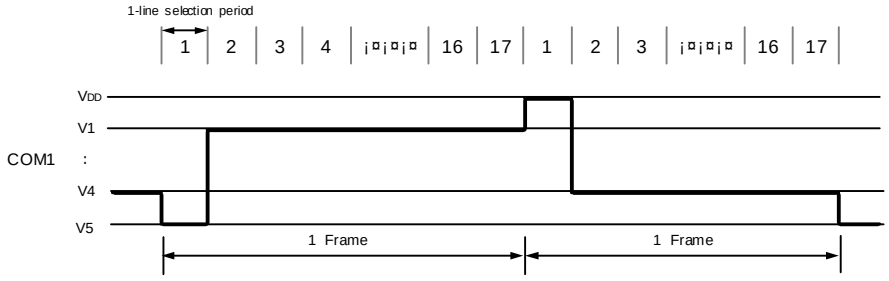
RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	1	0	0	1

63. Write Data to DDRAM : Write D

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	0	1	0	0	0	1	0	0

FRAME FREQUENCY

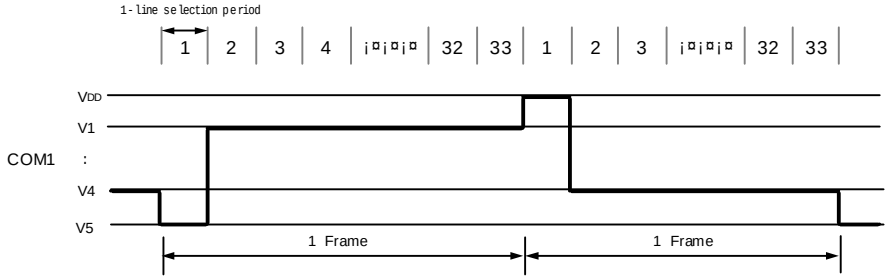
1) 1/17 duty cycle



Item	Display Font Width	
	5-dot font width	6-dot font width
1-line selection period	200 clocks	240 clocks
Frame frequency	79.4Hz	66.2Hz

* fosc = 270 kHz (1 clock = 3.7µs)

2) 1/33 duty cycle

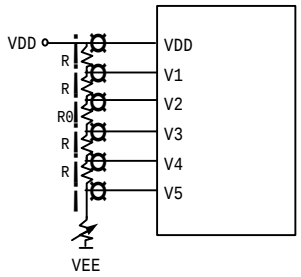


Item	Display Font Width	
	5-dot font width	6-dot font width
1-line selection period	100 clocks	120 clocks
Frame frequency	81.8Hz	68.2Hz

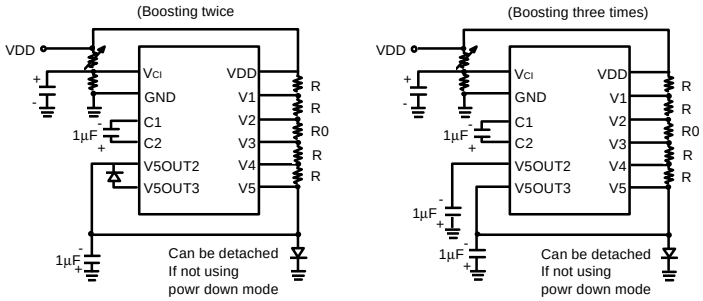
* fosc = 270 kHz (1 clock = 3.7 µs)

POWER SUPPLY FOR DRIVING LCD PANEL

1) When an external power supply is used



2) When an internal booster is used



* 1. Boosted output voltage should not exceed the maximum value (13 V) of the LCD driving voltage. Especially, a voltage of over 4.3V should not be input to the reference voltage (Vci) when boosting three times.

2. A voltage of over 5.5V should not be input to the reference voltage (Vci) when boosting twice.

3. The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (Refer to Table 13)

Table 13. Duty Ratio and Power Supply for LCD Driving

Item		Data	
Number of lines		1	2 or 4
Duty ratio		1/17	1/33
Bias		1/5	1/6.7
Divided resistance	R	R	R
	R0	R	2.7R

MAXIMUM ABSOLUTE RATE

Characteristic	Symbol	Value	Unit
Power Supply Voltage (1)	V_{DD}	-0.3 to +7.0	V
Power Supply Voltage (2)	V_{LCD}	V_{DD} -15.0 to V_{DD} +0.3	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Operating Temperature	T_{OPR}	-30 to +85	^{o}C
Storage Temperature	T_{STG}	-55 to +125	^{o}C

* Voltage greater than above may damage to the circuit (VDD≥V1≥V2≥V3≥V4≥V5)

ELECTRICAL CHARACTERISTICS

DC Characteristics

(VDD = 2.7V to 5.5V, Ta=-30 to +85 °C)

Characteristic	Symbol	Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	-		2.7	-	5.5	V
Supply Current	I_{DD}	Internal oscillation or external clock. (V_{DD}=3.0V,fosc=270KHz		-	0.15	0.3	mA
Input Voltage (1) (Except OSC1)	V_{IH1}	-		$0.7V_{DD}$	-	V_{DD}	-
	V_{IL1}	V_{DD}=2.7 to 3.0		-0.3	-	$0.2V_{DD}$	
		V_{DD}=3.0 to 5.5		-0.3	-	0.6	
Input Voltage (2) (Osc1)	V_{IH2}	-		$0.7V_{DD}$	-	V_{DD}	V
	V_{IL2}	-		-	-	$0.2V_{DD}$	
Output Voltage (1) (DB0 To DB7)	V_{OH1}	I_{OH}=-0.1mA		$0.75V_{DD}$	-	-	V
	V_{OL1}	I_{OL}=0.1 mA		-	-	$0.2V_{DD}$	
Output Voltage(2) (Except DB0 To DB7)	V_{OH2}	I_O=-40 µA		$0.8V_{DD}$	-	-	V
	V_{OL1}	I_O=40 µA		-	-	$0.2V_{DD}$	
Voltage Drop	Vd_{COM}	I_O= ±0.1mA		-	-	1	V
	Vd_{SEG}			-	-	1	
Input Leakage Current	I_{IL}	V_{IN}=0V to V_{DD}		-1	-	1	µA
Low Input Current	I_{IN}	V_{IN}=0V, V_{DD}=3V (PULL UP)		-10	-50	-120	
Internal Clock (external Rf)	f_{OSC}	Rf=91kΩ ±2% (V_{DD}=5V)		190	270	350	KHz
External Clock	f_{EC}	-		125	270	410	KHz
	duty			45	50	55	%
	t_R, t_F			-	-	0.2	µs
Voltage Converter Out2 (Vci = 4.5V)	V_{OUT2}	Ta = 25 °C, C=1µF, I_{OUT} = 0.25mA, f_{OSC}=270KHz		-3.0	-4.2	-	V
Voltage Converter Out3 (Vci = 2.7V)	V_{OUT3}			-4.3	-5.1	-	
Voltage Converter Input	Vci	-		1.0	-	4.5	V
LCD Driving Voltage	V_{LCD}	V_{DD}-V5	1/5 Bias	3.0	-	13.0	
			1/6.7 Bias	3.0	-	13.0	

AC Characteristics

(V_{DD}=4.5 to 5.5V, Ta=-30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(1) Write Mode (refer to Fig-15)	E Cycle Time	tc,	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_H1	10	-	-	
	Data Setup Time	tsu2	60	-	-	
	Data Hold Time	t_H2	10	-	-	
(2) Read Mode (refer to Fig-16)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	160	
	Data Hold Time	t_{DH}	5	-	-	
(3) Serial Interface Mode (refer to Fig-17)	Serial Clock Cycle Time	tc	0.5	-	20	µs
	Serial Clock Rise/Fall Time	t_R,t_F	-	-	50	ns
	Serial Clock Width (High, Low)	tw	200	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	t_H1	20	-	-	
	Serial Input Data Setup Time	tsu2	100	-	-	
	Serial Input Data Hold Time	t_H2	100	-	-	
	Serial Output Data Delay Time	t_D	-	-	160	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

AC Characteristics (continued)

(V_{DD}=2.7 tp 4.5V, Ta=-30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
(4) Write Mode (refer to Fig-15)	E Cycle Time	tc,	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_H1	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_H2	10	-	-	
(5) Read Mode (refer to Fig-16)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	
(6) Serial Interface Mode (refer to Fig-17)	Serial Clock Cycle Time	tc	1	-	20	µs
	Serial Clock Rise/Fall Time	t_R,t_F	-	-	50	ns
	Serial Clock Width (High, Low)	tw	400	-	-	
	Chip Select Setup Time	tsu1	60	-	-	
	Chip Select Hold Time	t_H1	20	-	-	
	Serial Input Data Setup Time	tsu2	200	-	-	
	Serial Input Data Hold Time	t_H2	200	-	-	
	Serial Output Data Delay Time	t_D	-	-	360	
	Serial Output Data Hold Time	t_{DH}	5	-	-	

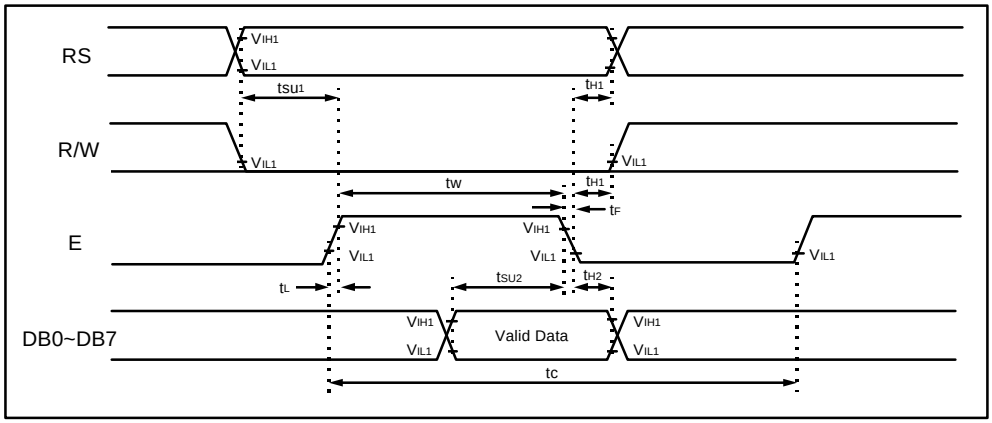


Fig-15. Write Mode

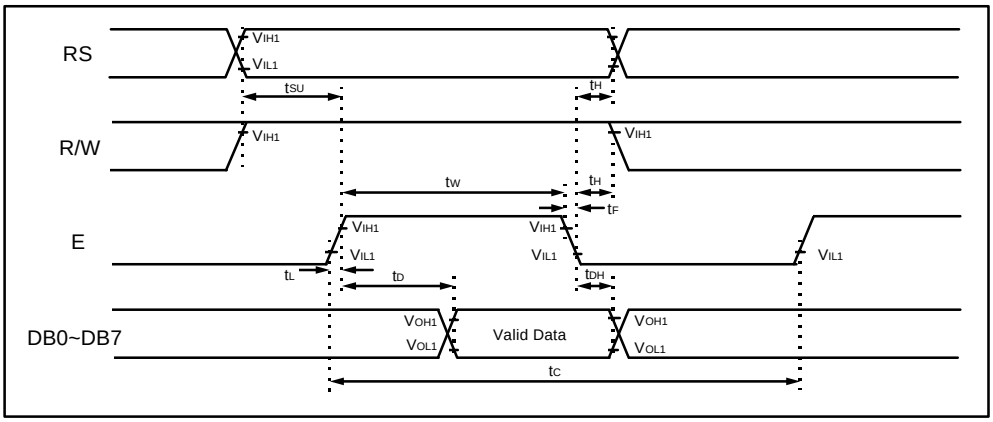


Fig-16. Read Mode

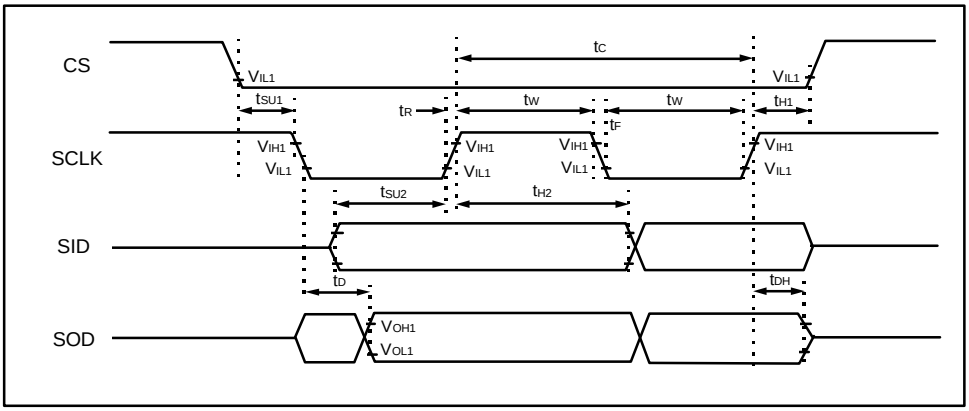


Fig-17. Serial Interface Mode

Reset Timing

(V_{DD} = 2.7 to 5.5V, Ta = -30 to +85°C)

Item	Symbol	Min	Typ	Max	Unit
Reset low level width (refer to Fig-18)	t_{RES}	10	-	-	ms

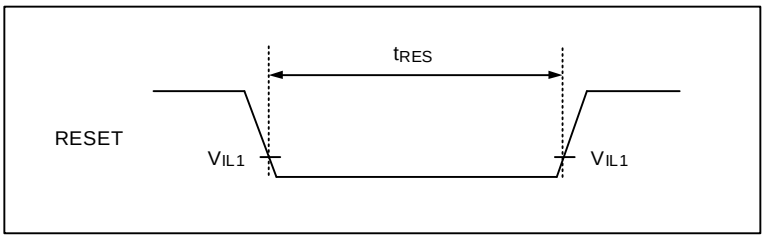


Fig-18. Reset Timing Diagram