8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

S54164
N74164

S54164–A,F,W • N74164–A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The S54164 is characterized for operation over the full military temperature range of −55°C to 125°C; the N74164 is characterized for operation from 0°C to 70°C.

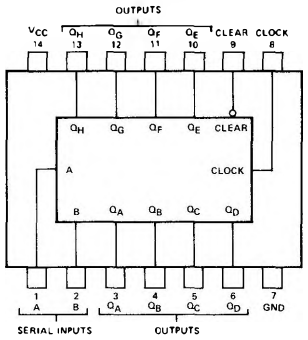
TRUTH TABLE

SERIAL INPUTS A AND B

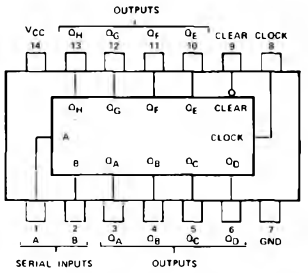
INPUTS $AT t_n$		OUTPUT $AT t_n+1$
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

PIN CONFIGURATIONS

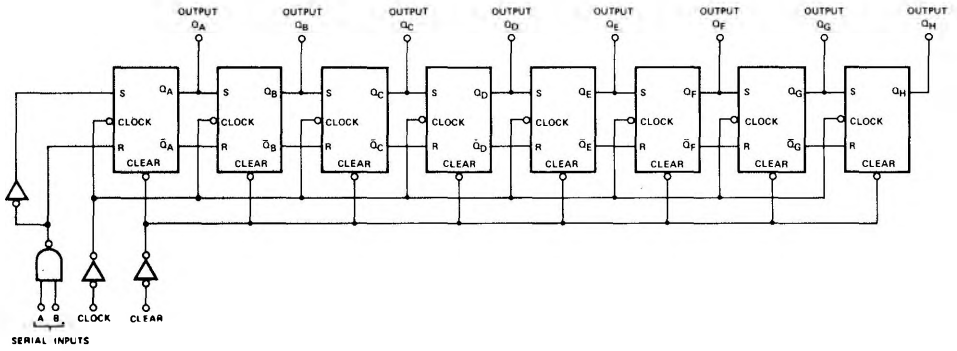
W PACKAGE



A,F PACKAGE



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54164			N74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			10			10	
Low logic level			5			5	
Input Clock Frequency, f_{clock}	0		25	0		25	MHz
Width of Clock or Clear Input Pulse, t_w	20			20			ns
Data Setup Time, t_{setup}	15			15			ns
Data Hold Time, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		S54164			N74164			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = -12mA			-1.5			-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = -400μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 8mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			-1.6			-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		-10		-27.5	-9		-27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note	$V_{I(clock)}$ = 0.4V		30			30		mA
			$V_{I(clock)}$ = 2.4V		37	54		37	54	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input	C_L = 15pF		24	36	ns
		C_L = 50pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input	C_L = 15pF	8	17	27	ns
		C_L = 50pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input	C_L = 15pF	10	21	32	ns
		C_L = 50pF	10	25	37	

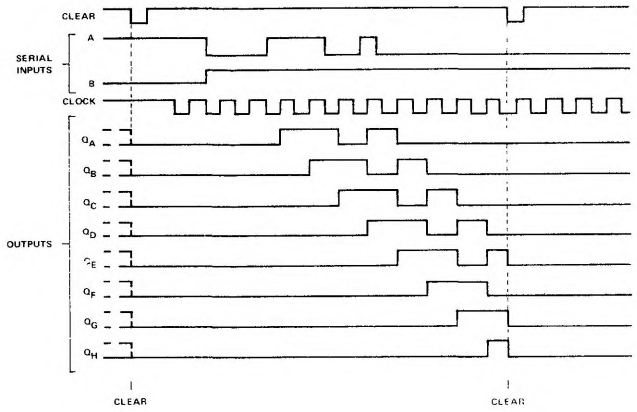
* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

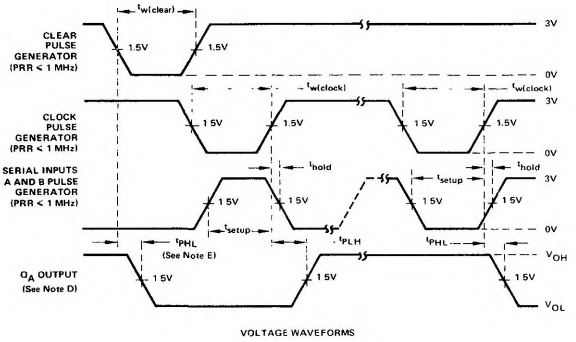
† Not more than two outputs should be shorted at a time.

NOTE : I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5V, applied to clear.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:
A. The pulse generators have the following characteristics: $t_r \leq 10ns$, $t_f \leq 10ns$, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.