DESCRIPTION

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the 8 bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

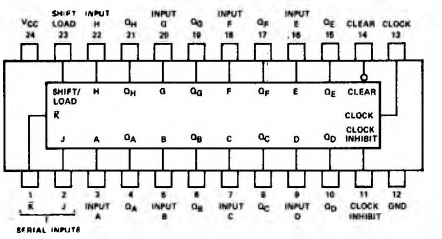
Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-K inputs. See the J-K inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

PIN CONFIGURATIONS

N,F,Q PACKAGES



†Pin assignments for these circuits are the same for packages.

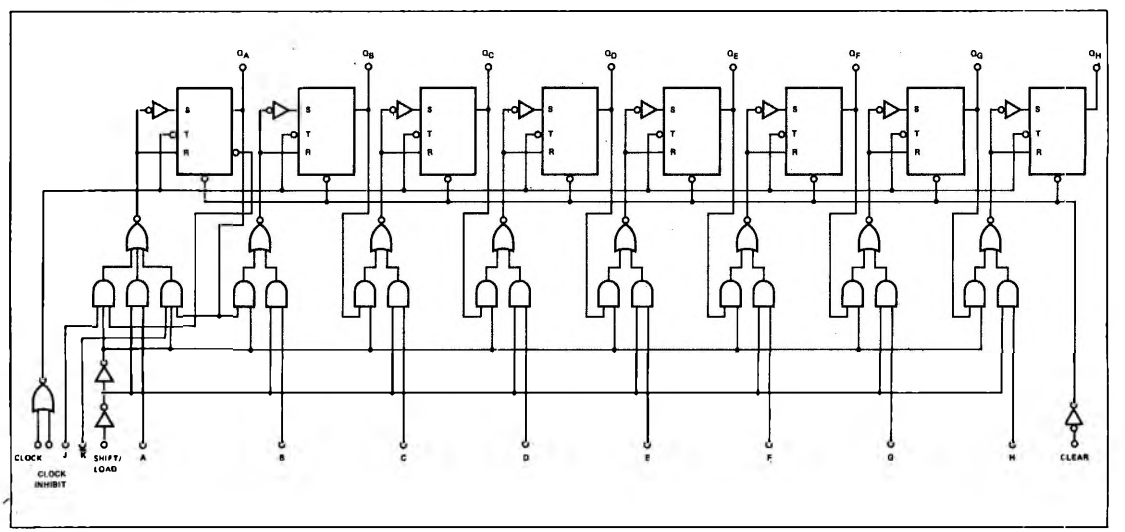
TRUTH TABLE

INPUTS at t_n		OUTPUT t_{n+1}
J	$\overline{R}$	Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

H - high level, L = low level

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

	S54199			N74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out From each output, N: High logic level			20			20	
Low logic level			10			10	
Input Count Frequency, f_{count}	0		25	0		25	MHz
Width of Clock or Clear Pulse, t_w	20			20			ns
Mode-Control Setup Time, t_{setup}	30			30			ns
Data Setup Time, t_{setup}	20			20			ns
Hold Time at any Input, t_{hold}	0			0			ns
Operating Free-Air Temperature, T_A	−55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *		S54199			N74199			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OH} = −800μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V,	V_{IH} = 2V, I_{OL} = 16mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current†	V_{CC} = MAX		−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	Table Below		72	104		72	116	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15pF, R_L = 400Ω	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

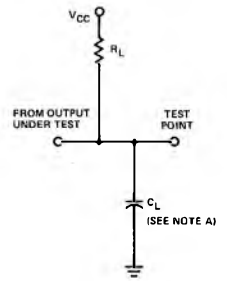
TEST CONDITIONS FOR I_{CC} (all outputs are open)

TYPE	APPLY 4.5V	FIRST GROUND, THEN APPLY 4.5V	GROUND
S54199, N74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

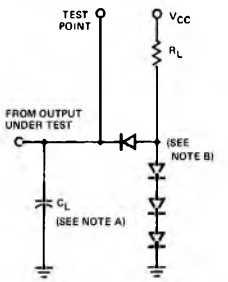
54/74 And 54/74H Typical A.C. Loads And Waveforms

PARAMETER MEASUREMENT INFORMATION

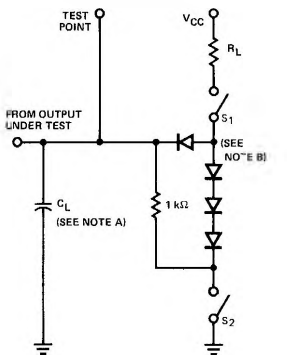
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



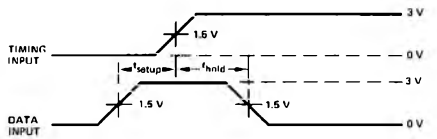
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



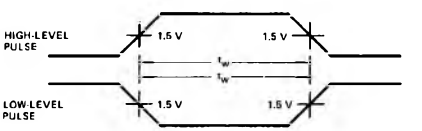
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

TYPICAL AC WAVEFORMS

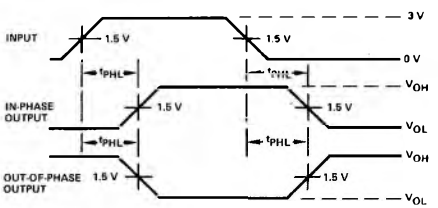
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



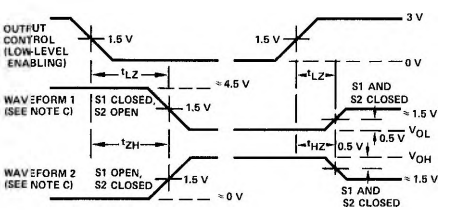
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.