

EXCESS 3-TO-DECIMAL DECODER

S5443 N7443

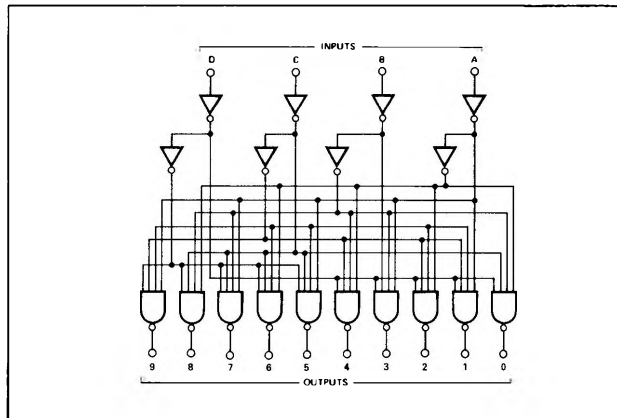
S5443—B,F,W • N7443—B

DIGITAL 54/74 TTL SERIES

DESCRIPTION

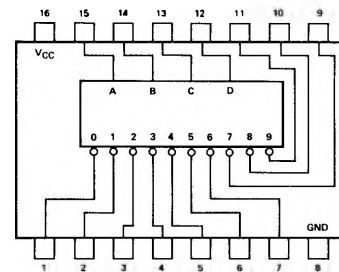
The 54/7443 Excess 3 Code to Decimal Decoder is a TTL MSI array utilized in decoding and logic conversion application. The 54/7443 decodes excess 3 code numbers to one of ten outputs.

LOGIC DIAGRAM



PIN CONFIGURATIONS

B,F,W PACKAGE



TRUTH TABLE

S5443/N7443
EXCESS
INPUT

D	C	B	A
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0

ALL TYPES
DECIMAL
OUTPUT

0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S5443 Circuits	4.5	5	5.5	V
N7443 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output, N			10	

SIGNETICS DIGITAL 54/74 TTL SERIES - S5443 • N7443
ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS *	MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$			0.8	V
$V_{out(1)}$	Logical 1 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2\text{V}$, $V_{in(0)} = 0.8\text{V}$, $I_{load} = -400\mu\text{A}$	2.4			V
$V_{out(0)}$	Logical 0 output voltage	$V_{CC} = \text{MIN}$, $V_{in(1)} = 2\text{V}$, $V_{in(0)} = 0.8\text{V}$, $I_{sink} = 16\text{mA}$			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$			40	μA
		$V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-1.6	mA
I_{OS}	Short-circuit output current †	$V_{CC} = \text{MAX}$, S5443	-20		-55	mA
		N7443	-18		-55	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, S5443		28	41	mA
		N7443		28	56	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, $N = 10$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	$C_L = 15\text{pF}$, $R_L = 400\Omega$		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	$C_L = 15\text{pF}$, $R_L = 400\Omega$	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	$C_L = 15\text{pF}$, $R_L = 400\Omega$		26	35	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions of the applicable device type.

** All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

† Not more than one output should be shorted at a time.