DUAL J-K MASTER-SLAVE FLIP-FLOP WITH PRESET AND CLEAR S5476-B, F,W • N7476-B, F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

The S5476B/N7476B J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

- 1. Isolate slave from master
- 2. Enter information from J and K inputs to master
- 3. Disable J and K inputs
- 4. Transfer information from master to slave.

TRUTH TABLE





CLOCK WAVEFORM

PIN CONFIGURATIONS



POSITIVE LOGIC

Low input to preset sets Q to logical 1 Low input to clear sets Q to logical 0 Clear and preset are independent from clock

SCHEMATIC (each flip-flop)



SIGNETICS DIGITAL 54/74 TTL SERIES S5476 • N7476

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V _{CC} : S5476 Circuits	4.5	5	5.5	v
N7476 Circuits	4.75	5	5.25	V V
Operating Free-Air Temperature Range, TA: S5476 Circuits	-55	25	125	°c
N7476 Circuits	0	25	70	°C
Normalized Fanout from each Output, N			10	
Width of Clock Pulse, tp(clock)	20			ns
Width of Preset Pulse, tp(preset)	25			ns
Width of Clear Pulse, tp(clear)	25	1		ns
Input Setup Time, tsetup	≥ ^t p(clock)			
Input Hold Time, thold	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*		MIN	TYP**	МАХ	UNIT	
Vin(1)	Input voltage required to ensure logical 1 at any input terminal	V _{CC} = MIN			2			v
V _{in(0)}	Input voltage required to ensure logical 0 at any input terminal	V _{CC} = MIN					0.8	v
V _{out(1)}	Logical 1 output voltage	V _{CC} = MIN,	$I_{load} = -400 \mu A$		2.4	3.5		V V
V _{out(0)}	Logical 0 output voltage	V _{CC} = MIN,	I _{sink} = 16mA			0.22	0.4	v
l _{in(0)}	Logical 0 level input current at J or K	V _{CC} = MAX,	V _{in} = 0.4V				-1.6	mA
[†] in(0)	Logical O level input current at clear, preset, or clock	V _{CC} = MAX,	V _{in} = 0.4V				-3.2	mA
lin(1)	Logical 1 level input current at J or K	V _{CC} = MAX, V _{CC} = MAX,					40 1	μA mA
lin(1)	Logical 1 level input current at clear, preset, or clock	V _{CC} = MAX, V _{CC} = MAX,	V _{in} = 2.4V V _{in} = 5.5V				80 1	μA mA
los	Short circuit output current [†]	V _{CC} = MAX,	V _{in} = 0	S5476 N7476	-20 -18		-57 -57	mA
'cc	Supply current (each flip-flop)	V _{CC} = MAX,	V _{in} = 5V			20	40	mA

SWITCHING CHARACTERISTICS, V_{cc} = 5V, $\ T_{A}$ = 25°C, $\ N$ = 10

PARAMETER		TEST CONDITIONS		MIN	түр	MAX	
fclock	Maximum clock frequency	C _L = 15pF,	R _L = 400Ω	15	20	-	MHz
^t pd1	Propagation delay time to logical 0 level from clear or preset to output	С _L = 15рF,	R _L = 400Ω		16	25	ns
^t pd0	Propagation delay time to logical 1 level from clear or preset to output	С _L = 15pF,	R _L = 400Ω		25	40	ns
^t pd1	Propagation delay time to logical 1 level from clock to output	С _L = 15рF,	RL = 400Ω	10	16	25	ns
^t pd0	Propagation delay time to logical 0 level from clock to output	С _L = 15pF,	R _L = 400\$2	10	25	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. • All typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$. † Not more than one output should be shorted at a time.