

N7448-B,W

DIGITAL 54/74 TTL SERIES

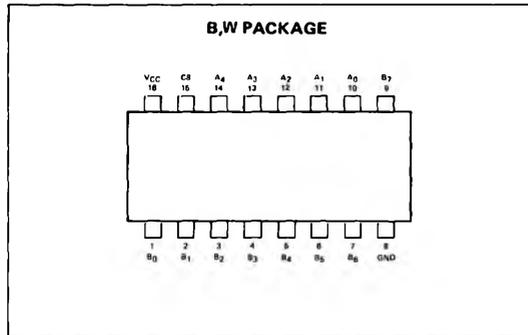
DESCRIPTION

The 7488 is a TTL 256-Bit Read Only Memory organized as 32 word with 8 bits per word. The words are selected by five binary address lines with full word decoding incorporated on the chip. A Chip Select input is provided for additional decoding flexibility, which will cause all eight outputs to go to the high state when the Chip Select input is taken high.

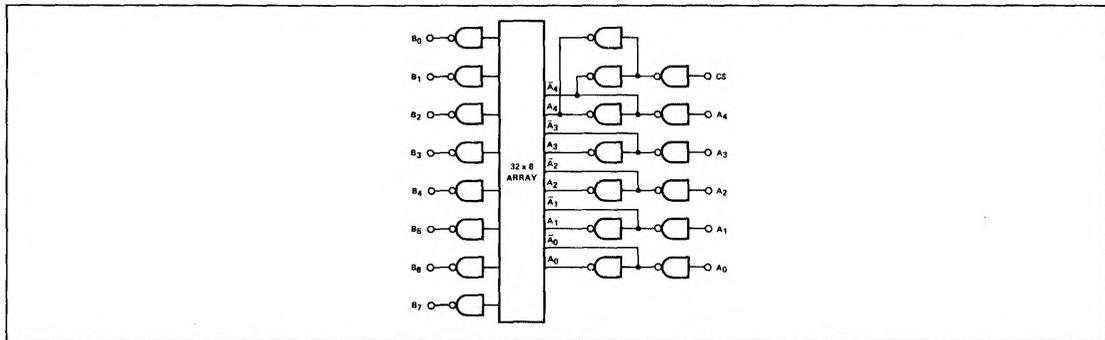
This device is fully TTL or DTL compatible. The outputs are uncommitted collectors, which allows wired-OR operation with the outputs of other TTL or DTL devices. These outputs are capable of sinking twelve standard DCL loads. Propagation delay time is 50ns maximum. Power dissipation is 310 milliwatts with 400 milliwatts maximum.

Customer may specify patterns for the 256-Bit Read Only Memory by completing the truth table/order blank.

PIN CONFIGURATIONS



LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<p>See 8223 or 8224 Data Sheet for Pin-for-Pin Replacement</p>					

256-BIT READ ONLY MEMORIES TRUTH TABLE/ORDER BLANK

CUSTOMER: _____							THIS PORTION TO BE COMPLETED BY SIGNETICS							
P.O. NO.: _____							PART NO.: _____							
YOUR PART NO.: _____							S.D. NO.: _____							
DATE: _____							DATE RECEIVED: _____							
WORD	INPUTS						OUTPUTS							
	A ₄	A ₃	A ₂	A ₁	A ₀	ENABLE	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
ALL	X	X	X	X	X	1	1	1	1	1	1	1	1	1