DESCRIPTION

The S5491/N7491 is a monolithic serial-in, serial-out 8-bit shift register utilizing high-speed transistor-transistor logic (TTL) circuits. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the S5491/N7491 to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the S5470/N7470 flip-flop and the S5474/N7474 dual D-type flip-flop.

TRUTH TABLE

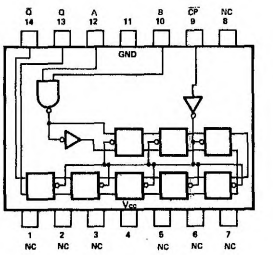
LOGIC

t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

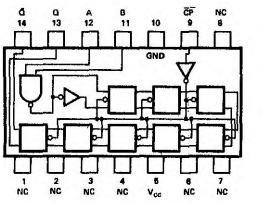
NOTES:
1. t_n = bit time before clock pulse.
2. t_{n+8} = bit time after 8 clock pulse.

PIN CONFIGURATIONS

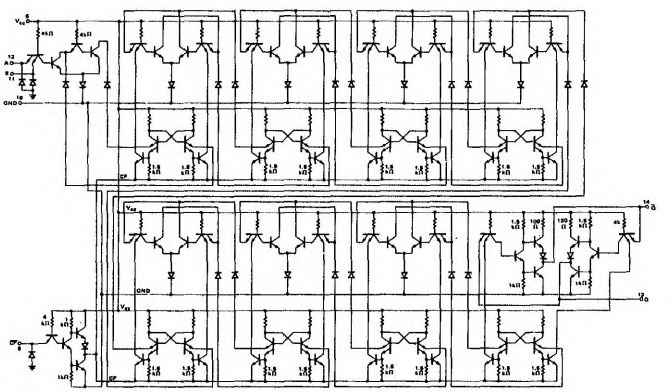
W PACKAGE



A,F PACKAGE



SCHEMATIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: S5491 Circuits		4.5	5	5.5	V
N7491 Circuits		4.75	5	5.25	V
Normalized Fan-Out from each Output, N				10	
Operating Free-Air Temperature Range, T_A:	S5491 Circuits	-55	25	125	°C
	N7491 Circuits	0	25	70	°C
Width of Clock Pulse, $t_{p(clock)}$		25			ns
Input Setup Time, t_{setup}		25			ns
Input Hold Time, t_{hold}		0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			MIN	TYP**	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN,	I_{load} = −400μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN,	I_{sink} = 16mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX,	V_{in} = 0.4V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX,	V_{in} = 2.4V				40	μA
		V_{CC} = MAX,	V_{in} = 5.5V				1	mA
I_{OS}	Short circuit output current †	V_{CC} = MAX,	V_{out} = 0	S5491	−20		−57	mA
				N7491	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	V_{in} = 4.5V	S5491		35	50	mA
				N7491		35	58	mA

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	C_L = 15pF,	R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15pF,	R_L = 400Ω		24	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15pF,	R_L = 400Ω		27	40	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
** All typical values are at V_{CC} = 5V, T_A = 25°C.
† Not more than one output should be shorted at a time.