

### DESCRIPTION

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

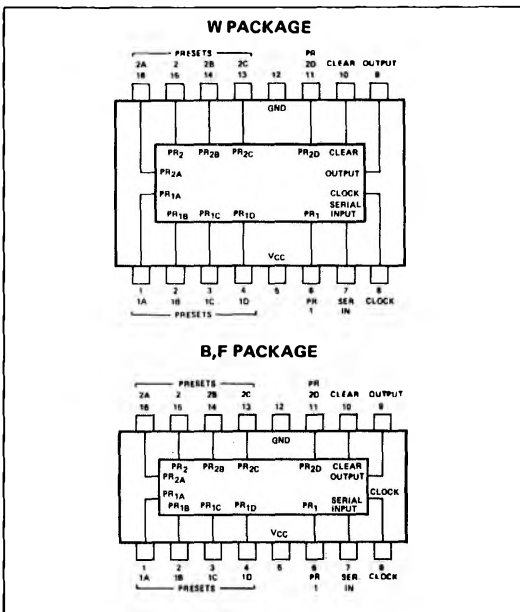
All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

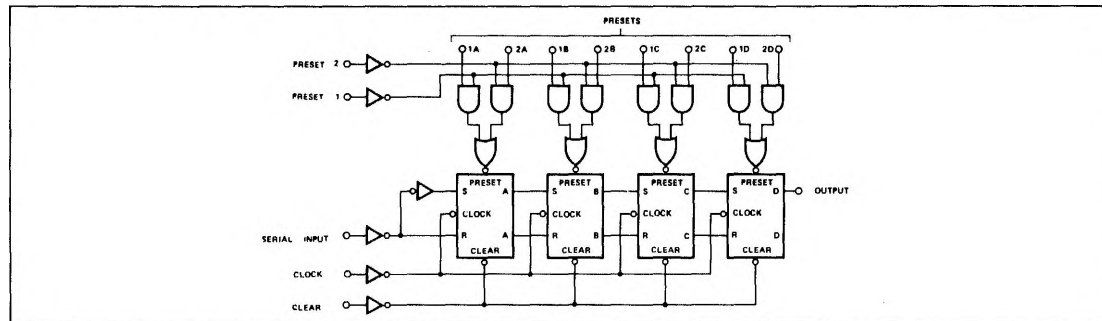
Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The output of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

### PIN CONFIGURATIONS



### LOGIC DIAGRAM



### RECOMMENDED OPERATING CONDITIONS

|                                         | MIN  | TYP | MAX  | UNIT |
|-----------------------------------------|------|-----|------|------|
| Supply Voltage $V_{CC}$                 | 4.5  | 5   | 5.5  | V    |
|                                         | 4.75 | 5   | 5.25 | V    |
| Normalized Fan-Out From Each Output     |      |     | 10   |      |
| Width of Clock Pulse, $t_{p(clock)}$    | 35   |     |      | ns   |
| Width of Clear Pulse, $t_{p(clear)}$    | 30   |     |      | ns   |
| Width of Preset Pulse, $t_{p(preset)}$  | 30   |     |      | ns   |
| Serial Input Setup Time: $t_{setup(1)}$ | 35   |     |      | ns   |
| $t_{setup(0)}$                          | 25   |     |      | ns   |
| Serial Input Hold Time, $t_{hold}$      | 0    |     |      |      |

## ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

| PARAMETER    |                                                                         | TEST CONDITIONS*                               | MIN | TYP** | MAX  | UNIT    |
|--------------|-------------------------------------------------------------------------|------------------------------------------------|-----|-------|------|---------|
| $V_{in(1)}$  | input voltage required to ensure logical 1 at any input terminal        | $V_{CC} = \text{MIN}$                          | 2   |       |      | V       |
| $V_{in(0)}$  | Input voltage required to ensure logical 0 at any input terminal        | $V_{CC} = \text{MIN}$                          |     |       | 0.8  | V       |
| $V_{out(1)}$ | Logical 1 output voltage                                                | $V_{CC} = \text{MIN}, I_{load} = -400 \mu A$   | 2.4 | 3.5   |      | V       |
| $V_{out(0)}$ | Logical 0 output voltage                                                | $V_{CC} = \text{MIN}, I_{sink} = 16 \text{mA}$ |     | 0.22  | 0.4  | V       |
| $I_{in(1)}$  | Logical 1 level input current at any input except preset 1 and preset 2 | $V_{CC} = \text{MAX}, V_{in} = 2.4 \text{V}$   |     |       | 40   | $\mu A$ |
|              |                                                                         | $V_{CC} = \text{MAX}, V_{in} = 5.5 \text{V}$   |     |       | 1    | mA      |
| $I_{in(1)}$  | Logical 1 level input current at preset 1 and preset 2                  | $V_{CC} = \text{MAX}, V_{in} = 2.4 \text{V}$   |     |       | 160  | $\mu A$ |
|              |                                                                         | $V_{CC} = \text{MAX}, V_{in} = 5.5 \text{V}$   |     |       | 1    | mA      |
| $I_{in(0)}$  | Logical 0 level input current at any input except preset 1 and preset 2 | $V_{CC} = \text{MAX}, V_{in} = 0.4 \text{V}$   |     |       | -1.6 | mA      |
|              |                                                                         |                                                |     |       |      |         |
| $I_{in(0)}$  | Logical 0 level input current at preset 1 and preset 2                  | $V_{CC} = \text{MAX}, V_{in} = 0.4 \text{V}$   |     |       | -6.4 | mA      |
|              |                                                                         |                                                |     |       |      |         |
| $I_{OS}$     | Short-circuit input current†                                            | $V_{CC} = \text{MAX}, V_{out} = 0$ S5494       | -20 |       | -57  | mA      |
|              |                                                                         | N7494                                          | -18 |       | -57  | mA      |
| $I_{CC}$     | Supply current                                                          | S5494                                          |     | 35    | 50   | mA      |
|              |                                                                         | N7494                                          |     | 35    | 58   | mA      |

SWITCHING CHARACTERISTICS,  $V_{CC} = 5 \text{V}$ ,  $T_A = 25^\circ \text{C}$ ,  $N = 10$ 

| PARAMETER |                                                                          | TEST CONDITIONS      |                    | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------------------------------------------|----------------------|--------------------|-----|-----|-----|------|
| $f_{max}$ | Maximum clock frequency                                                  | $C_L = 15 \text{pF}$ | $R_L = 400 \Omega$ | 10  |     |     | MHz  |
| $t_{pd1}$ | Propagation delay time to logical 1 level from clock to output to output | $C_L = 15 \text{pF}$ | $R_L = 400 \Omega$ |     | 25  | 40  | ns   |
|           | Propagation delay time to logical 0 level from clock to output           | $C_L = 15 \text{pF}$ | $R_L = 400 \Omega$ |     | 25  | 40  | ns   |
| $t_{pd1}$ | Propagation delay time to logical 1 level from preset to output          | $C_L = 15 \text{pF}$ | $R_L = 400 \Omega$ |     |     | 35  | ns   |
|           | Propagation delay time to logical 0 level from clear to output           | $C_L = 15 \text{pF}$ | $R_L = 400 \Omega$ |     |     | 40  | ns   |

\* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.

\*\* All typical values are at  $V_{CC} = 5 \text{V}$ ,  $T_A = 25^\circ \text{C}$ .

† Not more than one output should be shorted at a time.