

J-K MASTER-SLAVE FLIP-FLOP

S54H72 N74H72

S54H72-A,F,W • N74H72-A,F

DIGITAL 54/74 TTL SERIES

DESCRIPTION

These J-K flip-flops are based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state

TRUTH TABLE

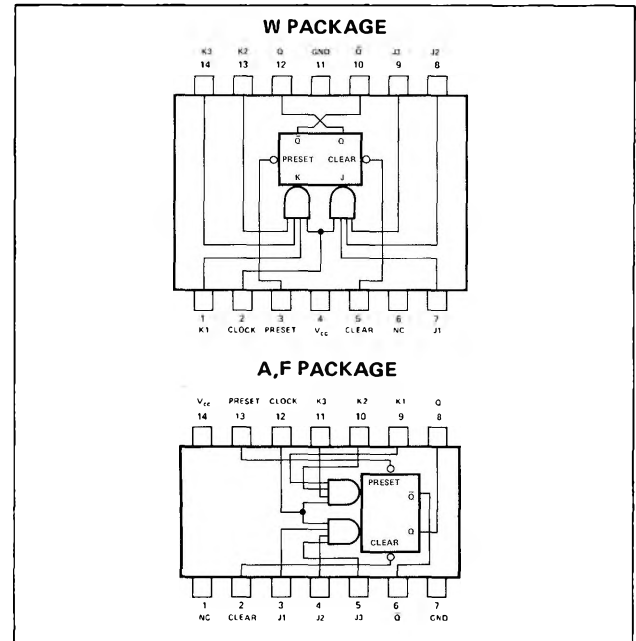
LOGIC

(Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

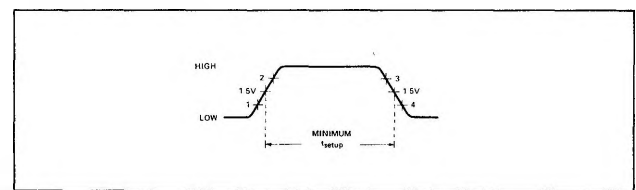
NOTES:

1. $J = J_1 \cdot J_2 \cdot J_3$
2. $K = K_1 \cdot K_2 \cdot K_3$
3. t_n = bit time before clock pulse
4. t_{n+1} = bit time after clock pulse.

PIN CONFIGURATIONS



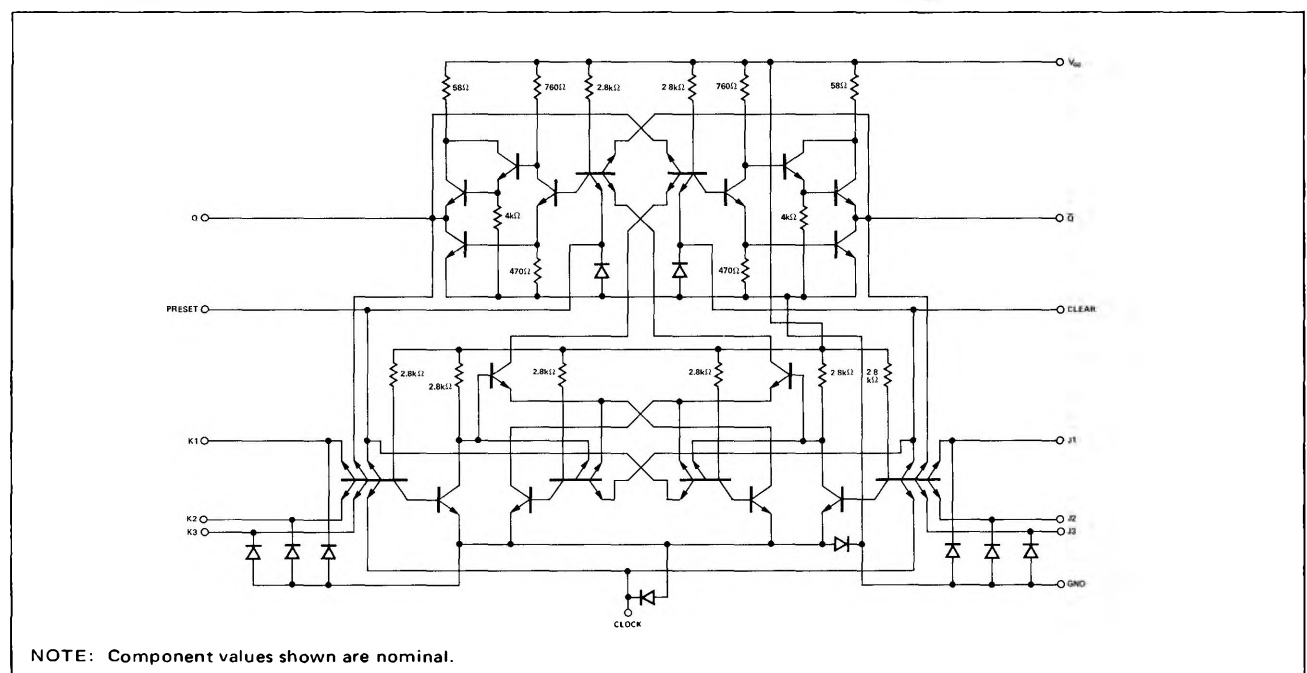
CLOCK WAVEFORM



POSITIVE LOGIC

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

SCHEMATIC DIAGRAM



NOTE: Component values shown are nominal.

SIGNETICS DIGITAL 54/74 TTL SERIES — S54H72 • N74H72
RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} : S54H72 Circuits	4.5	5	5.5	V
N74H72 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A : S54H72 Circuits	-55	25	125	°C
N74H72 Circuits	0	25	70	°C
Normalized Fan-Out from each Output, N			10	
Width of Clock Pulse, $t_{p(\text{clock})}$	12			ns
Width of Preset Pulse, $t_{p(\text{preset})}$	16			ns
Width of Clear Pulse, $t_{p(\text{clear})}$	16			ns
Input Setup Time, t_{setup} (See above)	$\geq t_{p(\text{clock})}$			
Input Hold Time, t_{hold}	0			

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS *	MIN	TYP†	MAX	UNIT
$V_{in(1)}$ Input voltage required to ensure logical 1 at any input terminal	$V_{CC} = \text{MIN}$	2			V
$V_{in(0)}$ Input voltage required to ensure logical 0 at any input terminal	$V_{CC} = \text{MIN}$,			0.8	V
$V_{out(1)}$ Logical 1 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{load}} = -500\mu\text{A}$	2.4			V
$V_{out(0)}$ Logical 0 output voltage	$V_{CC} = \text{MIN}$, $I_{\text{sink}} = 20\text{mA}$			0.4	V
$I_{in(0)}$ Logical 0 level input current at J1, J2, J3, K1, K2, K3, or clock	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-2	mA
$I_{in(0)}$ Logical 0 level input current at preset or clear	$V_{CC} = \text{MAX}$, $V_{in} = 0.4\text{V}$			-4	mA
$I_{in(1)}$ Logical 1 level input current at J1, J2, J3, K1, K2, or K3	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			50 1	μA mA
$I_{in(1)}$ Logical 1 level input current at clock	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			50 1	μA mA
$I_{in(1)}$ Logical 1 level input current at preset or clear	$V_{CC} = \text{MAX}$, $V_{in} = 2.4\text{V}$ $V_{CC} = \text{MAX}$, $V_{in} = 5.5\text{V}$			100 1	μA mA
I_{OS} Short circuit output current**	$V_{CC} = \text{MAX}$, $V_{in} = 0$	-40		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$,		16	25	mA

SWITCHING CHARACTERISTICS, $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$, N = 10

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock} Maximum clock frequency	$C_L = 25\text{pF}$, $R_L = 280\Omega$	25	30		MHz
t_{pd1} Propagation delay time to logical 1 level from clear or preset to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		6	13	ns
t_{pd0} Propagation delay time to logical 0 level from clear or preset to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		12	24	ns
t_{pd1} Propagation delay time to logical 1 level from clock to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		16	21	ns
t_{pd0} Propagation delay time to logical 0 level from clock to output	$C_L = 25\text{pF}$, $R_L = 280\Omega$		22	27	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** Not more than one output should be shorted at a time, and duration of short circuit test should not exceed 1 second.

† All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.