signetics

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DIGITAL 54/74 TTL SERIES

S54S257
S54S258
N74S257
N74S258

DESCRIPTION

These Schottky-clamped high-performance multiplexers feature three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

The typical propagation delay times from data input to output average only 4.8 nanoseconds for the S54S257, N74S157 and only 4 nanoseconds for the S54S258, N74S258. Also, to minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

FEATURES

- **TRI-STATE OUTPUTS INTERFACE DIRECTLY WITH SYSTEM BUS**
- **SCHOTTKY-CLAMPED FOR SIGNIFICANT IMPROVEMENT IN A-C PERFORMANCE**
- **FULLY COMPATIBLE WITH MOST TTL FUNCTIONS INCLUDING MSI**
- **SAME PIN ASSIGNMENTS AS S54S157, N74S157 AND S54S158, N74S158**
- **PROVIDES BUS INTERFACE FROM MULTIPLE SOURCES IN HIGH-PERFORMANCE SYSTEMS**
- **N54S257 AND N54S258 ARE GUARANTEED FOR OPERATION OVER THE FULL MILITARY TEMPERATURE RANGE OF −55°C TO 125°C**

FUNCTION TABLE

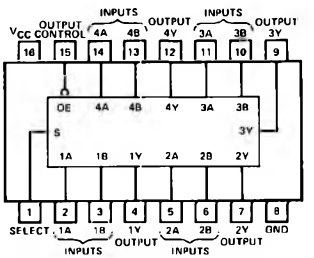
INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	N54S257 S74S257	N54S258 S74S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)

PIN CONFIGURATION

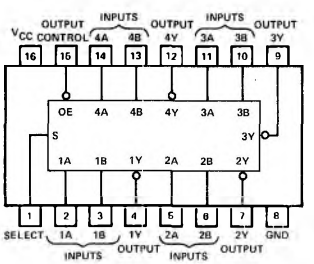
J OR N DUAL IN-LINE OR W FLAT PACKAGE
(TOP VIEW)

S54S257, N74S257



Positive Logic: See function table

S54S258, N74S258



Positive Logic: See function table

RECOMMENDED OPERATING CONDITIONS

		S54S257, S54S258			N74S257, N74S258			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			40			130	
	Low logic level			10			10	
High-level output current, I_{OH}				2			6.5	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER			TEST CONDITIONS*	S54S257, S54S258			N74S257, N74S258			UNIT
				MIN	TYP**	MAX	MIN	TYP**	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, Series 54S	2.5	3.4		2.5	3.4		V
			V_{IL} = 0.8 V, I_{OH} = MAX, Series 74S	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 2.4 V			50			50	µA
			V_{CC} = MAX, V_O = 0.4 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	S input	V_{CC} = MAX, V_I = 2.7 V			100			100	µA
		Any other				50			50	
I_{IL}	Low-level input current	S input	V_{CC} = MAX, V_I = 0.5 V			−4			−4	mA
		Any other				−2			−2	
I_{OS}	Short circuit output current‡		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	All outputs high	V_{CC} = MAX, See Note 1		44	68		36	56	mA
		All outputs low			60	93		52	81	
		All outputs off			64	99		56	87	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
**All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time and duration of the short circuit test should not exceed one second.
NOTE 1: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

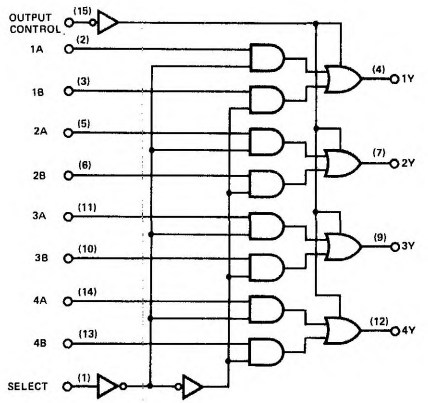
SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	S54S257, N74S257			S54S258, N74S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	Any	C_L = 15 pF, R_L = 280 Ω, See Note 4		5	7.5		4	6	ns
t_{PHL}					4.5	6.5		4	6	
t_{PLH}	Select	Any			8.5			8	12	ns
t_{PHL}					8.5			7.5	12	
t_{ZH}	Output	Any			13	19.5		13	19.5	ns
t_{ZL}	Control				14	21		14	21	
t_{HZ}	Output	Any	C_L = 5 pF See Note 2		5.5	8.5		5.5	8.5	ns
t_{LZ}	Control				9	14		9	14	

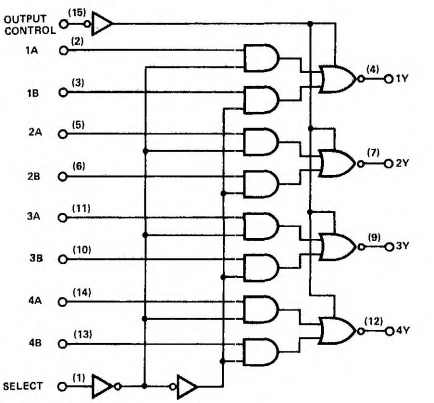
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: Load circuit and waveforms are shown on page 2-293

FUNCTIONAL BLOCK DIAGRAMS

S54S257, N74S257



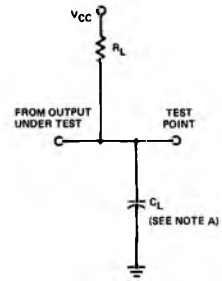
S54S258, N74S258



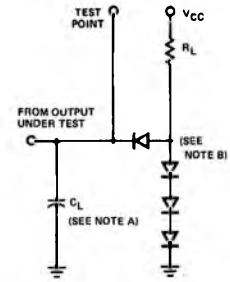
54/74S Typical A.C. Loads And Waveforms

PARAMETER MEASUREMENT INFORMATION

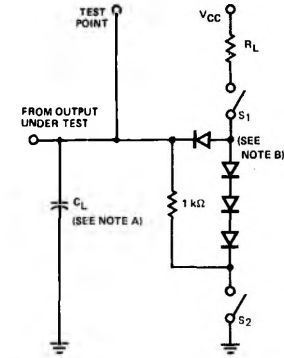
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



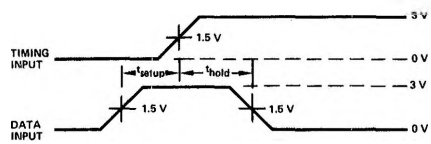
LOAD CIRCUIT FOR TRI-STATE OUTPUTS



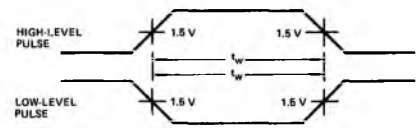
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

TYPICAL AC WAVEFORMS

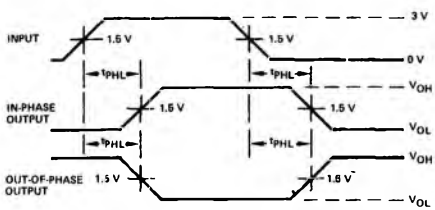
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



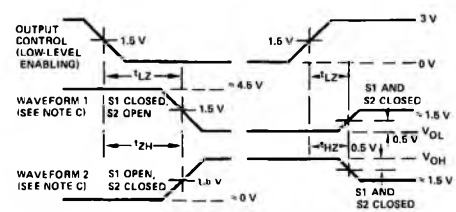
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS



NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR $\leq$ 1 MHz, and $Z_{out} \approx 50\ \Omega$.