NCP45524, NCP45525

Product Preview

ecoSWITCH™

Advanced Load Management

Controlled Load Switch with Low R_{ON}

The NCP4552x series of load switches provide a component and area-reducing solution for efficient power domain switching with inrush current limit via soft start. These devices are designed to integrate control and driver functionality with a high performance low on-resistance power MOSFET in a single package. This cost effective solution is ideal for power management and hot-swap applications requiring low power consumption in a small footprint.

Features

- Advanced Controller with Charge Pump
- Integrated N–Channel MOSFET with Low R_{ON}
- Soft-Start via Controlled Slew Rate
- Adjustable Slew Rate Control (NCP45525)
- Power Good Output (NCP45524)
- Input Voltage Range 0.5 V to 13.5 V
- Extremely Low Standby Current
- Load Bleed Function
- This is a Pb–free Device

Typical Applications

- Notebook and Tablet Computers
- Handheld & Mobile Electronics
- Portable Medical Devices
- Hard Drives & Peripheral Ports

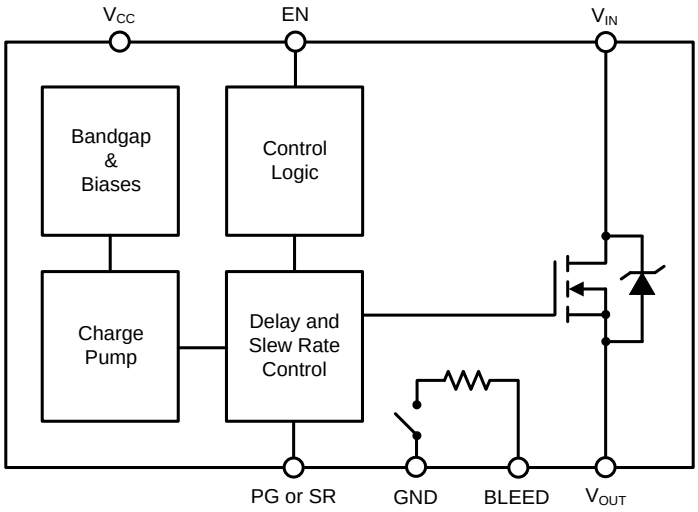

Figure 1. Block Diagram

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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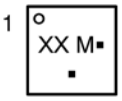
R_{ON} TYP	V_{CC}	V_{IN}	I_{MAX}
18.0 mΩ	3.3 V	1.8 V	6 A
18.8 mΩ	3.3 V	5 V	
21.9 mΩ	3.3 V	12 V	

DFN8, 2x2
CASE 506CC

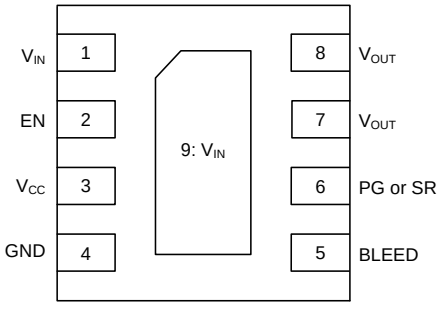
MARKING DIAGRAM



XX = 4H for NCP45524-H
= 4L for NCP45524-L
= 5H for NCP45525-H
= 5L for NCP45525-L
M = Date Code
▪ = Pb–Free Package

(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

Table 1. PIN DESCRIPTION

Pin	Name	Function
1, 9	V_{IN}	Drain of MOSFET (0.5 V – 13.5 V), Pin 1 must be connected to Pin 9
2	EN	NCP45524–H & NCP45525–H – Active–high digital input used to turn on the MOSFET, pin has an internal pull down resistor to GND
		NCP45524–L & NCP45525–L – Active–low digital input used to turn on the MOSFET, pin has an internal pull up resistor to V_{CC}
3	V_{CC}	Supply voltage to controller (3.0 V – 5.5 V)
4	GND	Controller ground
5	BLEED	Load bleed connection, must be tied to V_{OUT} either directly or through a resistor (see Applications Information)
6	PG	NCP45524 – Active–high, open–drain output that indicates when the gate of the MOSFET is fully driven, external pull up resistor ≥ 1 kΩ to an external voltage source required
	SR	NCP45525 – Slew rate adjustment
7, 8	V_{OUT}	Source of MOSFET connected to load

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.3 to 6	V
Input Voltage Range	V_{IN}	-0.3 to 18	V
Output Voltage Range	V_{OUT}	-0.3 to 18	V
EN Digital Input Range	V_{EN}	-0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 1)	V_{PG}	-0.3 to 6	V
Thermal Resistance, Junction-to-Air (Note 2)	$R_{\theta JA}$	40.0	°C/W
Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	72.7	°C/W
Thermal Resistance, Junction-to-Case (V_{IN} Paddle)	$R_{\theta JC}$	5.3	°C/W
Continuous MOSFET Current @ T_A = 25°C	I_{MAX}	6	A
Total Power Dissipation @ T_A = 25°C (Notes 2 and 4) Derate above T_A = 25°C	P_D	2.50 24.9	W mW/°C
Total Power Dissipation @ T_A = 25°C (Notes 3 and 4) Derate above T_A = 25°C	P_D	1.37 13.8	W mW/°C
Storage Temperature Range	T_{STG}	-40 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Notes 5 and 6)	ESD_{HBM}	2.0	kV
ESD Capability, Charged Device Model (Note 5)	ESD_{CDM}	1.0	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. NCP45524 only. PG is an open-drain output that requires an external pull up resistor ≥ 1 kΩ to an external voltage source.
2. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
3. Surface-mounted on FR4 board using the minimum recommended pad size, 1 oz Cu.
4. Specified for derating purposes only, ensure that I_{MAX} is never exceeded.
5. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
   ESD Charged Device Model per JESD22-C101
6. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3	5.5	V
Input Voltage	V_{IN}	0.5	13.5	V
Ground	GND		0	V
Ambient Temperature	T_A	-40	85	°C
Junction Temperature	T_J	-40	125	°C

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Conditions (Note 7)	Symbol	Min	Typ	Max	Unit
MOSFET						
On-Resistance	V_{CC} = 3.3 V; V_{IN} = 1.8 V	R_{ON}		18.0	24.0	mΩ
	V_{CC} = 3.3 V; V_{IN} = 5 V			18.8	25.0	
	V_{CC} = 3.3 V; V_{IN} = 12 V			21.9	31.7	
Leakage Current (Note 8)	V_{EN} = 0 V; V_{IN} = 13.5 V	I_{LEAK}		0.1	1	μA
CONTROLLER						
Supply Standby Current (Note 9)	V_{EN} = 0 V; V_{CC} = 3 V	I_{STBY}		0.65	2	μA
	V_{EN} = 0 V; V_{CC} = 5.5 V			3.2	4.5	
Supply Dynamic Current (Note 10)	V_{EN} = V_{CC} = 3 V; V_{IN} = 12 V	I_{DYN}		180	300	μA
	V_{EN} = V_{CC} = 5.5 V; V_{IN} = 1.8 V			430	680	
Bleed Resistance	V_{EN} = 0 V; V_{CC} = 3 V	R_{BLEED}	86	115	144	Ω
	V_{EN} = 0 V; V_{CC} = 5.5 V		72	97	121	
EN Input High Voltage	V_{CC} = 3 V – 5.5 V	V_{IH}	2			V
EN Input Low Voltage	V_{CC} = 3 V – 5.5 V	V_{IL}			0.8	V
EN Input Leakage Current	NCP45524–H; NCP45525–H; V_{EN} = 0 V	I_{IL}		90	500	nA
	NCP45524–L; NCP45525–L; V_{EN} = V_{CC}	I_{IH}		90	500	
EN Pull Down Resistance	NCP45524–H; NCP45525–H	R_{PD}	76	100	124	kΩ
EN Pull Up Resistance	NCP45524–L; NCP45525–L	R_{PU}	76	100	124	kΩ
PG Output Low Voltage (Note 11)	NCP45524; V_{CC} = 3 V; I_{SINK} = 5 mA	V_{OL}			0.2	V
PG Output Leakage Current (Note 12)	NCP45524; V_{CC} = 3 V; V_{TERM} = 3.3 V	I_{OH}		5	100	nA
Slew Rate Control Constant (Note 13)	NCP45525; V_{CC} = 3 V	K_{SR}	24	31	38	μA

7. V_{EN} shown only for NCP45524–H, NCP45525–H (EN Active–High) unless otherwise specified.
8. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
9. Average current from V_{CC} to GND with MOSFET turned off.
10. Average current from V_{CC} to GND after charge up time of MOSFET.
11. PG is an open-drain output that is pulled low when the MOSFET is disabled.
12. PG is an open-drain output that is not driven when the gate of the MOSFET is fully charged, requires an external pull up resistor ≥ 1 kΩ to an external voltage source, V_{TERM}.
13. See Applications Information section for details on how to adjust the slew rate.

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Note 14)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
V_{CC} = 3.3 V, V_{IN} = 1.8 V						
Output Slew Rate	R_L = 10 Ω, C_L = 0.1 μF	SR		13.1		kV/s
Output Turn-on Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{ON}		230		μs
Output Turn-off Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{OFF}		1.2		μs
V_{CC} = 5.0 V, V_{IN} = 1.8 V						
Output Slew Rate	R_L = 10 Ω, C_L = 0.1 μF	SR		13.4		kV/s
Output Turn-on Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{ON}		195		μs
Output Turn-off Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{OFF}		1.0		μs
V_{CC} = 3.3 V, V_{IN} = 12 V						
Output Slew Rate	R_L = 10 Ω, C_L = 0.1 μF	SR		13.5		kV/s
Output Turn-on Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{ON}		270		μs
Output Turn-off Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{OFF}		0.4		μs
V_{CC} = 5.0 V, V_{IN} = 12 V						
Output Slew Rate	R_L = 10 Ω, C_L = 0.1 μF	SR		13.9		kV/s
Output Turn-on Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{ON}		260		μs
Output Turn-off Delay	R_L = 10 Ω, C_L = 0.1 μF	T_{OFF}		0.2		μs

14. See below figure for Test Circuit and Timing Diagrams.

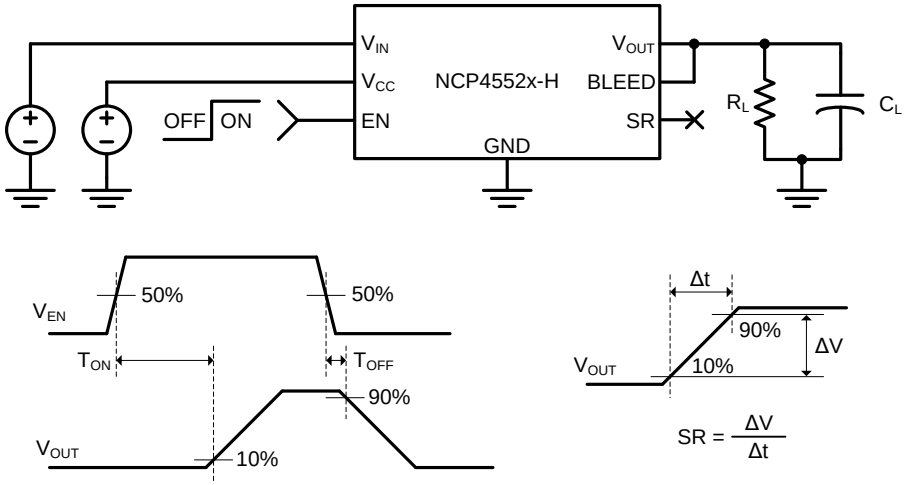


Figure 2. Test Circuit and Timing Diagrams

ORDERING INFORMATION

Device	Pin 6 Functionality	EN Polarity	Package	Shipping†
NCP45524IMNTWG–H	PG	Active–High	DFN8 (Pb–Free)	3000 / Tape & Reel
NCP45524IMNTWG–L	PG	Active–Low		
NCP45525IMNTWG–H	SR	Active–High		
NCP45525IMNTWG–L	SR	Active–Low		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

APPLICATIONS INFORMATION

Enable Control

Both the NCP45524 and the NCP45525 have two part numbers, NCP4552x-H and NCP4552x-L, that only differ in the polarity of the enable control.

The NCP4552x-H parts allow for enabling the MOSFET in an active-high configuration. When the EN pin is at a logic high level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. Similarly, when the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not being driven.

The NCP4552x-L parts allow for enabling the MOSFET in an active-low configuration. When the EN pin is at a logic low level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. Similarly, when the EN pin is at a logic high level, the MOSFET will be disabled. An internal pull up resistor to V_{CC} on the EN pin ensures that the MOSFET will be disabled when not being driven.

Load Bleed

The NCP4552x devices have an on-chip bleed resistor that is used to bleed the charge off of the load to ground after the MOSFET has been disabled. In series with the bleed resistor is a bleed switch that is enabled whenever the MOSFET is disabled. Delays are added to the enable of this switch to ensure that both the MOSFET and the bleed switch are not concurrently active.

In order to realize this functionality, the BLEED pin must be connected to V_{OUT} either directly or through a resistor, R_{EXT}, which should not exceed 1 kΩ.

Power Good

The NCP45524 devices have a power good output (PG) that is used to indicate when the gate of the MOSFET is fully driven. The PG pin is an active-high, open-drain output that requires an external pull up resistor ≥ 1 kΩ to an external voltage source compatible with input levels of other devices connected to this pin. When the power good feature is not used in the application, the PG pin can be tied to ground.

Slew Rate Control

The NCP4552x devices are equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

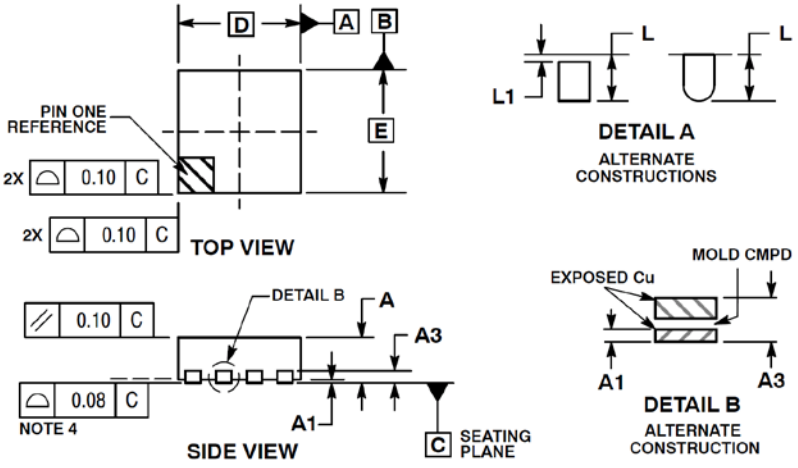
The slew rate of the NCP45525 can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$Slew\ Rate = \frac{K_{SR}}{C_{SR}}\ [V/s]$$

where K_{SR} is the specified slew rate control constant, found in Table 4, and C_{SR} is the slew rate control capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

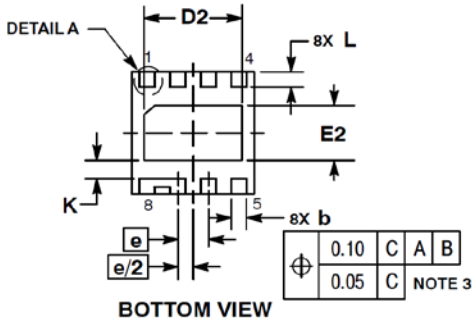
PACKAGE DIMENSIONS

DFN8 2x2, 0.5P
CASE 506CC
ISSUE O

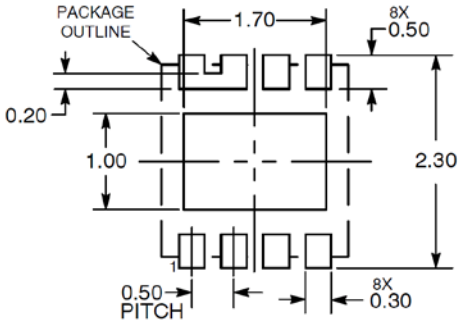


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.50	1.70
E	2.00 BSC	
E2	0.80	1.00
e	0.50 BSC	
K	0.27 REF	
L	0.18	0.38
L1	---	0.15



RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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