NCP552

80 mA CMOS Low Iq NOCAP™ Voltage Regulator

The NCP552 series of fixed output NOCAP linear regulators are designed for handheld communication equipment and portable battery powered applications which require low quiescent. The NCP552 series features an ultra–low quiescent current of 2.8 μA. Each device contains a voltage reference unit, an error amplifier, a PMOS power transistor, resistors for setting output voltage, current limit, and temperature limit protection circuits.

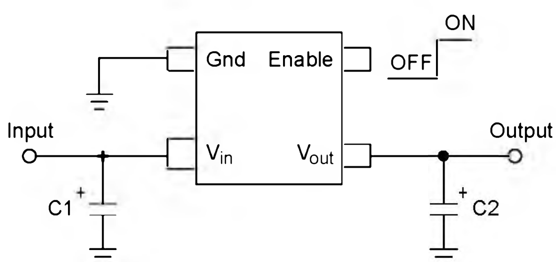
The NCP552 has been designed to be used with low cost ceramic capacitors. This device has the ability to operate without an output capacitor. The device is housed in the micro–miniature SC82–AB surface mount package. Standard voltage versions are 1.5, 1.8, 2.5, 2.7, 2.8, 3.0, 3.3, and 5.0 V. Other voltages are available in 100 mV steps.

Features

- Low Quiescent Current of 2.8 μA Typical
- Low Output Voltage Option
- Output Voltage Accuracy of 2.0%
- Industrial Temperature Range of –40°C to 85°C

Typical Applications

- Battery Powered Consumer Products
- Hand–Held Instruments
- Camcorders and Cameras



This device contains 32 active transistors

Figure 1. Typical Application Diagram

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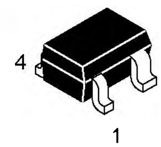
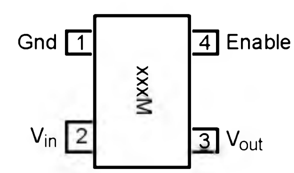


SC82–AB (SC70–4)
SQ SUFFIX
CASE 419C

PIN CONNECTIONS AND MARKING DIAGRAM



(Top View)

xxx = Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 303 of this data sheet.

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	Gnd	Power supply ground.
2	Vin	Positive power supply input voltage.
3	Vout	Regulated output voltage.
4	Enable	This input is used to place the device into low–power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to Vin.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	12	V
Enable Voltage	Enable	–0.3 to V_{in} +0.3	V
Output Voltage	V_{out}	–0.3 to V_{in} +0.3	V
Power Dissipation and Thermal Characteristics Power Dissipation Thermal Resistance, Junction to Ambient	 P_D $R_{\theta JA}$	 Internally Limited 400	 W °C/W
Operating Junction Temperature	T_J	+125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Lead Soldering Temperature @ 260°C	T_{solder}	10	sec

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL–STD–883, Method 3015
   Machine Model Method 200 V
2. Latch up capability (85°C) ±200 mA DC with trigger voltage.

ELECTRICAL CHARACTERISTICS (V_{in} = $V_{out(nom.)}$ + 1.0 V, V_{enable} = V_{in}, C_{in} = 1.0 μF, C_{out} = 1.0 μF, T_J = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_A = 25°C, I_{out} = 10 mA)	V_{out}				V
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.5 V		2.425	2.5	2.575	
2.7 V		2.646	2.7	2.754	
2.8 V		2.744	2.8	2.856	
3.0 V		2.94	3.0	3.06	
3.3 V		3.234	3.3	3.366	
5.0 V		4.900	5.0	5.100	
Output Voltage (T_A = –40°C to 85°C, I_{out} = 10 mA)	V_{out}				V
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.5 V		2.425	2.5	2.575	
2.7 V		2.619	2.7	2.781	
2.8 V		2.716	2.8	2.884	
3.0 V		2.910	3.0	3.09	
3.3 V		3.201	3.3	3.399	
5.0 V		4.900	5.0	5.100	
Line Regulation (V_{in} = V_{out} + 1.0 V to 12 V, I_{out} = 10 mA)	Reg_{line}	–	2.0	4.5	mV/V
Load Regulation (I_{out} = 1.0 mA to 80 mA, V_{in} = V_{out} + 2.0 V)	Reg_{load}	–	0.3	0.8	mV/mA
Output Current (V_{in} = V_{out} + 2.0 V)	$I_{o(nom.)}$				mA
1.5 V, 1.8 V		80	180	–	
2.5 V, 2.7 V, 2.8 V, 3.0 V		80	180	–	
3.3 V,		80	180	–	
5.0 V		80	180	–	
Dropout Voltage (T_A = –40°C to 85°C, I_{out} = 80 mA, Measured at V_{out} –3.0%)	V_{in}–V_{out}				mV
1.5 V		–	1300	1800	
1.8 V		–	1100	1600	
2.5 V		–	800	1400	
2.7 V		–	750	1200	
2.8 V		–	730	1200	
3.0 V		–	680	1000	
3.3 V		–	650	1000	
5.0 V		–	470	1000	
Quiescent Current	I_Q				μA
(Enable Input = 0 V)		–	0.1	1.0	
(Enable Input = V_{in}, I_{out} = 1.0 mA to $I_{o(nom.)}$, V_{in} = V_{out} +2.0 V)		–	2.8	6.0	
Output Short Circuit Current (V_{in} = V_{out} + 2.0 V)	$I_{out(max)}$				mA
1.5 V, 1.8 V		100	230	450	
2.5 V, 2.7 V, 2.8 V, 3.0 V		100	300	450	
3.3 V,		100	300	450	
5.0 V		100	300	450	
Output Voltage Noise (f = 20 Hz to 100 kHz, I_{out} = 10 mA) (C_{out} = 1.0 μF)	V_n	–	90	–	μVrms
Enable Input Threshold Voltage	$V_{th(en)}$				V
(Voltage Increasing, Output Turns On, Logic High)		1.3	–	–	
(Voltage Decreasing, Output Turns Off, Logic Low)		–	–	0.3	
Output Voltage Temperature Coefficient	T_C	–	±100	–	ppm/°C

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3.0% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

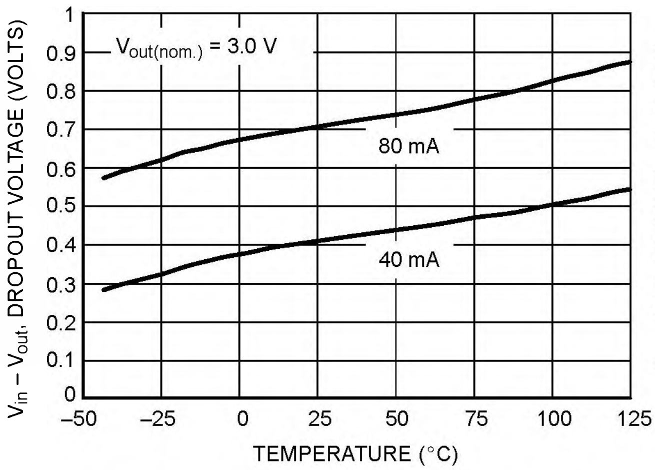


Figure 2. Dropout Voltage versus Temperature

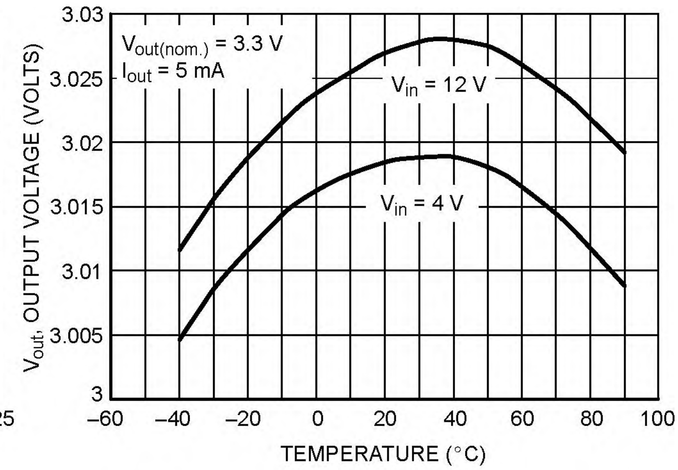


Figure 3. Output Voltage versus Temperature

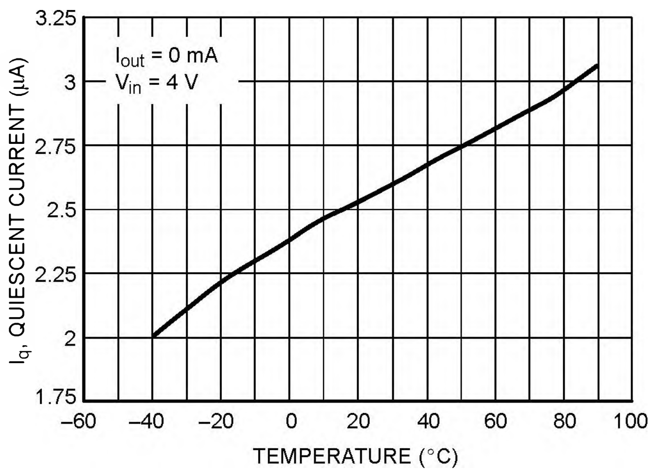


Figure 4. Quiescent Current versus Temperature

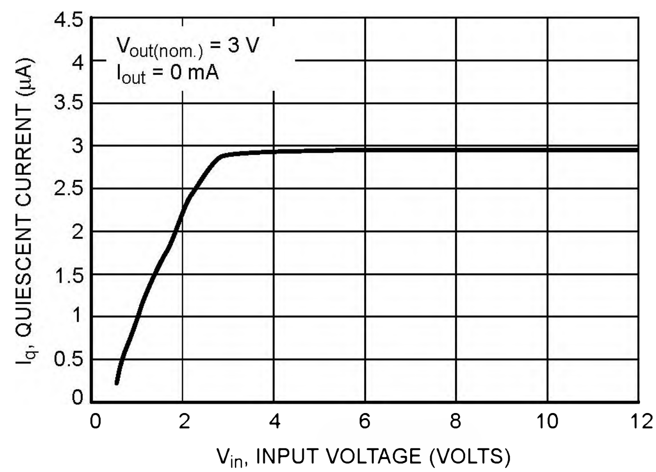


Figure 5. Quiescent Current versus Input Voltage

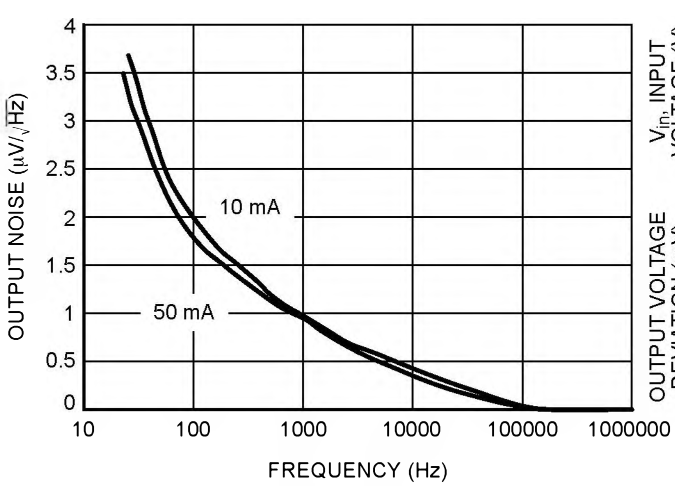


Figure 6. Output Noise Density

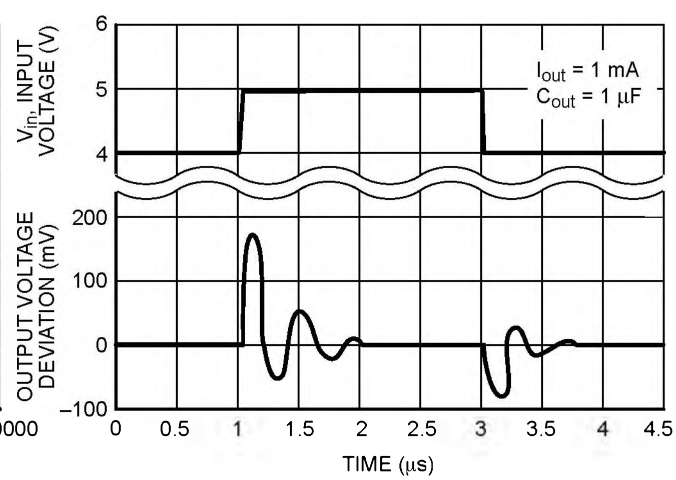


Figure 7. Line Transient Response

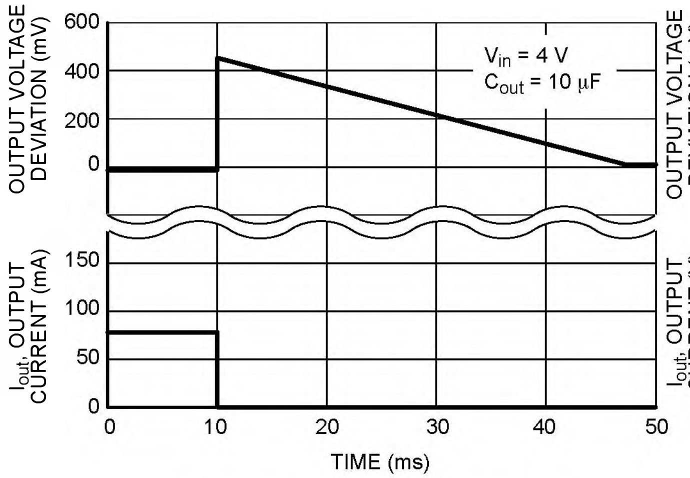


Figure 8. Load Transient Response

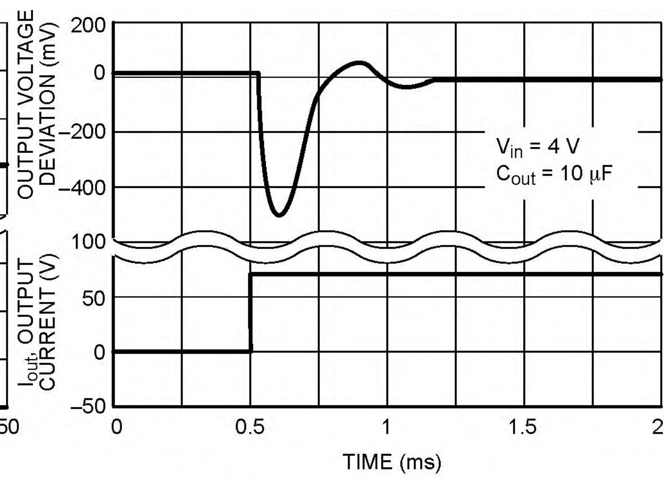


Figure 9. Load Transient Response

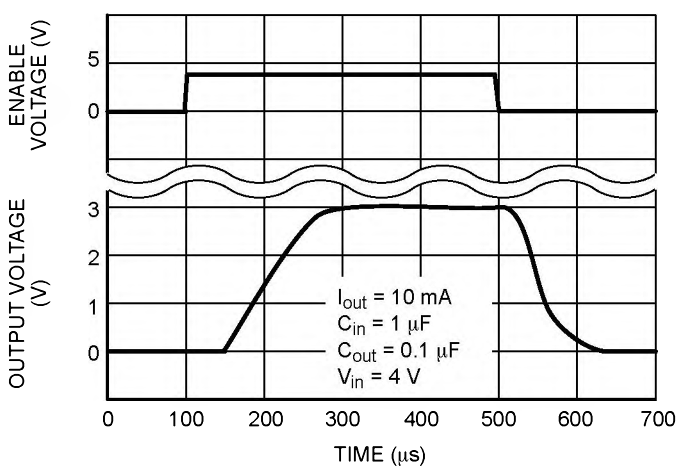


Figure 10. Turn–On Response

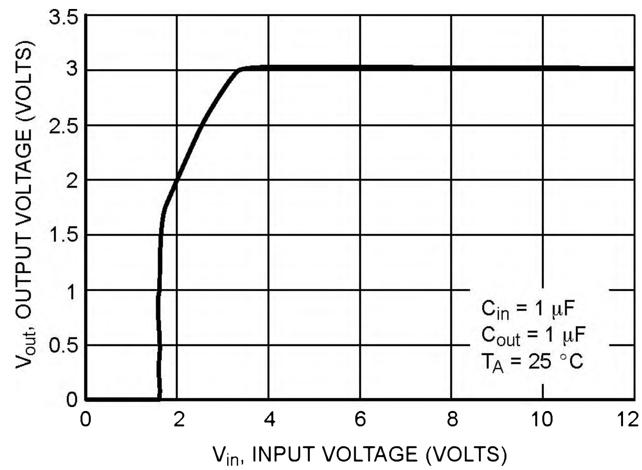


Figure 11. Output Voltage versus Input Voltage

APPLICATIONS INFORMATION

A typical application circuit for the NCP552 series is shown in Figure 1, front page.

Input Decoupling (C1)

A 1.0 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP552 package. Higher values and lower ESR will improve the overall line transient response. If large line or load transients are not expected, then it is possible to operate the regulator without the use of a capacitor.
TDK capacitor: C2012X5R1C105K, or C1608X5R1A105K

Output Decoupling (C2)

The NCP552 is a stable regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. If load transients are not to be expected, then it is possible for the regulator to operate with no output capacitor. Otherwise, capacitors exhibiting ESRs ranging from a few mΩ up to 10 Ω can thus safely be used. The minimum decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.
TDK capacitor: C2012X5R1C105K, C1608X5R1A105K, or C3216X7R1C105K

Enable Operation

The enable pin will turn on the regulator when pulled high and turn off the regulator when pulled low. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}.

Hints

Please be sure the Vin and Gnd lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP552 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP552 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the NCP552 can dissipate up to 250 mW @ 25°C.

The power dissipated by the NCP552 can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd}(I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

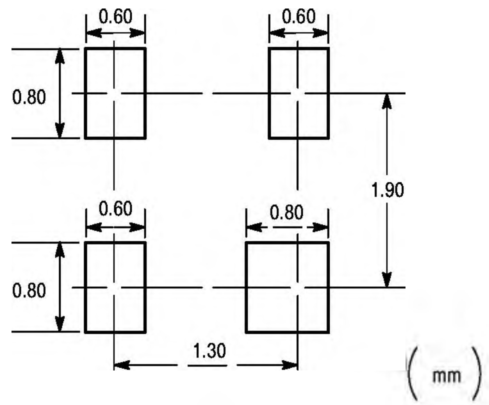
$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{gnd} + I_{out}}$$

If an 80 mA output current is needed then the ground current from the data sheet is 2.8 μA. For an NCP552 (3.0 V), the maximum input voltage will then be 6.12 V.

INFORMATION FOR USING THE SC–82AB SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SC–82AB (SC70–4)

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping
NCP552SQ15T1	1.5	LAW	SC82–AB (SC70–4)	3000 Units/ 8″ Tape & Reel
NCP552SQ18T1	1.8	LAX		
NCP552SQ25T1	2.5	LAY		
NCP552SQ27T1	2.7	LAZ		
NCP552SQ28T1	2.8	LBA		
NCP552SQ30T1	3.0	LBB		
NCP552SQ33T1	3.3	LBC		
NCP552SQ50T1	5.0	LBD		

Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.