6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

DESCRIPTION

The NE5036 is an easy to use, low cost, successive approximation Analog to Digital converter, fabricated in Bipolar/I^2L technology, and packaged in a convenient 8-pin mini dip package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{START}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

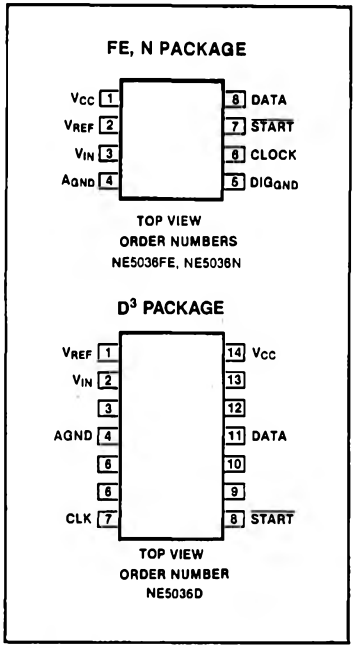
FEATURES

- Three-state output buffer for easy μProcessor interfacing
- Fast successive approximation converter, 23μsec
- T^2L compatible inputs and outputs
- Easy interface to CMOS μProcessors
- Guaranteed no missing codes over full operating range
- Single supply operation, + 5V
- High impedance analog inputs
- Positive true binary serial output

APPLICATIONS

- Temperature control
- μP-based appliances
- Light level monitor
- Electronic toys
- Joystick interface
- μP/Transducer interface

PIN CONFIGURATION

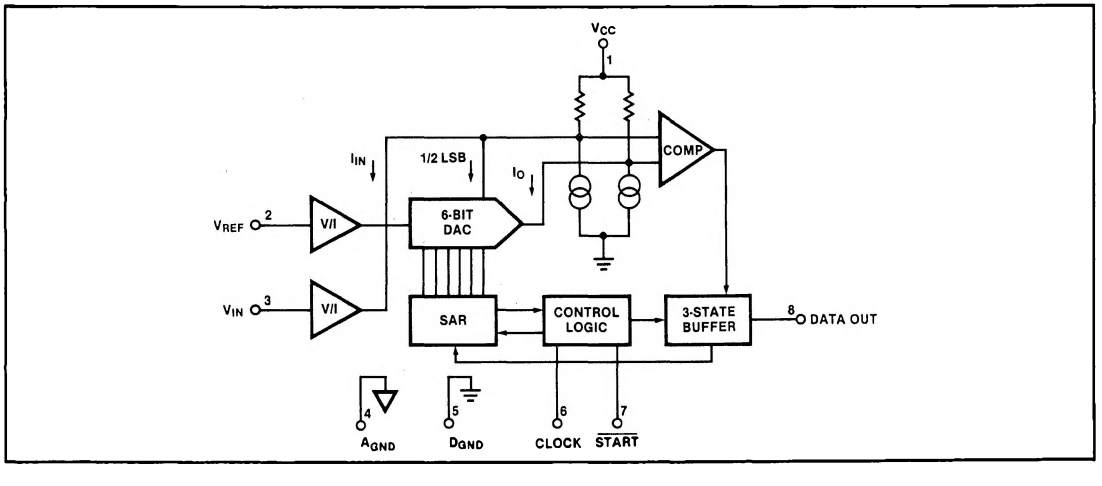


NOTES:
1. SOL-Released in large SO package only
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{START}$ & CLOCK)	7	V
D_{OUT}	Data output pin		
	Three-state mode	7	V
	Enabled mode	20	mA
Δ_{GND}	Analog GND to digital GND	± 1	V
T_A	Operating temperature range	0 to 70	°C
T_{Stg}	Storage temperature range	– 65 to 150	°C
t_{Sold}	Lead soldering temperature	300	°C
P_D	Power dissipation		
	FE package	220	mW
	N package	220	mW

BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full scale gain error[2,3,4]	V_{REF} = 2.0V, T_A = 25°C		±1	±2	LSB
ϵ_{ZS}	Zero scale offset error[2]	V_{REF} = 2.0V, T_A = 25°C		±1/2	−1/2, +2	LSB
P_{SR}	Power supply rejection Max change in full scale[2]	V_{REF} = 2.0V 4.75V ≤ V_{CC} ≤ 5.5V		±1/2	±1	LSB
I_{IN}	Analog input bias current	0 ≤ V_{IN} ≤ 2.5V		1	10	μA
I_{REF}	Reference bias current	0 ≤ V_{REF} ≤ 2.5V		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current	2.4V ≤ V_{OH}	300			μA
I_{OL}	Logic '0' output current	V_{OL} ≤ 0.4V	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	μA
I_{CC}	Positive supply current			14	24	mA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V; V_{REF} = 2.0V; Clock = 350kHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Max clock frequency				350			kHz
T_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width				1.3			μs
t_S	Setup time, $\overline{START}$ to clock[6]	Clock	$\overline{START}$		500			ns
$t_{P(OUT)}$	Propagation delay[5]	Data out	Clock	T_A = 25°C, t_r = t_f < 20ns			600	ns
$t_{P(3\text{-STATE})}$	Propagation delay[5]	Data (3-State)	$\overline{START}$	T_A = 25°C, t_r = t_f < 20ns			600	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)
5. The time between the specified reference points on the clock and the output waveforms with the output changing (low to high or high to low).
6. The high to low transition of the $\overline{START}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{START}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.

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CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally generated clock source (max freq = 350 kHz) must be provided to pin 6. An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{\text{START}}$ pin going low, successive approximation conversion commences after the first low going edge of the clock pulse. Successive bits, beginning with the MSB (D5) are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less, that bit stays at 1 and the output buffer goes to 1. After the second high to low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{\text{START}}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{\text{START}}$ pulse.

When $\overline{\text{START}}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal 1/2 LSB offset, so that the code transition points are located 1/2 LSB on either side of the exact analog input for a given code. Thus the first transition (000000 to 000001) will occur at an input of 1/2 LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The Ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF and should be located close to the device to minimize the effects of noise spikes on V_{CC}.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance at these inputs at or below 2K-ohms.

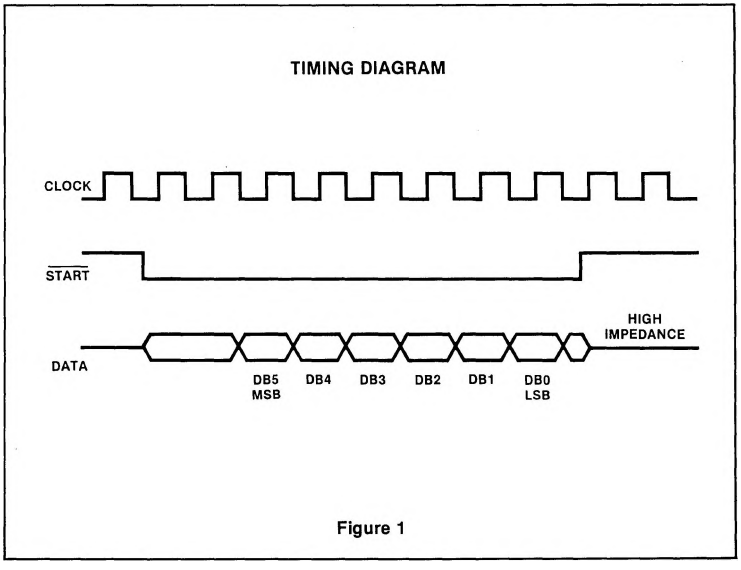


Figure 1

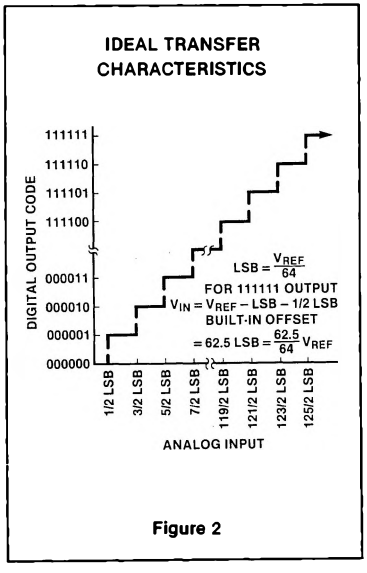
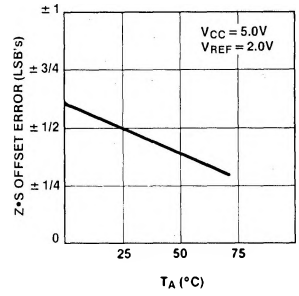


Figure 2

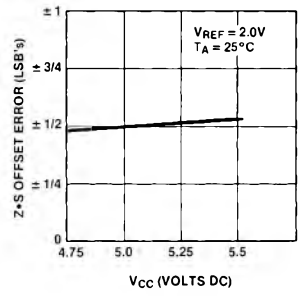
6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

TYPICAL PERFORMANCE CHARACTERISTICS

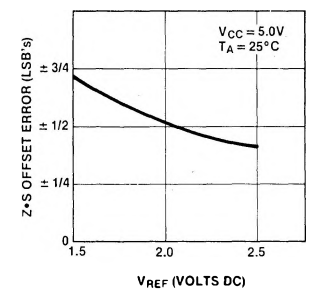
ZERO SCALE OFFSET ERROR vs TEMPERATURE



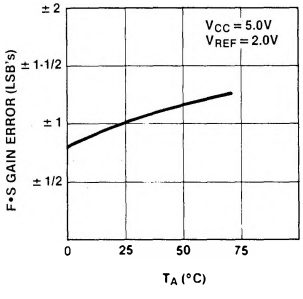
ZERO SCALE OFFSET ERROR vs V_{CC}



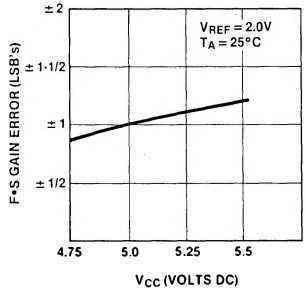
ZERO SCALE OFFSET ERROR vs V_{REF}



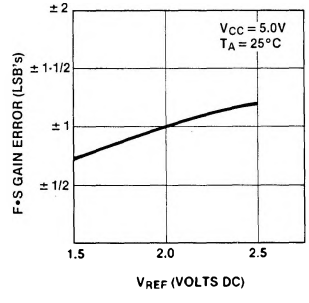
FULL SCALE GAIN ERROR vs TEMPERATURE



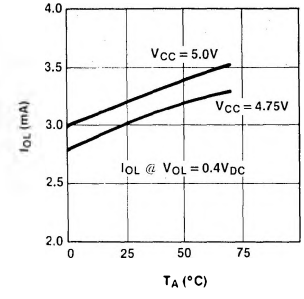
FULL SCALE GAIN ERROR vs V_{CC}



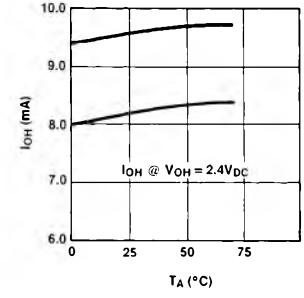
FULL SCALE GAIN ERROR vs R_{REF}



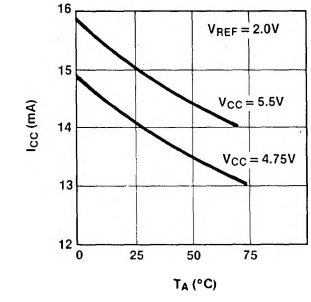
I_{OL} vs TEMPERATURE (DATA OUTPUT)



I_{OH} vs TEMPERATURE (DATA OUTPUT)



I_{CC} vs TEMPERATURE



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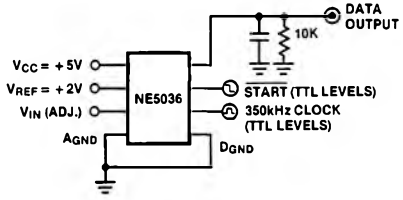
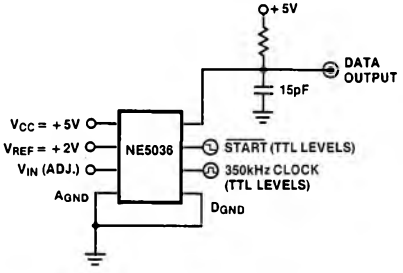
AC TEST CIRCUITS AND WAVEFORMS

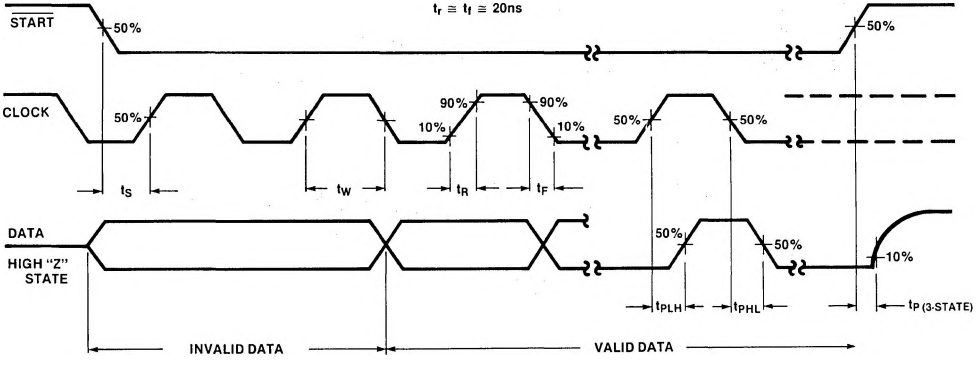
PROPAGATION DELAY TIME $t_{p\ (DATA)}$

DATA OUTPUT (LOW TO HIGH)



DATA OUTPUT (HIGH TO LOW)





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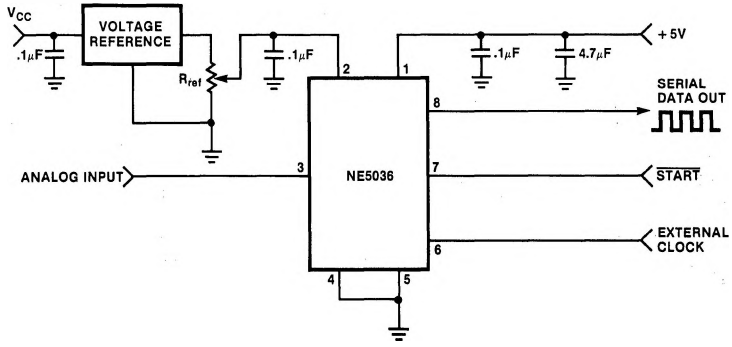
TYPICAL APPLICATION

1. BASIC NE5036 CONFIGURATION



2. DIGITAL COMMUNICATIONS USING NE5036