HIGH SPEED FSK MODEM RECEIVER — NE5081

DESCRIPTION

The NE5081 is the receiver chip of a two chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies in the 802 standard. However, the receiver will work at other frequencies.

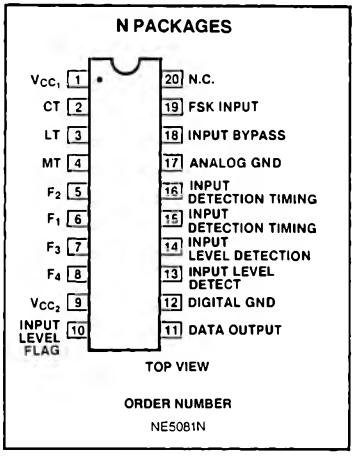
FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half or full duplex operation
- Low bit rate error (10^{-12} typical)

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

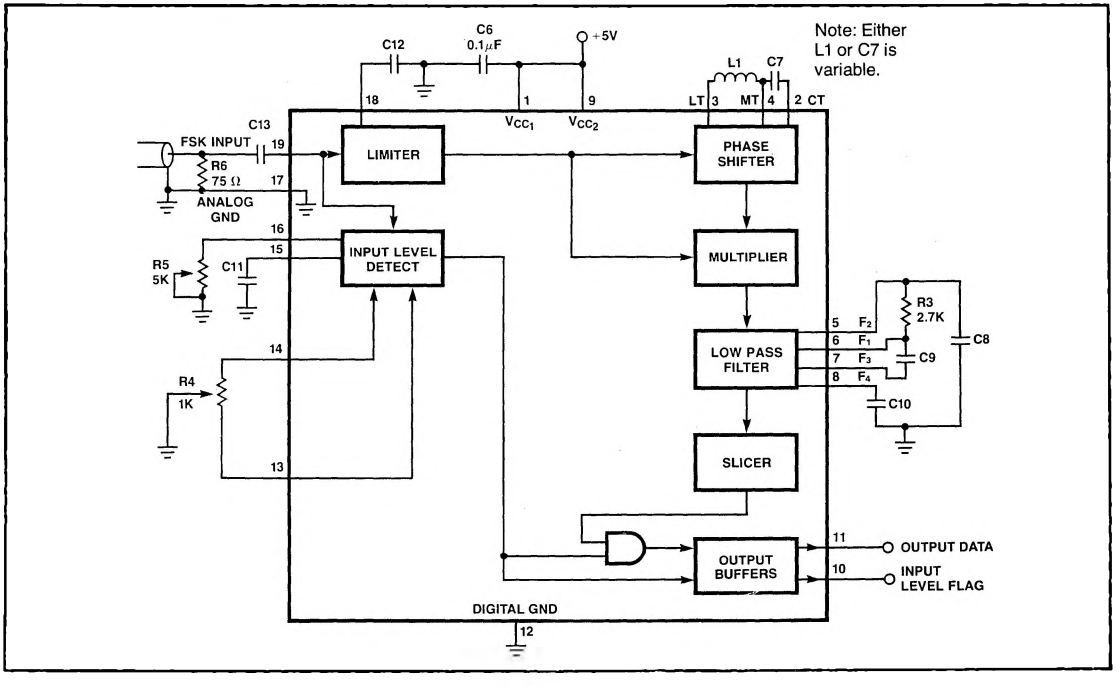
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

SYMBOL & PARAMETER	RATING	UNIT
Supply Voltage V_{CC_1} V_{CC_2}	+6	Volts
Input Voltage Range	-0.3 to $+V_{CC}$	Volts
Output (Data, Level Detect) Max Sink Current	20	mA
Power Dissipation	800	mW
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering, 10 sec)	300	°C
Max Differential Voltage between Analog and Digital Grounds	100	mV

BLOCK DIAGRAM



HIGH SPEED FSK MODEM RECEIVER — NE5081

GENERAL DESCRIPTION

The NE5081 will accept an FSK encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4 (Token-Passing Single Channel Phase-Continuous FSK Bus) i.e., 3.75MHz and 6.25MHz. However, it will work at other frequencies (see note 1).

Its normal acceptable input signal level range is from 16mV RMS to 1V RMS. (This can be adjusted, see note 2 below.)

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ±40nSec (see definition of "Jitter" note 3).

Notes:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Fig. 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV RMS.
3. Jitter Definition
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	V_{CC_1}—should be connected to the 5 volt supply and pin 9
2	**CT**—one end of an external capacitor that is used to tune the receiver
3	**LT**—one end of an inductor that is used to tune the receiver
4	**MT**—the junction of the capacitor and inductor used for tuning the receiver
5	**F2**
6	**F1** Pins 5, 6, 7, 8 are used for a low pass filter to remove carrier
7	**F3** harmonics from the data output
8	**F4**
9	V_{CC_2}—connect to Pin 1 (see Pin 1 function) close to the device
10	**INPUT LEVEL FLAG**—this pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level
11	**DATA OUTPUT**—supplies T^2L level data that corresponds to the FSK input received
12	**DIGITAL GROUND**—should be connected to digital ground
13 and 14	**INPUT LEVEL DETECT**—These pins are used to set the level of input signal that the device will accept as valid
15	**INPUT DETECTION TIMING**—an external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable
16	**INPUT DETECTION TIMING**—same as pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency
17	**ANALOG GROUND**—connect to analog ground close to the device
18	**INPUT BYPASS**—A capacitor between this pin and ground is used to bypass the input bias circuitry
19	**INPUT**—the FSK signal from the cable goes to this pin
20	**NO CONNECTION**

HIGH SPEED FSK MODEM RECEIVER — NE5081

ELECTRICAL CHARACTERISTICS

$V_{CC_{1,2}}$ = 4.75-5.25V. External LC circuit tuned to 5MHz. Input level detect set at 16mV Rms, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	TEST CONDITIONS	NE5081			UNIT
			Min.	Typ.	Max.	
Logic Low Frequency	F_0	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
Logic High Frequency	F_1	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
Minimum Input Detect Level	IN_{DL}	Minimum input level that is detected as carrier. See Note 2 in General Description	5		50	mV RMS
LOGIC LEVELS:						
Data Output	V_{OL}	I_{OL} = 4.0mA V_{IN} > 16mV RMS Freq = F_0			0.4	Volts
Data Output	V_{OH}	I_{OH} = −400μA V_{IN} > 16mV RMS Freq = F_1	2.4			Volts
Data Output	V_{OH}	I_{OH} = −400μA V_{IN} < 5mV RMS Freq = F_0	2.4			Volts
Input Detect Flag	V_{OL}	I_{OL} = 4.0mA V_{IN} = 0V RMS			0.4	Volts
	V_{OH}	I_{OH} = −400μA V_{IN} > 16mV	2.4			Volts
Supply Current	I_{CC}	V_{CC} = 5.25V (V_{CC_1} connected to V_{CC_2}) V_{IN} = 1.0V RMS Freq = F_1 or F_0			50	mA
Bit Error Rate	B.E.R	Input Signal > 16mV RMS. maximum in-band noise = 1.6mV RMS		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	NE5081			UNIT
				Min.	Typ.	Max.	
Delay Time T_B	Input Level Detect Flag	Input On	Figure 1		0.05	1	μS
Delay Time T_C	Input Level Detect Flag	Input Off	Figure 1	.5	1.5	2.5	μS
Delay Time T_D	Output Enabled	Input On	Figure 2			2	μS
Delay Time T_E	Output Disabled	Input Off	Figure 2	.5	1.5	2.5	μS
Required Delay	Carrier Turn Off	Valid Data End		2			μS

TIMING DIAGRAMS

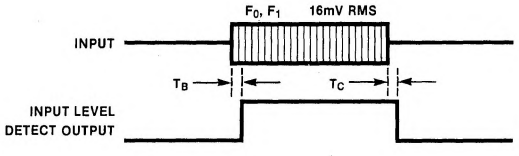


Figure 1. Delay Time, T_B, T_C

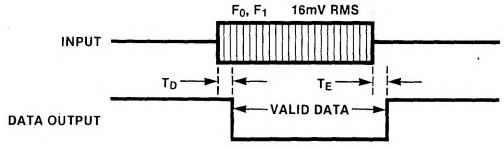


Figure 2. Delay Time, T_D, T_E