Signetics

NE/SA5217

Fiber Optic Postamplifier with Link Status Indicator

Objective Specification

Linear Products

DESCRIPTION

THE NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible, instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmidt trigger function by connecting two external capacitors. The result is that a much longer string of 1's and 0's, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the post-amplifier inputs. The NE/SA5212/5217 or NE/SA5211/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

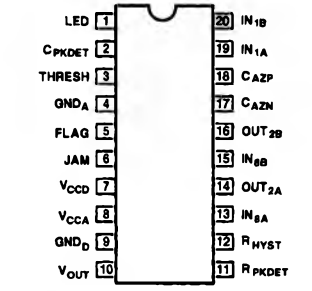
- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**
- **Good for 2^{23}-1 pseudo random number sequence**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5217D
20-Pin Plastic SOL	−40°C to +85°C	SA5217D

PIN CONFIGURATION

D[1] Package



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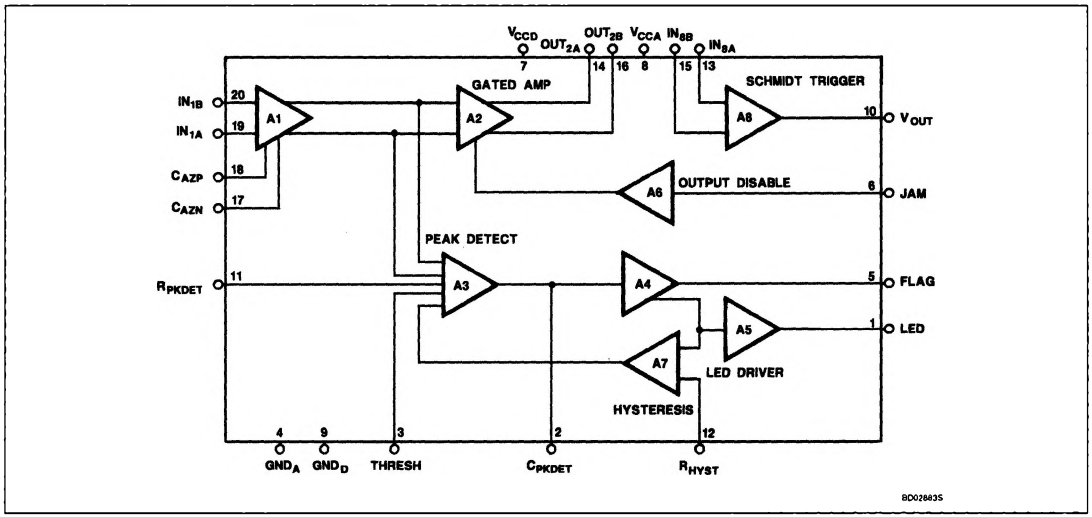
NOTE:
1. SOL — Released in large SO package only.

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, Low. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/− inputs)	3.16	3.4	3.63	3.13	3.4	3.65	V	
V_{O1}	A1 output bias voltage (+/− outputs)	3.17	3.8	4.45	3.10	3.8	4.50	V	
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (V_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to 5.25V		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I8}	A8 input bias voltage (+/− inputs)	3.59	3.7	3.85	3.7	3.86	V		
V_{OH}	High-level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		−40	−26		−40	−24.4	μA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		−95			−95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA

DC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	-450	-240		-485	-240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5214			SA5214			UNIT
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test Circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test Circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Maximum Functional A1 input signal (single ended)	Test Circuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage range	Test circuit, $T_A = 25°C$		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz R_{RHYST}=5k R_{THRESH} = 47k		12			12	mV_{P-P}	
t_{TLH}	TTL Output Rise Time 20% to 80%	Test circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$	2.5				2.5		%

NOTE:
1. The NE/SA5217 is capable of detecting a much lower input level. Operation under 12mV_{P-P} cannot be guaranteed by present day automatic testers.

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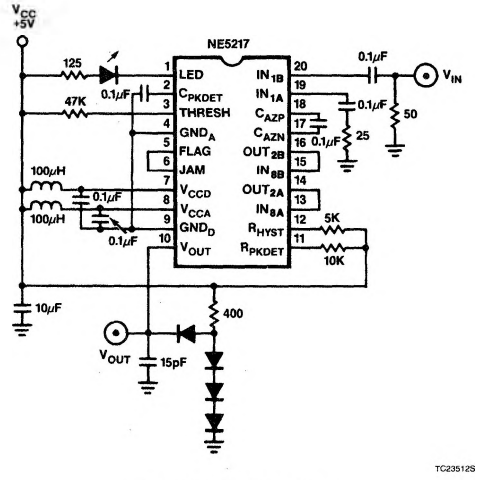
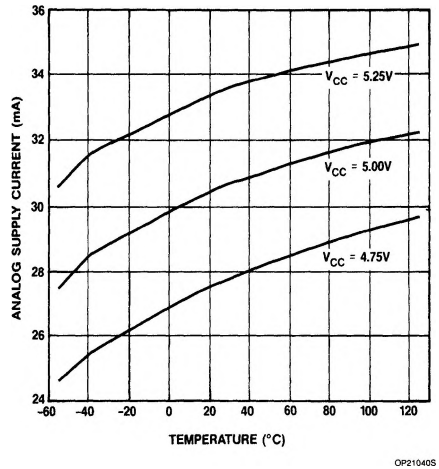


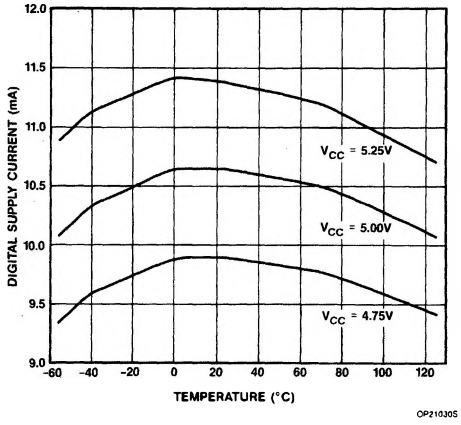
Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

Analog Supply Current vs Temperature



Digital Supply Current vs Temperature



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THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5217 post amplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

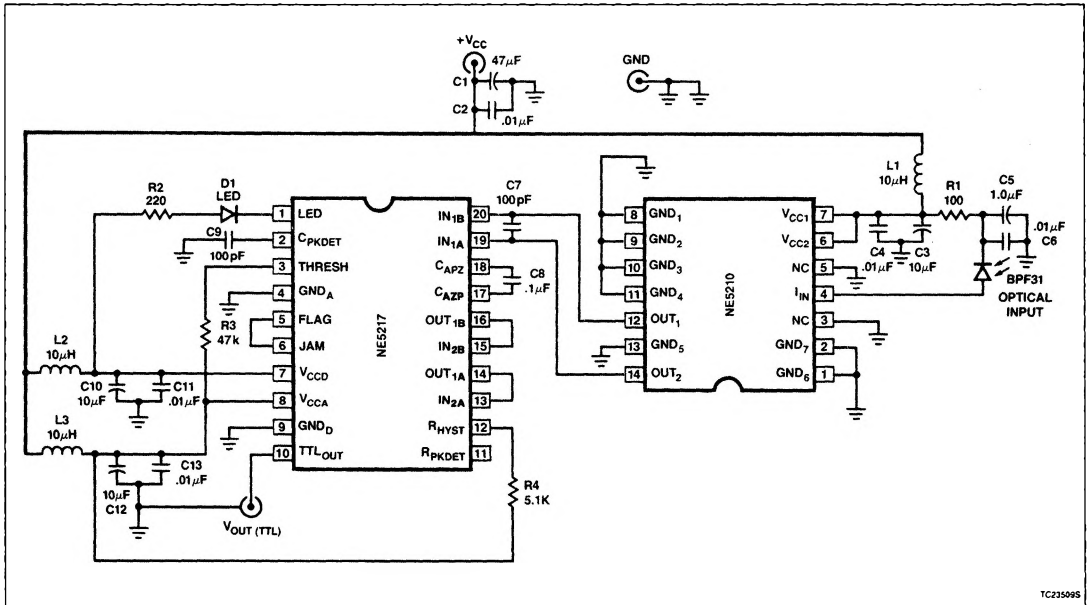
The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifiers's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5217 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et a1.

A typical application of the NE5217 post amplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to Application Brief AB 1432.



NOTE:
The NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver