Operational Amplifiers

NH0023/NH0023C sample and hold amplifier

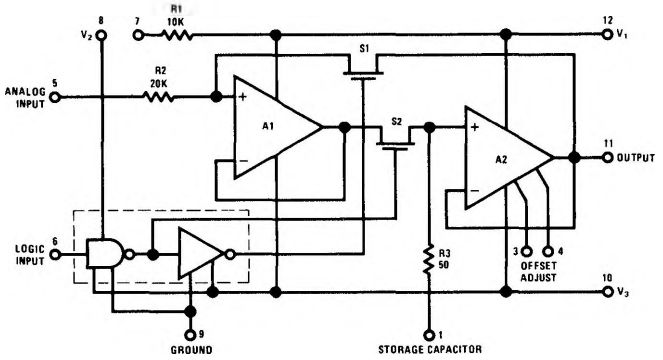
general description

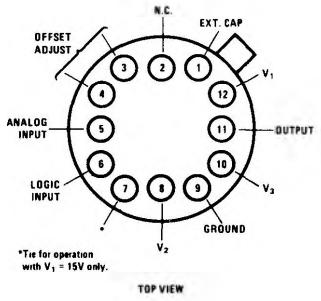
The NH0023/NH0023C is a complete sample and hold circuit including input buffer amplifier, output buffer amplifier, analog signal sampling gate, and logic circuitry. The device is designed to operate from ±15V dc supplies, but provision is made for connection of a separate 5V logic supply in minimum noise applications. Other important design features include:

- 0.5 mV/sec drift at 25°C, C_S = 0.01 μF and V_{OUT} = ±5V
- Sample acquisition time of 100 μs for a full 20V change
- ±10V input voltage range
- Logic inputs are TTL/DTL compatible
- Input offset is adjustable with a single 10k trimpot
- Output is short circuit proof

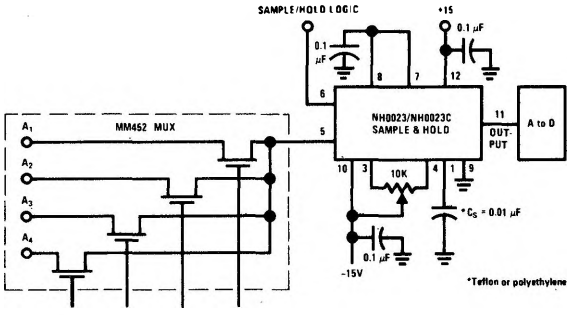
The NH0023/NH0023C is ideally suited for a wide variety of sample and hold applications including analog to digital conversion and synchronous demodulation. The NH0023 is specified over the temperature range of −55°C to +125°C; whereas the NH0023C is specified from 0°C to 85°C.

schematic and connection diagrams





typical application



absolute maximum ratings

$V_1 - V_3$ (Differential Voltage)	40V
V_2 Maximum	7V
Logic Input Voltage Maximum	5.5V
Analog Input Voltage	±15V
Power Dissipation	1.5W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range NH0023	−55°C to +125°C
NH0023C	0°C to +85°C

electrical characteristics (Notes 1 & 2)

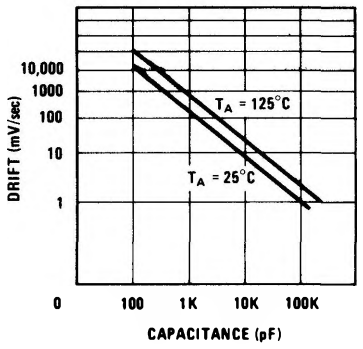
PARAMETER	CONDITIONS	NH0023			NH0023C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Sample (Logic "1") Input Voltage	V_2 = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V_2 = 5.5V, V_{IN} = 2.4V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V_2 = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V_2 = 5.5V, V_{IN} = 0.4V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current V_1 & V_3	V_1 = +15V, V_3 = −15V V_{IN} = 0V, V_{OUT} = 0V		4.5	6.0		4.5	6.0	mA
Supply Current V_2	V_2 = 5.0V, V_{IN} = 0V		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V_{OUT} = ±10V (Full Scale)			0.01			0.01	%
Input Impedance Sample	$V_{IN} \geq 2.0$	500			300			kΩ
Input Impedance Hold	$V_{IN} \leq 0.8V$	20			20			kΩ
Drift Rate	$V_{OUT} \leq \pm 5V$, C_S = 0.01 μF T_A = 25°C			0.5		0.5		mV/sec
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF T_A = 25°C		10	20		20	50	mV/sec
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF −55°C ≤ T_A ≤ +125°C			100				mV/sec
Drift Rate	V_{OUT} = ±10V, C_S = 0.01 μF 0°C ≤ T_A ≤ 85°C						200	mV/sec
Sample Acquisition Time	ΔV_{OUT} = 20V		50	100		50	100	μs
Output Offset Voltage	$R_S \leq 10k$			±20			±20	mV
Analog Voltage Output Range	$R_L \geq 2k$	±10	±11		±10	±11		V

Note 1: Unless otherwise noted, these specifications apply for V_1 = +15V, V_2 = 5.0V, V_3 = −15V, pin 9 grounded, a 0.01 μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the NH0023, and 0°C to 85°C for the NH0023C.

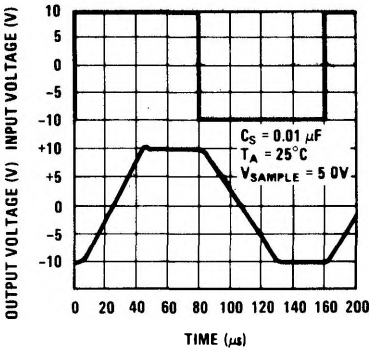
Note 2: All typical values are for T_A = 25°C.

typical performance

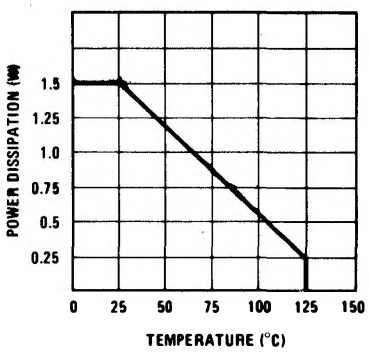
Drift vs Capacitance



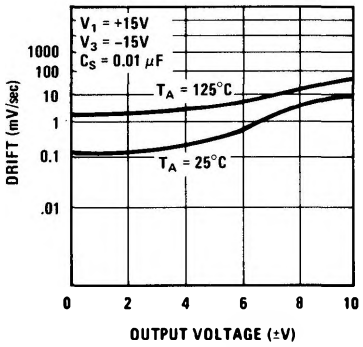
Acquisition Time



Power Dissipation



Drift vs. Output Voltage



applications information

1. *Drift Error Minimization*

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality teflon, polycarbonate, or polyethylene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-29 for detailed recommendations.

2. *Capacitor Selection*

The size of the capacitor is dictated by the desired drift rate and acquisition time. The drift is determined by $\frac{dv}{dt} = \frac{I}{C_S}$, where I is the sum of the leakage currents. At room temperature leakage current for the NH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_o RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_o RC_S}$$

where: R = the internal resistance in series with C_S
Δe_o = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_o C_S}}{20}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

3. *Offset Null*

Provision is made to null the NH0023/NH0023C by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4. *Elimination of the 5V Logic Supply*

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_2. Decoupling pin 8 to ground through 0.1 μF disc capacitor is recommended in order to minimize transients in the output.