

NM24C02L/C04L

2K-/4K-Bit Serial EEPROM with Extended Voltage (I²C Synchronous 2-Wire Bus)

General Description

The NM24C02L/04L devices are 2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements. National EEPROMs are designed and tested for applications requiring high reliability, high endurance and low power consumption.

These devices have an operating voltage range of 2.5V to 5.5V and are offered in an 8-pin small outline (SO) package, making these devices perfectly suited for low power applications that require minimal board space usage.

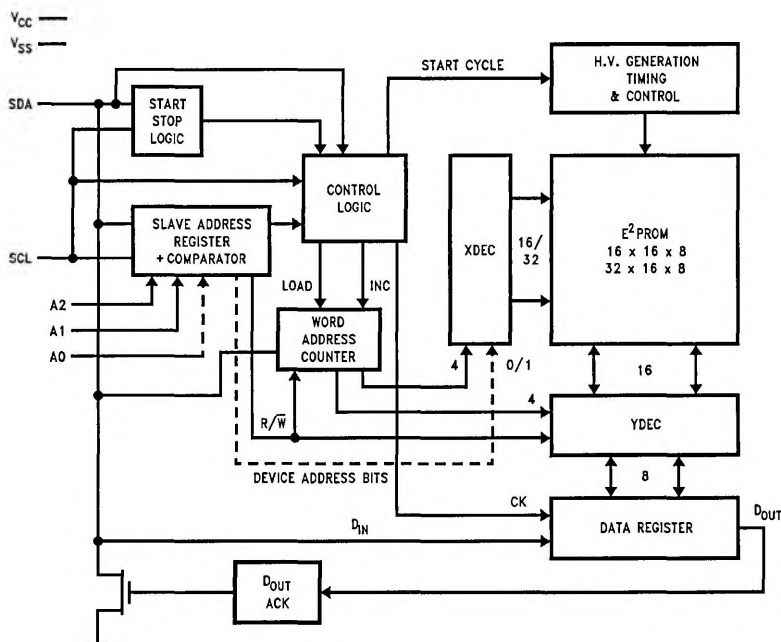
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the

user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

Features

- Extended operating voltage, 2.5V–5.5V
- Low Power CMOS
 - 2 mA active current typical
 - 60 μ A standby current typical
- 2-wire I²C serial interface
 - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
 - Minimizes total write time per byte
- Self timed write cycle
 - Typical write cycle time of 5 ms
- Endurance: 10⁶ data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 8 pin SO package

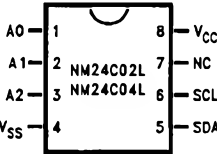
Functional Diagram



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Connection Diagrams

Dual-In-Line Package (N)
and SO Package (M8)



See NS Package Number
M08A (M8) and N08E (N)

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Pin Names

A0, A1, A2	Device Address Inputs
VSS	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
VCC	+ 5V

Ordering Information

Commercial Temperature Range (0°C to + 70°C)

Order Number
NM24C02LN/NM24C04LN NM24C02LM/NM24C04LM

Extended Temperature Range (– 40°C to + 85°C)

Order Number
NM24C02LEN/NM24C04LEN NM24C02LEM/NM24C04LEM

LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	0°C to +70°C
NM2402L/C04L	-40°C to +85°C
NM24C02EL/04EL	2.5V to 5.5V
Positive Power Supply (V_{CC})	

DC and AC Electrical Characteristics $V_{CC} = 2.5V$ to $4.5V$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	$f_{SCL} = 100\text{ kHz}$		2.0	3.0	mA
I_{SB}	Standby Current	$V_{IN} = GND$ or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	$V_{IN} = GND$ to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = GND$ to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 200\text{ }\mu A$			0.4	V

Capacitance $T_A = 25^\circ C$, $f = 1.0\text{ MHz}$, $V_{CC} = 5V$

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O} = 0V$	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	$V_{IN} = 0V$	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and $C_L = 100\text{ pF}$

Note 1: Typical values are for $T_A = 25^\circ C$ and nominal supply voltage (5V).
Note 2: This parameter is periodically sampled and not 100% tested.

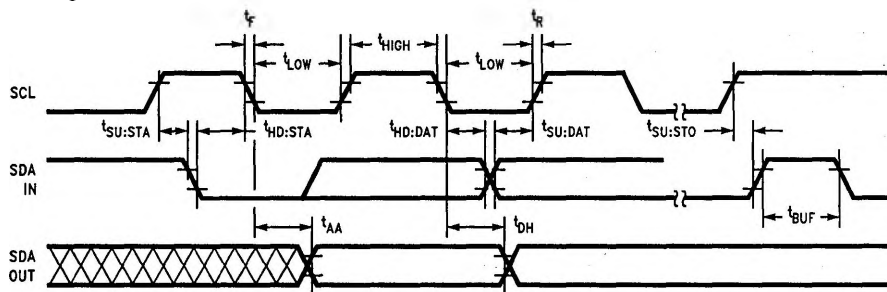
LOW VOLTAGE ($2.5V \leq V_{CC} < 4.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature -65°C to $+150^{\circ}\text{C}$

All Input or Output Voltages
with Respect to Ground $+6.5V$ to $-0.3V$

Lead Temperature
(Soldering, 10 seconds) $+300^{\circ}\text{C}$

ESD Rating 2000V min

Operating Conditions

Ambient Operating Temperature

NM24C02L/C04L

NM24C02EL/C04EL

Positive Power Supply (V_{CC})

0°C to $+70^{\circ}\text{C}$

-40°C to $+85^{\circ}\text{C}$

$2.5V$ to $5.5V$

DC and AC Electrical Characteristics $V_{CC} = 4.5V$ to $5.5V$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	$f_{SCL} = 100\text{ kHz}$		2.0	3.0	mA
I_{SB}	Standby Current	$V_{IN} = \text{GND or } V_{CC}$		60	100	μA
I_{LI}	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}$		0.1	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}$		0.1	10	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3\text{ mA}$			0.4	V

Capacitance $T_A = 25^{\circ}\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = 5V$

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O} = 0V$	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	$V_{IN} = 0V$	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and $C_L = 100\text{ pF}$

Note 1: Typical values are for $T_A = 25^{\circ}\text{C}$ and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

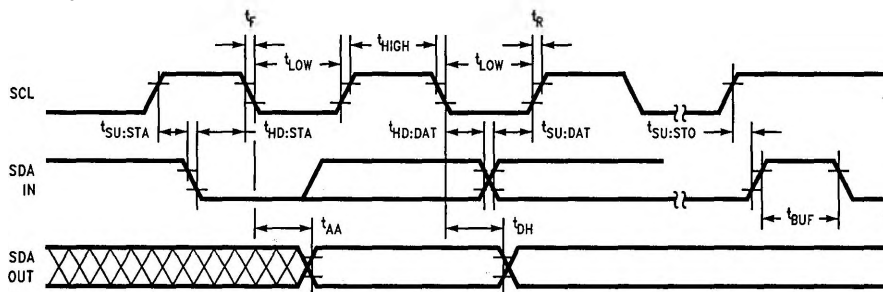
STANDARD VOLTAGE ($4.5V \leq V_{CC} \leq 5.5V$) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

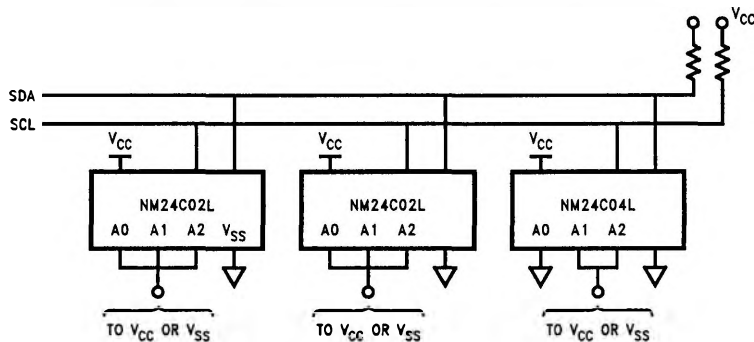
As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

Example of 8K (1/2 of Maximum Size) of Memory on 2-Wire Bus



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Note 1: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note 2: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note 3: It is recommended that the total line capacitance be less than 400 pF.

Note 4: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02L	DA	DA	DA	2048 Bits	1
NM24C04L	V _{SS}	DA	DA	4096 Bits	2

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS

INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) \times (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) \times (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) \times (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) \times (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/ V_{SS})

Device Operation

The NM24C02L/C04L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the NM24C02L/C04L will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing

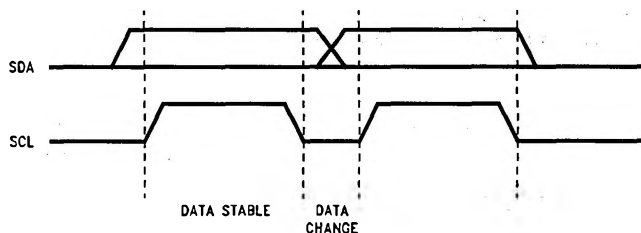
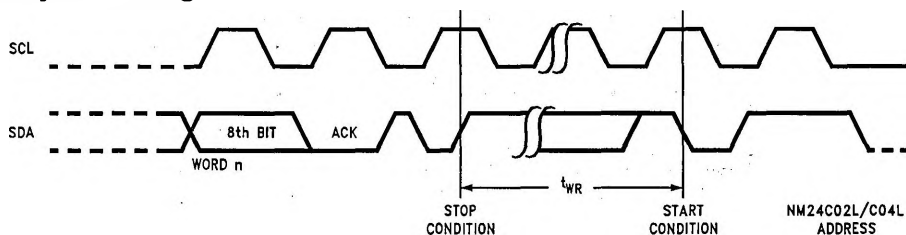


FIGURE 1. Data Validity

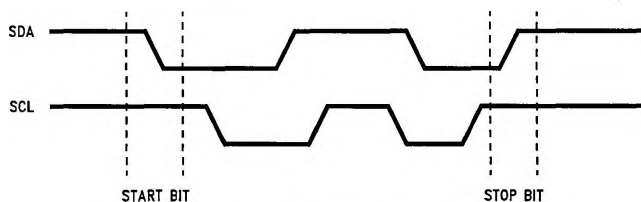


FIGURE 2. Definition of Start and Stop

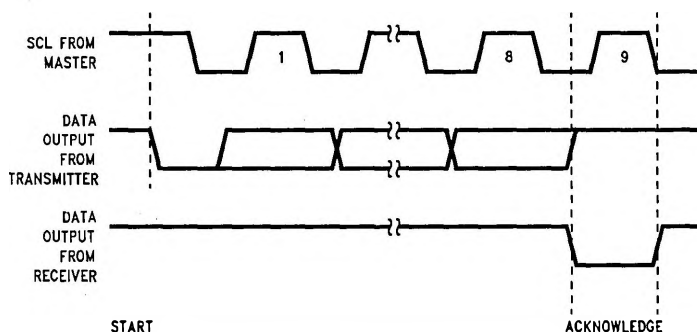


FIGURE 3. Acknowledge Response from Receiver

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ACKNOWLEDGE

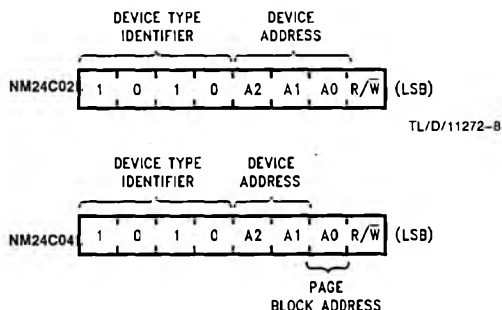
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for both devices: NM24C02L and NM24C04L.



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FIGURE 4. Slave Addresses

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(NONE)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C02	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

Device Addressing (Continued)

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C02L/C04L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24C02L/C04L responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL

begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

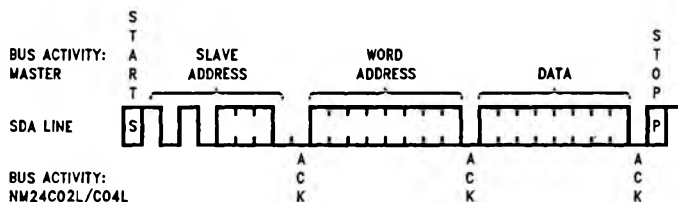


FIGURE 5. Byte Write

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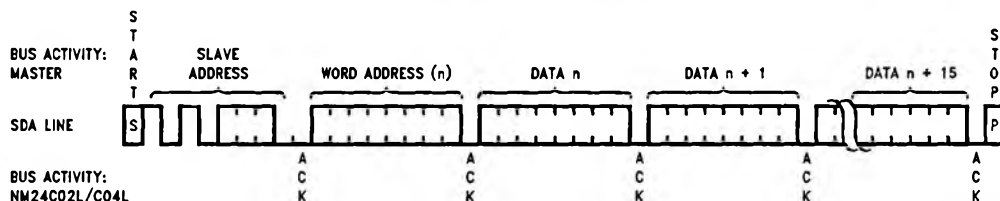
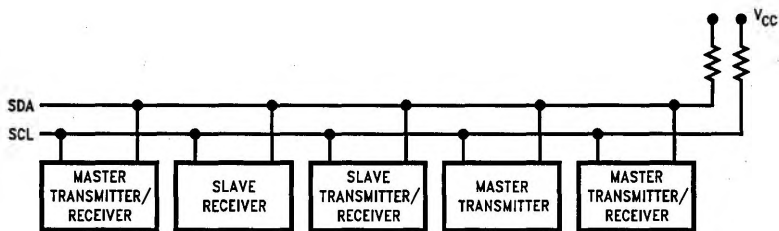


FIGURE 6. Page Write

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Write Operations (Continued)**FIGURE 10. Typical System Configuration**

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