National Semiconductor

NM93C06L/C46L/C56L/C66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V t0 5.5V)

General Description

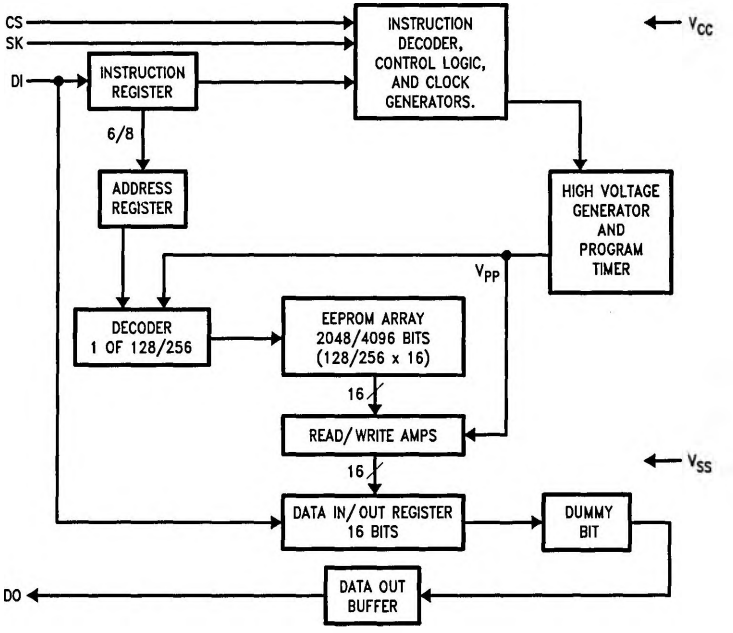
The NM93C06L/C46L/C56L/C66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CxxL Family functions in an extended voltage operating range, requires only a single power supply and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. These devices are available in an SO package for small space considerations.

The NM93CxxL Family interfaces to microprocessors and microcontrollers via a single 4-wire MICROWIRE™ bus which possesses the following parameters: SK (Serial Clock), CS (Chip Select), DI (Data Input) and DO (Data-Output). DI includes: instruction, address and data to be written. DO offers data read and programming status information. Serial interfacing allows 8-pin DIP or 8-pin SO packaging to minimize board space. The following seven instructions (op codes) control device operation: EWEN (Erase/Write Enable), EWDS (Erase/Write Disable), READ (Read), ERAL (Erase all registers), ERASE (Erase a register/address), WRAL (Write all registers with 16 bits of data) and WRITE (Write a register/address).

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; Typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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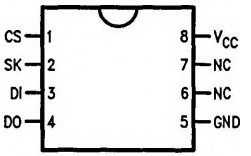
Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E or M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C06LN/NM93C46LN
NM93C56LN/NM93C66LN
NM93C06LM8/NM93C46LM8
NM93C56LM8/NM93C66LM8

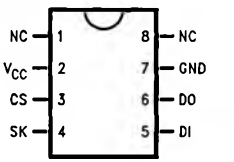
Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C06LEN/NM93C46LEN
NM93C56LEN/NM93C66LEN
NM93C06LEM8/NM93C46LEM8
NM93C56LEM8/NM93C66LEM8

Alternate (Turned) SO Pinout

Order Number
NM93C46TLM8/NM93C46TLEM8

Alternate SO Pinout (TM8)



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See NS Package Number M08A

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.2 0.2		μs
t_{DH}	DO Hold Time		Relative to SK	10		ns

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms

Capacitance (Note 4)

T_A = 25°C f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF		
V_{CC} Range	AC Test Conditions	
4.5V < V_{CC} < 5.5V	Input Pulse Levels	0.8V and 2.0V
	Timing Measurement Level (V_{IL}/V_{IH})	0.9V and 1.9V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 2.0V
	(TTL Load Conditions: I_{OL} = 2.1 mA, I_{OH} = −0.4 mA)	
2.0V < V_{CC} < 4.5V	Input Pulse Levels	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH})	0.4V and 1.6V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 1.6V
	(CMOS Load Conditions: I_{OL} = 10 μA, I_{OH} = −10 μA)	

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The above SK frequency specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	CS = 0V		50 50	μA
I_{IL}	Input Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	NM93C06LE-NM93C66LE	I_{OL} = 10 μA		0.2	V
f_{SK}	SK Clock Frequency	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		0 0	1 1	MHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 300		ns
t_{SKL}	SK Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 2) (Note 3)	250 250		ns
t_{CS}	Minimum CS Low Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	(Note 4) (Note 5)	250 250		ns
t_{CSS}	CS Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	50 50		ns
t_{DH}	DO Hold Time		Relative to SK	10		ns

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE	NM93C06L-NM93C66L NM93C06LE-NM93C66LE	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Note: Throughout this table "M" refers to temperature range (−55°C to +125°C), not package.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CxxL Family has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6 bits for the NM93C06 and NM93C46 and 8 bits for the NM93C56 and NM93C66 devices. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The READ instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to a 16-bit shift register output buffer. A dummy bit (logical 0) precedes all 16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state, (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 16 bits of data, programs all registers/addresses in the memory array with the specified data pattern, (Bulk write).

Instruction Set for the NM93C06L and NM93C46L

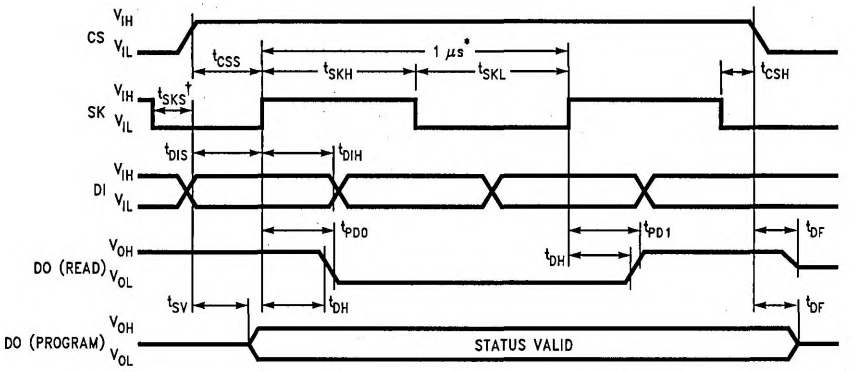
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NM93C56L and NM93C66L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
WRITE	1	01	A7–A0	D15–D0	Writes register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



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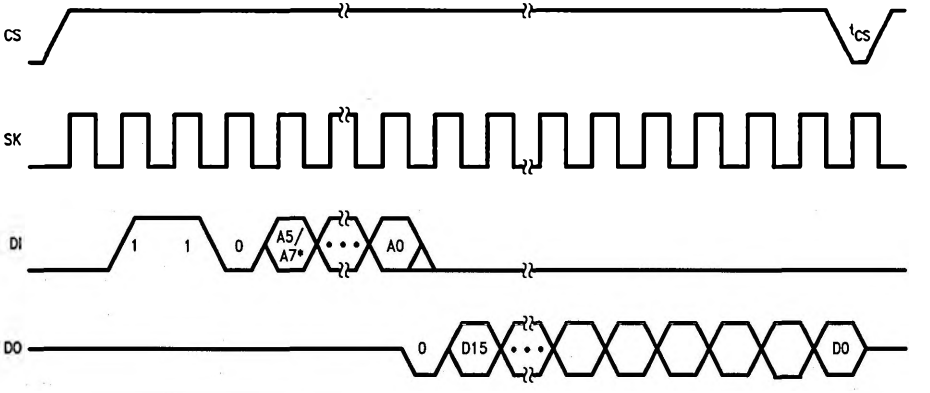
*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:



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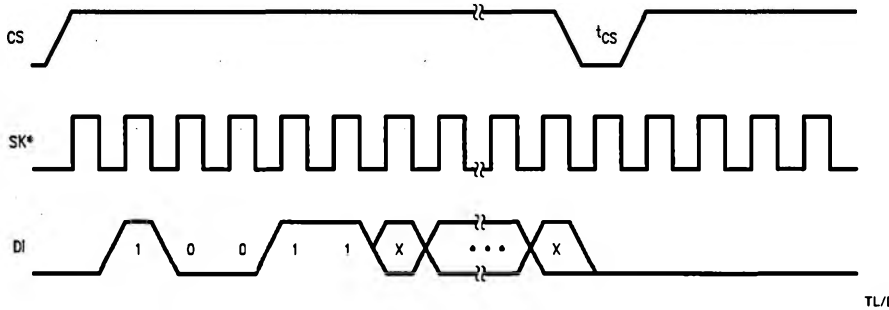
*Address bits A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

EWEN:



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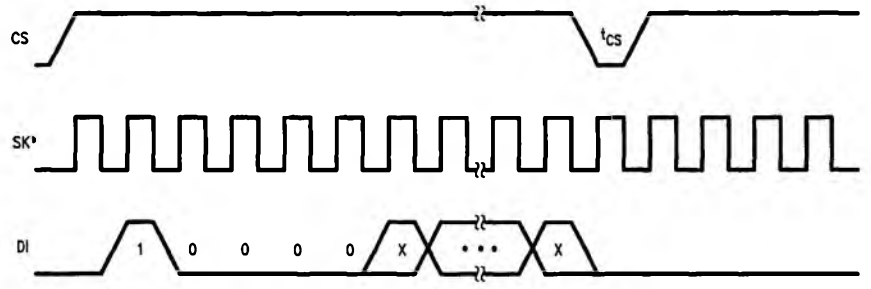
*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

EWDS:



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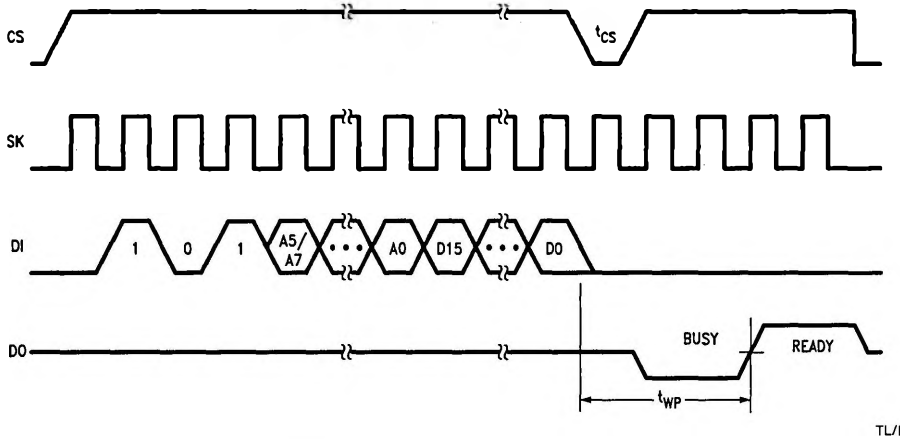
*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

WRITE:



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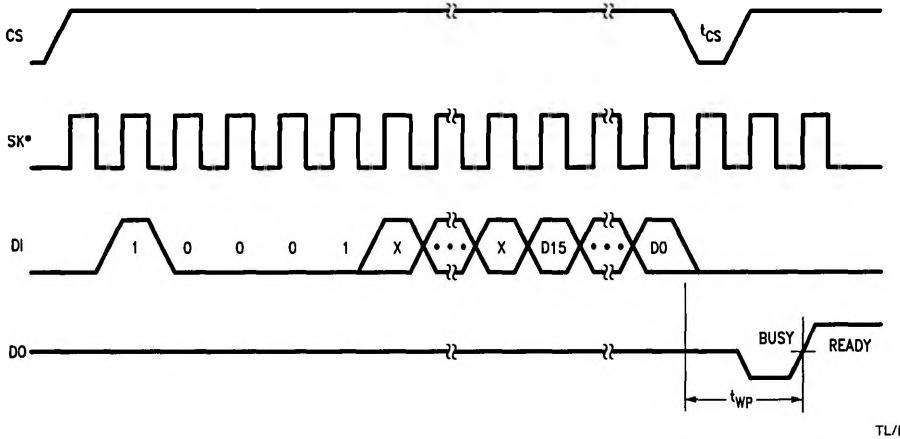
*Address bit A_5 and A_4 become "don't care" for NM93C06L.

*Address bit A_7 becomes a "don't care" for NM93C56L.

WRAL:

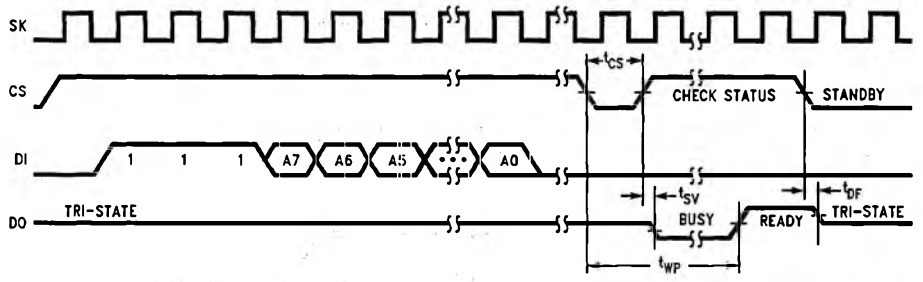


TL/D/10045–9

*The NM93C56L and NM93C66L require a minimum of 11 clock cycles. The NM93C06L and NM93C46L require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

ERASE:



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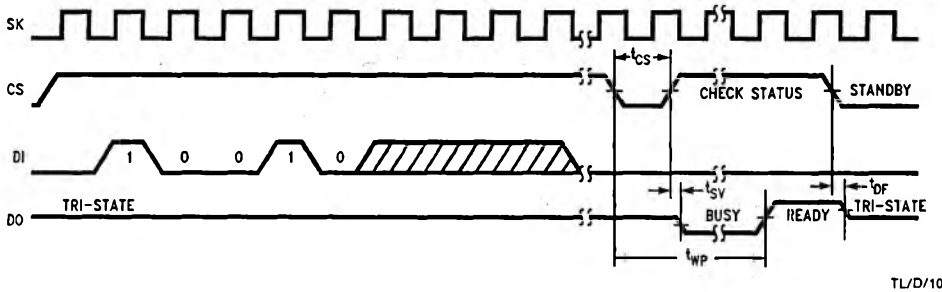
ERAL:



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