National Semiconductor

NM93C46AL
1024-Bit Serial EEPROM
64 x 16-Bit or 128 x 8-Bit Configurable

General Description

The NM93C46AL is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, low power consumption and a wide operating voltage range.

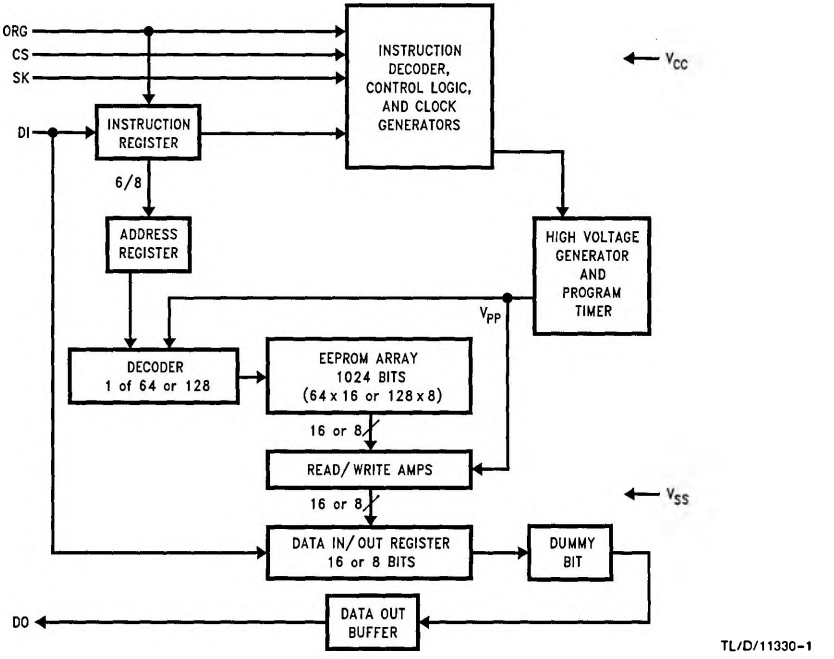
The interface is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46AL: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46AL is compatible with National Semiconductor's NM93C46L if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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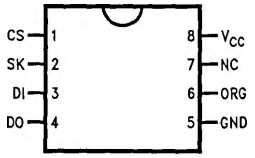
Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46ALN
NM93C46ALM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46ALEN
NM93C46ALEM8

LOW VOLTAGE (<4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Power Supply Range	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 250 kHz 4.5V ≤ V_{CC} ≤ 5.5V		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
	Pin 6			−10	10	
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1 0.8 V_{CC}	0.2 V_{CC} V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	NM93C46AL NM93C46ALE	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2}	Output Low Voltage		2V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA		0.1 V_{CC}	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	0.9 V_{CC}		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2)	1 1		μs
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 3)	1 1		μs

LOW VOLTAGE (<4.5V) SPECIFICATIONS

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.2 0.2		μs
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time				15	ms
t_{DH}	D0 Hold Time		Relative to SK	10		ns

Capacitance (Note 4)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 4 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. For example, if t_{SKL} = 1 μs, then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: For Commercial parts, CS must be brought low for a minimum of 1 μs between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHZ SK = 0.5 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHz SK = 0.5 MHz		3 3	mA
I_{CC3}	Standby Current	NM93C46AL NM93C46ALE	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NM93C46AL NM93C46ALE	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C46AL NM93C46ALE	I_{OL} = 2.1 mA I_{OL} = 2.1 mA		0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{SKL}	SK Low Time	NM93C46AL NM93C46ALE	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NM93C46AL NM93C46ALE	(Note 4) (Note 5)	250 500		ns

STANDARD VOLTAGE ($4.5 \leq V \leq 5.5$) (Continued)

DC and AC Electrical Characteristics (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46AL NM93C46ALE	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NM93C46AL NM93C46ALE	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NM93C46AL NM93C46ALE	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE	NM93C46AL NM93C46ALE	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = +25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

AC Test Conditions (>4.5V)

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46AL has seven instruction sets as described below. Note that each instruction set is broken down into the Start Bit (SB), Op code, Address (if applicable) and Data (if applicable). As shown in the timing diagrams and INSTRUCTION SET tables, address bits will have 6/7 bits and 8/16 bits for the data. All instruction bits are entered into the device on the SK low-to-high transitions.

Programming is enabled by bringing CS to a Logical 0 state for the required t_{CS} period. After this t_{CS} period the self-timed operation may be monitored by bringing CS to a logical 1 and observing the DO status: Logical 1 = READY (Ready for the next instruction) and Logical 0 = BUSY (Programming in progress).

Erase/Write Enable (EWEN):

When V_{CC} is applied to the device, it powers up in the programming Erase/Write disabled state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once this instruction is executed, programming remains enabled until the Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data disturbance, the Erase/Write Disable instruction disables all programming modes and should follow the end of all programming cycles.

Read (READ):

The Read instruction outputs the specified address data on the DO pin. After the READ instruction is received, the instruction and address are decoded and data is transferred from the address to an 8-/16-bit shift register output buffer. A dummy bit (logical 0) precedes all 8-/16-bit data out strings. The READ instruction may be executed from either the enabled or disabled state.

Erase (ERASE):

This instruction, when followed by an address location, programs all bits in the selected register/address to a 1 state (Register erase).

Erase All (ERAL):

This instruction programs all registers/addresses in the memory array to a 1 state (Bulk erase).

Write (WRITE):

This instruction, when followed by an address location and 8/16 bits of data, programs the selected register/address.

Write All (WRAL):

This instruction, when followed by 8/16 bits of data, programs all registers/addresses in the memory array with the specified data pattern (Bulk write).

Note: The NM93C46AL device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

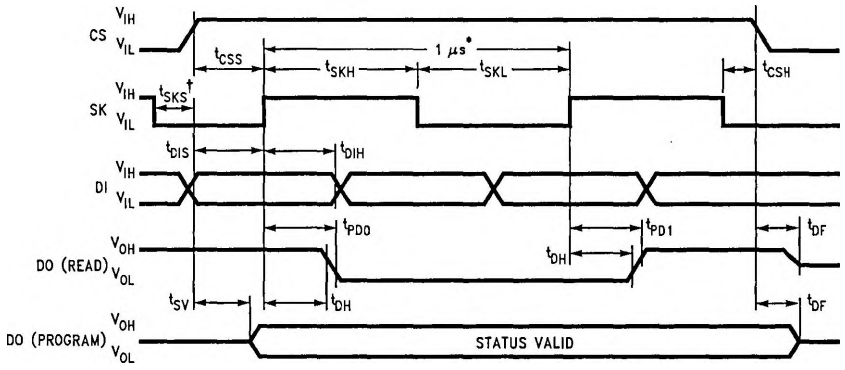
Instruction Set

Instruction	Start Bit	Opcode		Address*		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	1	1	A6–A0	A5–A0			Erase Address AN–A0
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	0	0	11XXXXX	11XXXX			Program Enable
EWDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

*It is necessary to clock in the "Don't Care" Address Bits.

Timing Diagrams

Synchronous Data Timing



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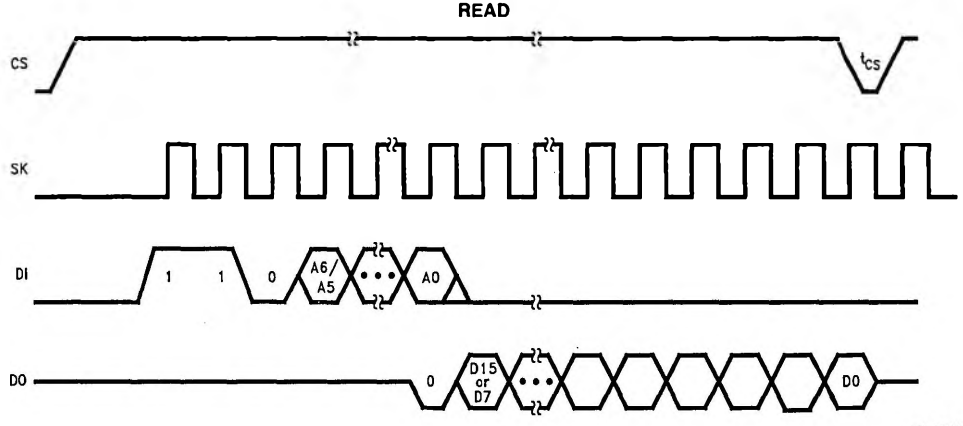
*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ



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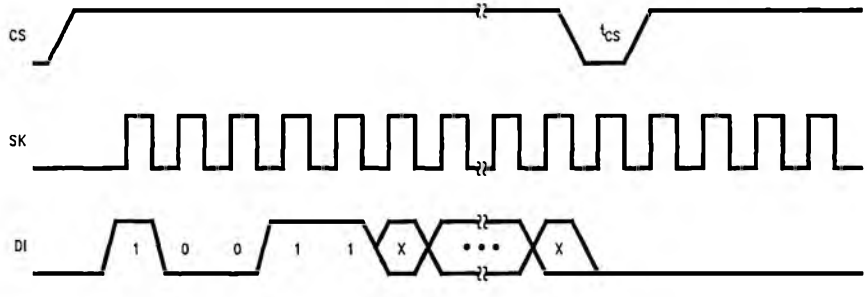
EWEN†

DO = TRI-STATE



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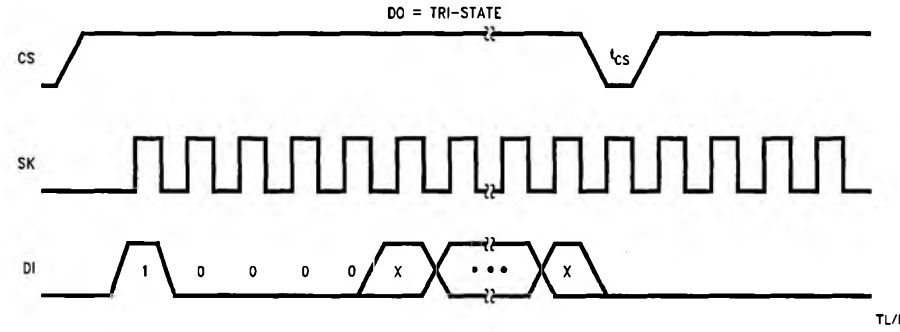
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

EWDS†



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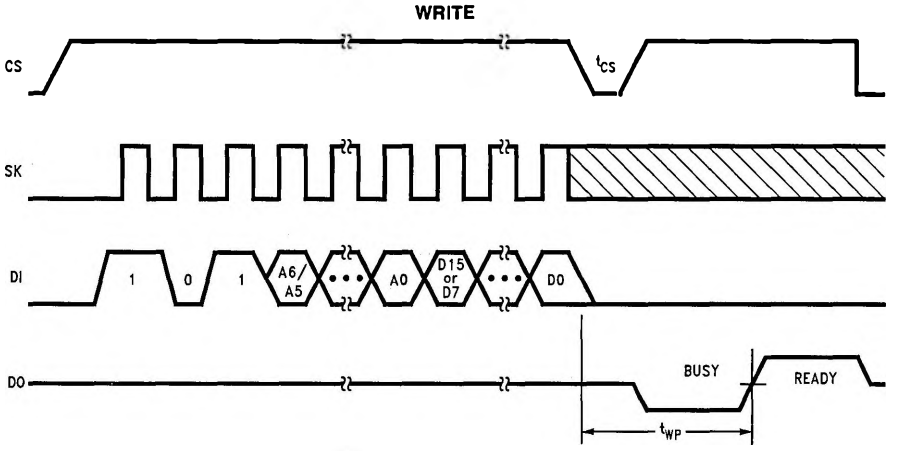
WRITE



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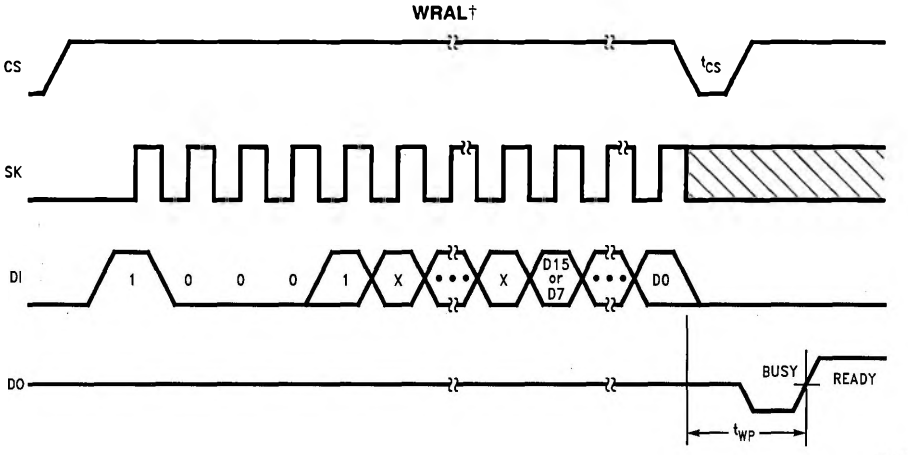
WRAL†



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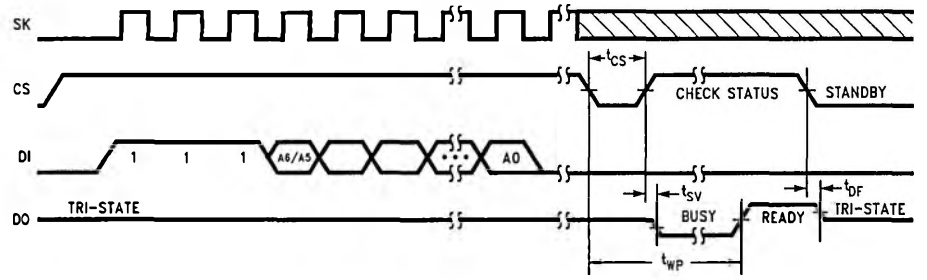
†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.

Timing Diagrams (Continued)

ERASE



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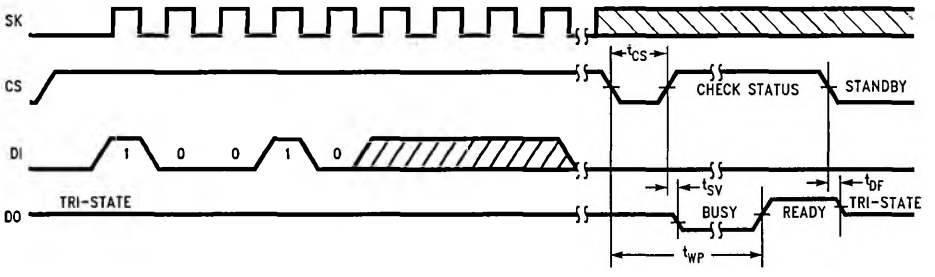
ERAL†



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†For the EWEN, EWDS, WRAL and ERAL it is necessary to provide a minimum number of clock cycles after the last bit of opcode is clocked in. In the 64x16 configuration a minimum of 4 additional clock cycles are required. In the 128 x 8 configuration a minimum of 5 additional clock cycles are required.