National Semiconductor

NM93C06/C46/C56/C66
256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™)

General Description

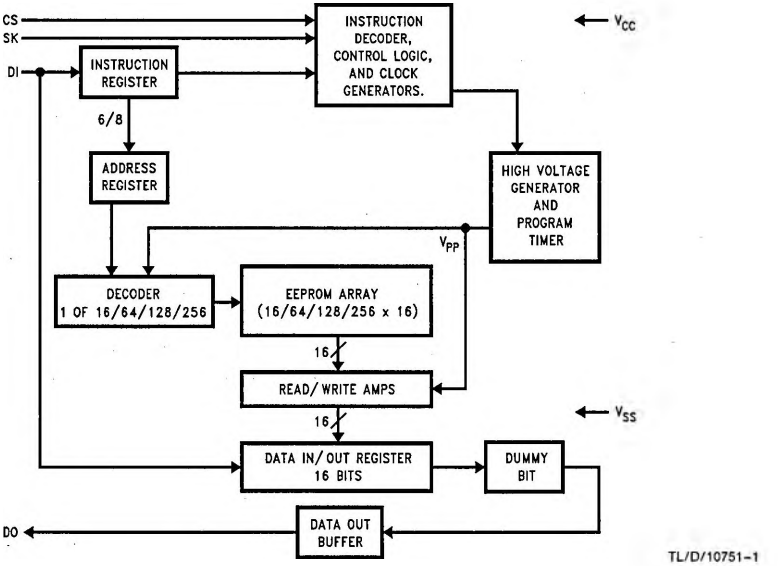
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

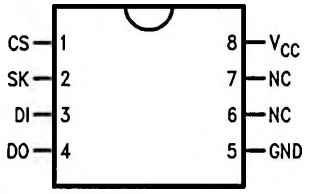
- Device status during programming mode
- Typical active current of 400 μA; Typical standby current of 25 μA
- Direct Write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93C06N/NM93C46N
NM93C56N/NM93C66N
NM93C06M8/NM93C46M8
NM93C56M8/NM93C66M8

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93C06MN/NM93C46MN
NM93C56MN/NM93C66MN
NM93C06MM8/NM93C46MM8
NM93C56MM8/NM93C66MM8

Extended Temp. Range (−40°C to +85°C)

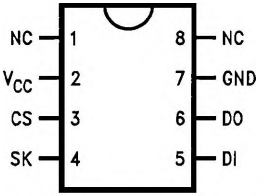
Order Number*
NM93C06EN/NM93C46EN
NM93C56EN/NM93C66EN
NM93C06EM8/NM93C46EM8
NM93C56EM8/NM93C66EM8

*For 14-Pin SO availability contact your local National Semiconductor Sales Office.

Alternate (Turned) SO Pinout

Order Number
NM93C46TM8 Commercial Temp.
NM93C46TEM8 Extended Temp.

Alternate SO Pinout (TM8)



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See NS Package M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06–NM93C66	0°C to +70°C
NM93C06E–NM93C66E	−40°C to +85°C
NM93C06M–NM93C66M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified)

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = 0V		50 50 100	μA
I_{IL}	Input Leakage	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93C06–NM93C66 NM93C06E–NM93C66E NM93C06M–NM93C66M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	NM93C06E–NM93C66E NM93C06M–NM93C66M	I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M		0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 4) (Note 5)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	Relative to SK	50 50 100		ns
t_{DH}	D0 Hold Time		Relative to SK	10*		ns
t_{DIS}	DI Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M-NM93C66M	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

*t_{DH} = 70 ns for the NM93C06 and NM93C46

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended temperature range parts specifies a minimum SK clock period of 1 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 μs; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial and Extended temperature range parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERASE ALL instruction is not required, see note below.

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

NOTE: The NM93C06/C46/C56/C66 devices do not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

Instruction Set for the NM93C06 and NM93C46

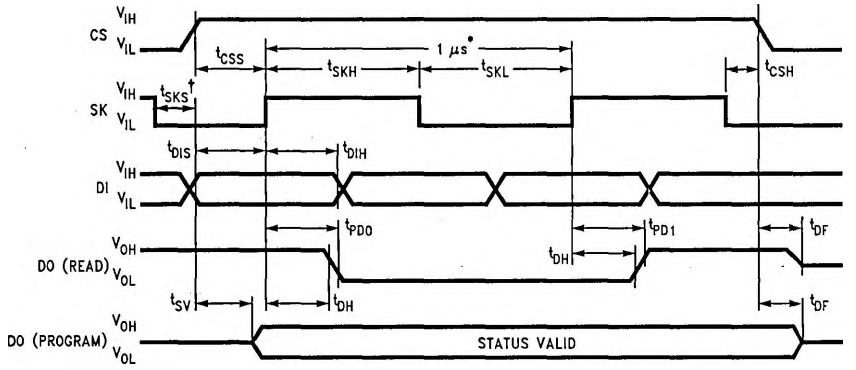
Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

Instruction Set for the NM93C56 and NM93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



*This is the minimum SK period (Note 2).
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

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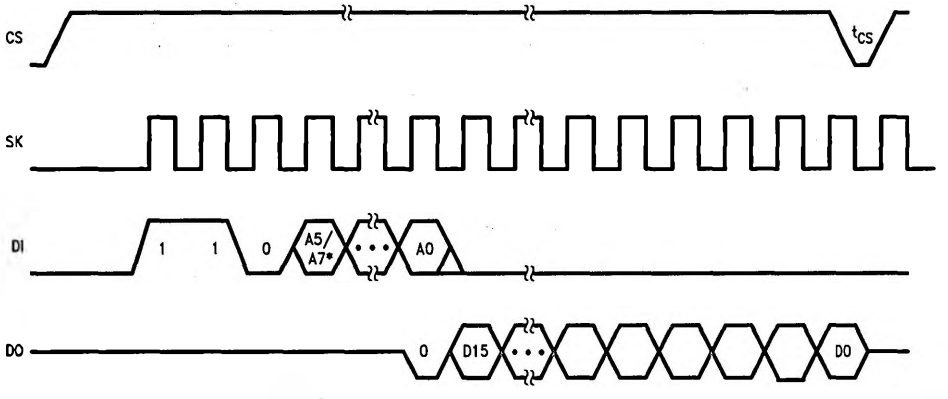
READ:



*Address bits A_5 and A_4 become "don't care" for NM93C06.
*Address bit A_7 becomes a "don't care" for NM93C56.

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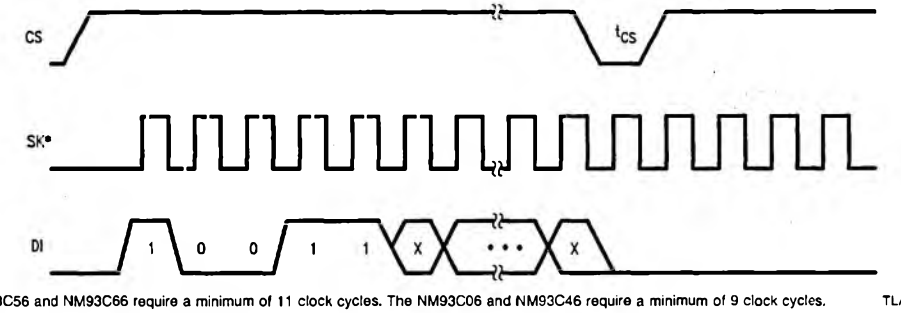
EWEN:



*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles.

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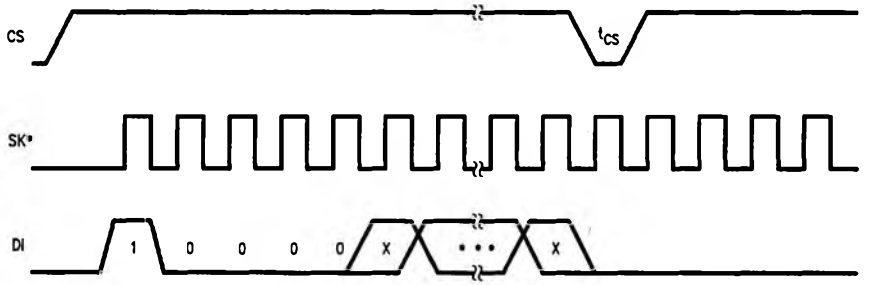
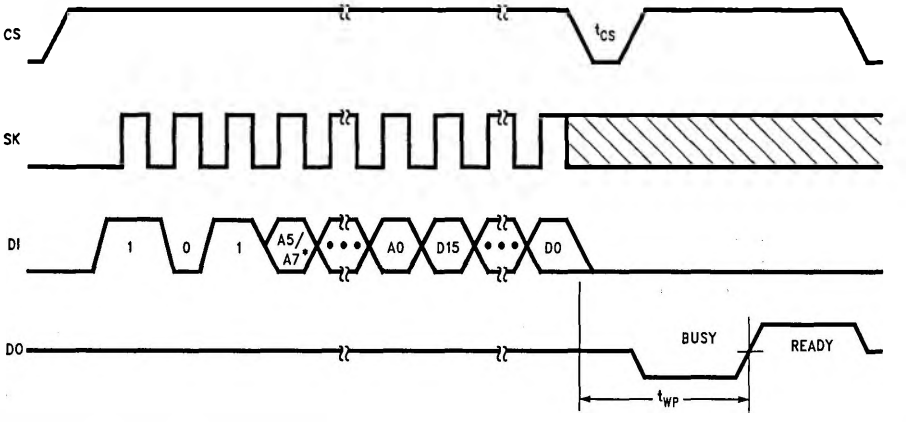
Timing Diagrams (Continued)

EWDS:



*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles. TL/D/10751–7

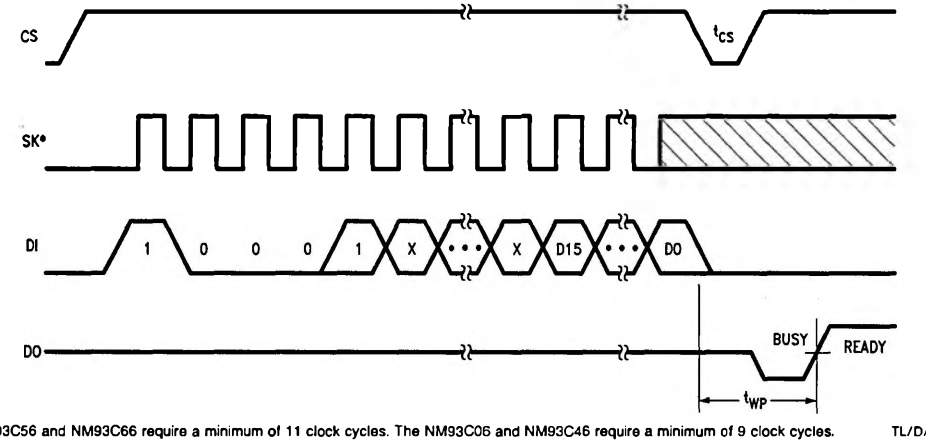
WRITE:



*Address bit A_5 and A_4 become "don't care" for NM93C06. TL/D/10751–8

*Address bit A_7 becomes a "don't care" for NM93C56.

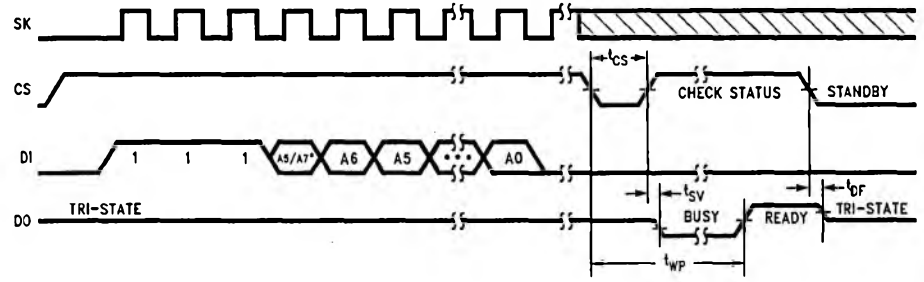
WRAL:†



*The NM93C56 and NM93C66 require a minimum of 11 clock cycles. The NM93C06 and NM93C46 require a minimum of 9 clock cycles. TL/D/10751–9

Timing Diagrams (Continued)

ERASE:



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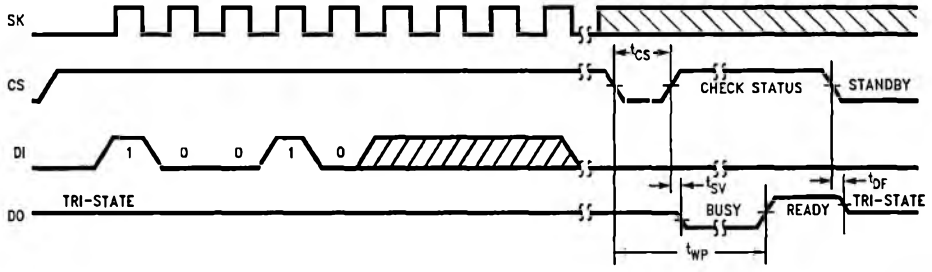
*Address bits A5 and A4 are "don't care" for NM93C06.

*Address bits A7 is "don't care" for NM93C56.

ERAL:



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