National Semiconductor

NM93CS06/CS46/CS56/CS66 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

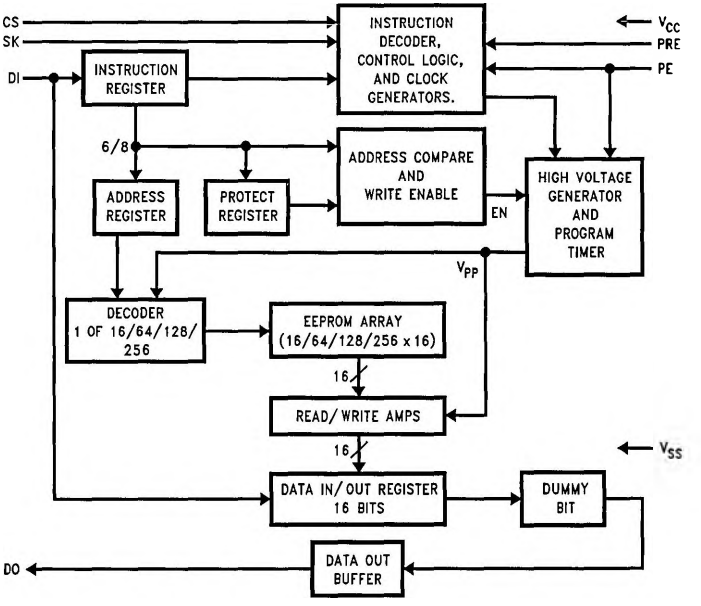
The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 registers of 16 bits each. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE™ compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μA and standby current of 25 μA
- Direct write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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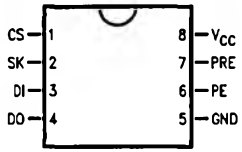
Connection Diagrams

PIN OUT:

Dual-In-Line Package (N) and 8-Pin SO (M8)*



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Top View

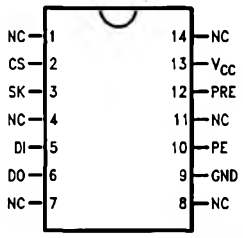
See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



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Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93CS06N/NM93CS46N/NM93CS56N/NM93CS66N
NM93CS06M8/NM93CS46M8/NM93CS56M8/NM93CS66M*

Extended Temp. Range (−40°C to +85°C)

Order Number*
NM93CS06EN/NM93CS46EN/NM93CS56EN/NM93CS66EN
NM93CS06EM8/NM93CS46EM8/NM93CS56EM8/NM93CS66EM*

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93CS06MN/NM93CS46MN/NM93CS56MN/NM93CS66MN
NM93CS06MM8/NM93CS46MM8/NM93CS56MM8

*The NM93CS66 is available in 8-Pin DIP and 14-Pin SO only.

Note: For 14-pin SO availability on the 93CS06, CS46 and CS56, contact your local National Semiconductor Sales Office.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxx	0°C to +70°C
NM93CSxxE	−40°C to +85°C
NM93CSxxM	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	CS = 0V		50 50 100	μA
I_{IL}	Input Leakage	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	V_{IN} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
I_{OL}	Output Leakage	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	V_{OUT} = 0V to V_{CC}	−2.5 −10 −10	2.5 10 10	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1}	Output Low Voltage	NM93CS06E-NM93CS66E NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage	NM93CS06M-NM93CS66M	I_{OH} = −400 μA	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M		0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 2) (Note 2) (Note 3)	250 300 500		ns
t_{SKL}	SK Low Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 2) (Note 2) (Note 3)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	(Note 4) (Note 4) (Note 5)	250 250 500		ns
t_{CSS}	CS Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to SK	50 50 100		ns
t_{PRES}	PRE Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M-NM93CS66M	Relative to SK	50 50 100		ns

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DH}	DO Hold Time		Relative to SK	10		ns
t_{PES}	PE Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to SK	50 50 100		ns
t_{DIS}	DI Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to SK	100 100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	Relative to CS Relative to CS Relative to CS	250 250 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	AC Test CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial and Extended parts specifies a minimum SK clock period of 1 microsecond; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 1 microsecond. For example, if t_{SKL} = 250 ns, then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Military Temperature parts specifies a minimum SK clock period of 2 microseconds; therefore, in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns, then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial and Extended parts, CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Military Temperature parts, CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93CSxx EEPROM Family has 10 instructions as described below. Note that there is a difference in the length of the instruction for the NM93CS06 and NM93CS46 vs. the NM93CS56 and NM93CS66. This is due to the fact that the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits (depending on device size) carry the op code and address. The address is either 6 or 8 bits depending on the device size.

Read and Sequential Register Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address sto in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **Immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **Immediately** precede a PRCLEAR instruction. The contents of the Protect Register will be read as 0's after a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **Immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **Immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06 and NM93CS46

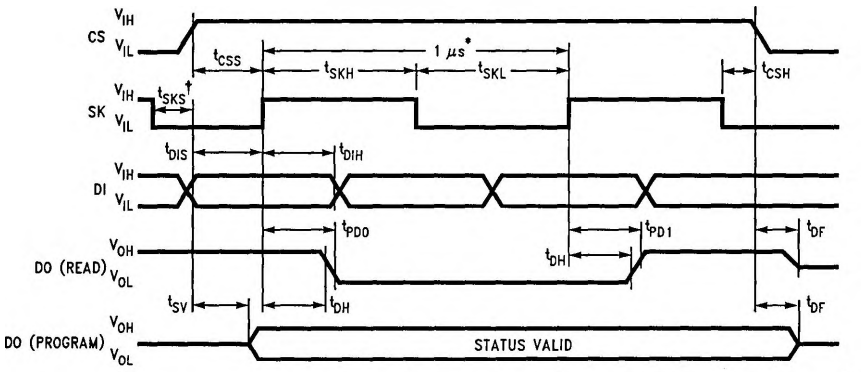
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE. Protect Register equals 0's.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Instruction Set for the NM93CS56 and NM93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE. Protect Register equals 0's.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

Synchronous Data Timing



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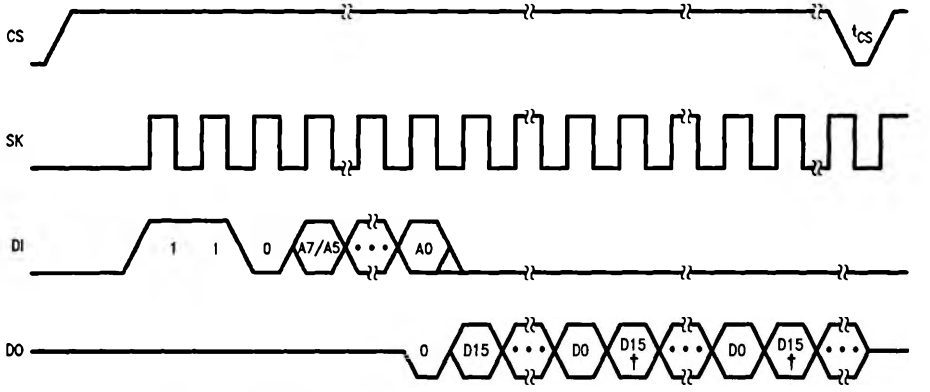
*This is the minimum SK period (Note 2).

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ:
PRE = 0, PE = X



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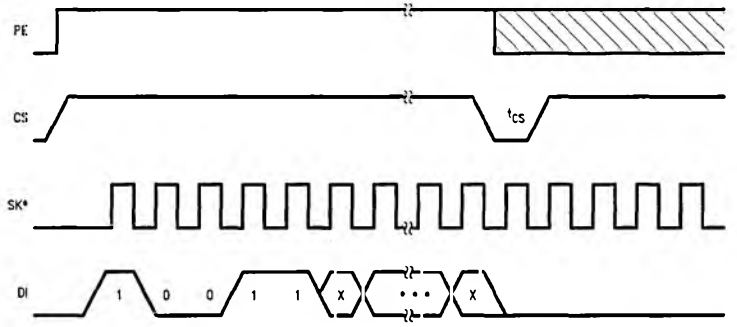
*Address bit A7 becomes "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

†The memory automatically cycles to the next register.

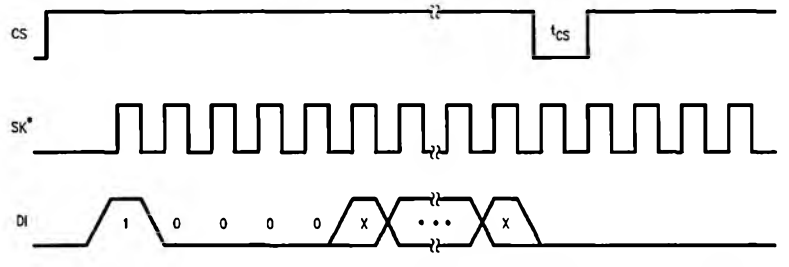
Timing Diagrams (Continued)

WEN:
PRE = 0, DO = TRI-STATE



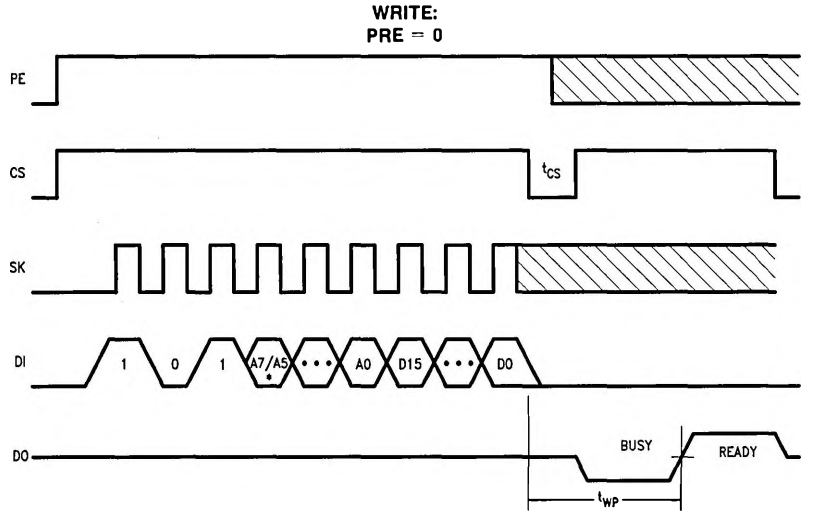
*The NM93CS56 and NM93CS66 require a minimum of 11 clocks cycles. The NM93CS06 and NM93CS46 require a minimum of 9 clock cycles.

WDS:
PRE = 0, PE = X, DO = TRI-STATE



*The NM93CS56 and NM93CS66 require a minimum of 11 clocks cycles. The NM93CS06 and NM93CS46 require a minimum of 9 clock cycles.

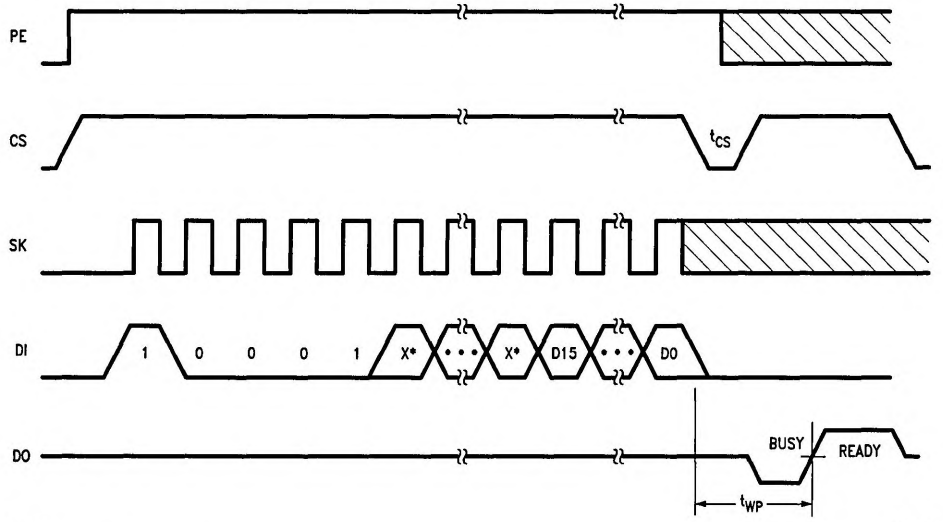
WRITE:
PRE = 0



*Address bit A7 becomes a "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

Timing Diagrams (Continued)

WRALL†:
PRE = 0



*Don't care

†Protect Register **MUST** be cleared.

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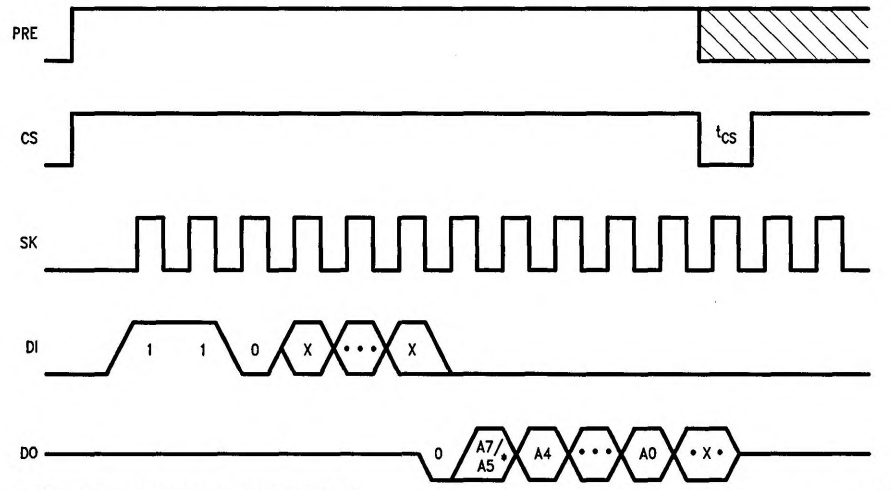
PRREAD:
PE = X



*Address bits A5 and A4 become "don't cares" for NM93CS06.

*Address bit A7 becomes "don't care" for NM93CS56.

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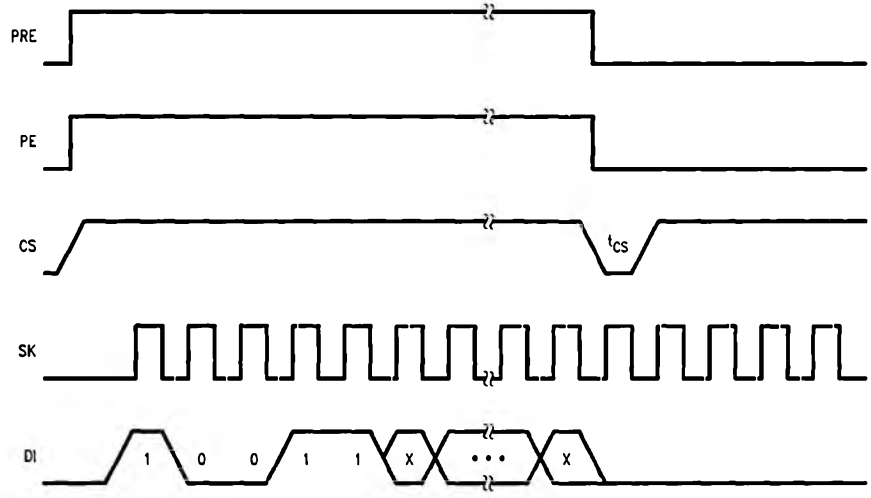
Timing Diagrams (Continued)

PREN*:
DO = TRI-STATE



*A WEN cycle must precede a PREN cycle.

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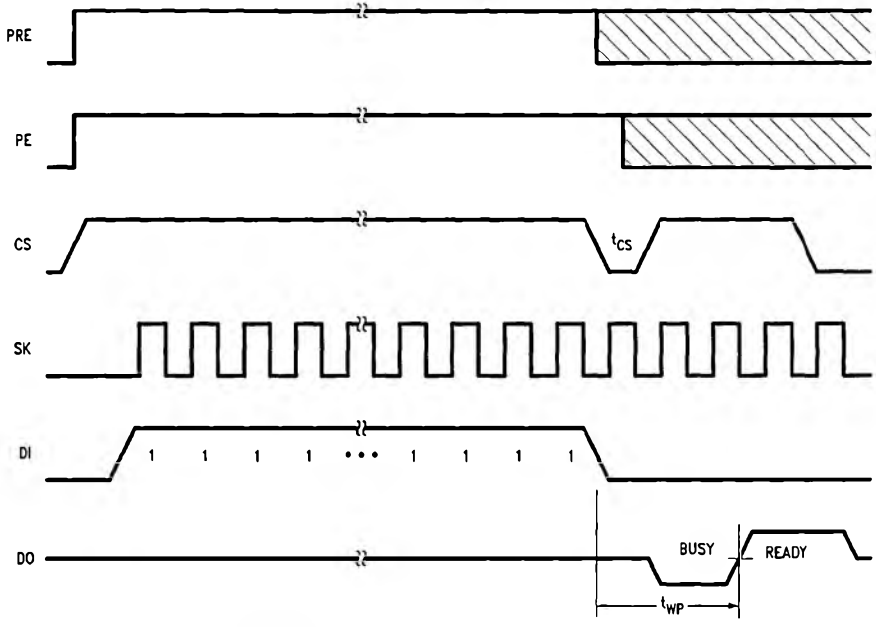
PRCLEAR*:



*A PREN cycle must **immediately** precede a PRCLEAR cycle.

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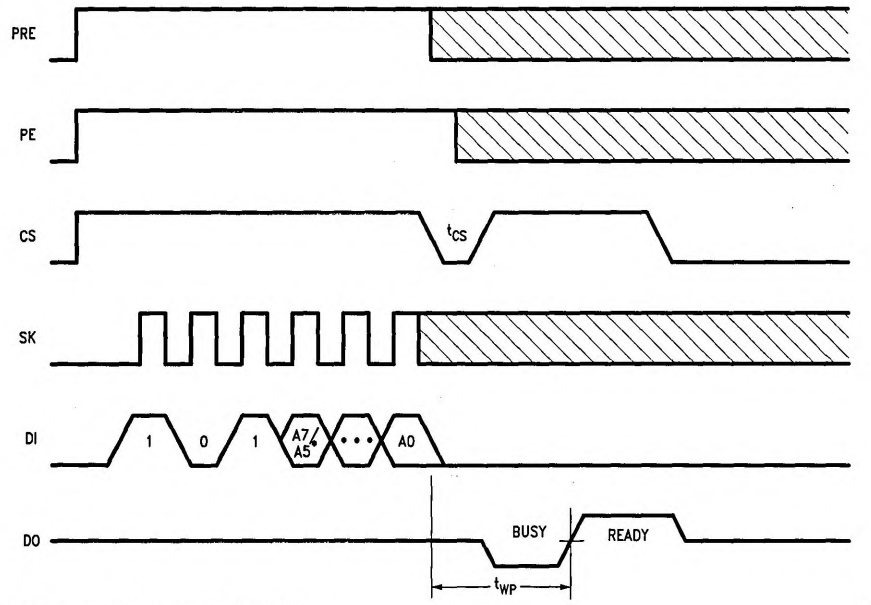
Timing Diagrams (Continued)

PRWRITE†:



*Address bit A7 becomes a "don't care" for NM93CS56.
*Address bits A5 and A4 become "don't cares" for NM93CS06.

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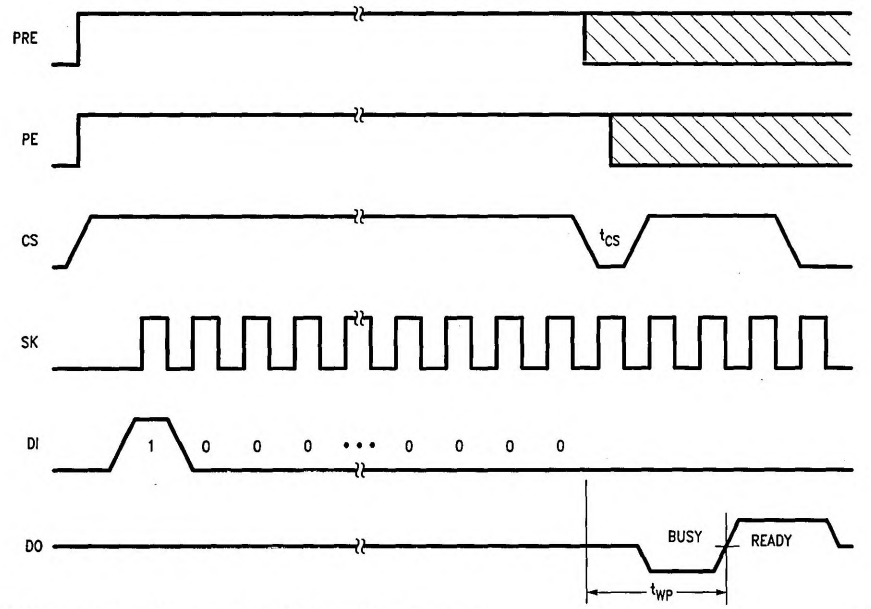
†Protect Register **MUST** be cleared before a PRWRITE cycle. A PREN cycle must **immediately** precede a PRWRITE cycle.

PRDS*:



***ONE TIME ONLY** instruction. A PREN cycle must **immediately** precede a PRDS cycle.

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