NT512D64S8HBAFM
512MB : 64M x 64
PC2700 / PC2100 Unbuffered DDR SO-DIMM

200pin Unbuffered DDR SO-DIMM Based on DDR333/266 32Mx8 SDRAM

Features

• 200-Pin Small Outline Dual In-Line Memory Module (SO-DIMM)
• 64Mx64 Double Unbuffered DDR SO-DIMM based on 32Mx8 DDR SDRAM.
• Performance:

	PC2700	PC2100	Unit
Speed Sort	-6K	-75B	
DIMM $\overline{CAS}$ Latency	2.5	2.5	
f_{CK} Clock Frequency	166	133	MHz
t_{CK} Clock Cycle	6	7.5	ns
f_{DQ} DQ Burst Frequency	333	266	MHz

• Intended for 133 MHz and 166 MHz applications
• Inputs and outputs are SSTL-2 compatible
• V_{DD} = 2.5Volt ± 0.2, V_{DDQ} = 2.5Volt ± 0.2
• SDRAMs have 4 internal banks for concurrent operation
• Module has two physical banks
• Differential clock inputs
• Data is read or written on both clock edges
• DRAM DLL aligns DQ and DQS transitions with clock transitions.
• Address and control signals are fully synchronous to positive clock edge
• Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 2, 2.5
  - Burst Type: Sequential or Interleave
  - Burst Length: 2, 4, 8
  - Operation: Burst Read and Write
• Auto Refresh (CBR) and Self Refresh Modes
• Automatic and controlled precharge commands
• 13/10/2 Addressing (row/column/bank)
• 7.8 μs Max. Average Periodic Refresh Interval
• Serial Presence Detect
• Gold contacts
• SDRAMs in 60-ball CSP Package

Description

NT512D64S8HBAFM is an unbuffered 200-Pin Double Data Rate (DDR) Synchronous DRAM Small Outline Dual In-Line Memory Module (SO-DIMM), organized as a two-bank 64Mx64 high-speed memory array. The module uses sixteen 32Mx8 DDR SDRAMs in 60-ball CSP packages. All NANYA DDR SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 2.66" long space-saving footprint. The DIMM is intended for use in applications operating up to 166 MHz clock speeds and achieves high-speed data transfer rates of up to 333 MHz. Prior to any access operation, the device $\overline{CAS}$ latency and burst type/ length/operation type must be programmed into the DIMM by address inputs A0-A12 and I/O inputs BA0 and BA1 using the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power
NT512D64S8HBAFM-6K	166MHz (6ns @ CL = 2.5)	DDR333	PC2700	64Mx64	Gold	2.5V
	133MHz (7.5ns @ CL = 2)					
NT512D64S8HBAFM-75B	133MHz (7.5ns @ CL = 2.5)	DDR266B	PC2100			
	100MHz (10ns @ CL = 2)					

Pin Description

CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	Differential Clock Inputs.	DQ0-DQ63	Data input/output
CKE0, CKE1	Clock Enable	DQS0-DQS7, DQS9-DQS16	Bidirectional data strobes
$\overline{RAS}$	Row Address Strobe		
$\overline{CAS}$	Column Address Strobe	VDD	Power (2.5V)
$\overline{WE}$	Write Enable	VDDQ	Supply voltage for DQs (2.5V)
$\overline{S0}$, $\overline{S1}$	Chip Selects	VSS	Ground
A0-A9, A11, A12	Address Inputs	NC	No Connect
A10/AP	Address Input/Autoprecharge	SCL	Serial Presence Detect Clock Input
BA0, BA1	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
VREF	Ref. Voltage for SSTL_2 inputs	SA0-2	Serial Presence Detect Address Inputs
VDDID	VDD Identification flag.	VDDSPD	Serial EEPROM positive power supply (2.5V)

Pinout

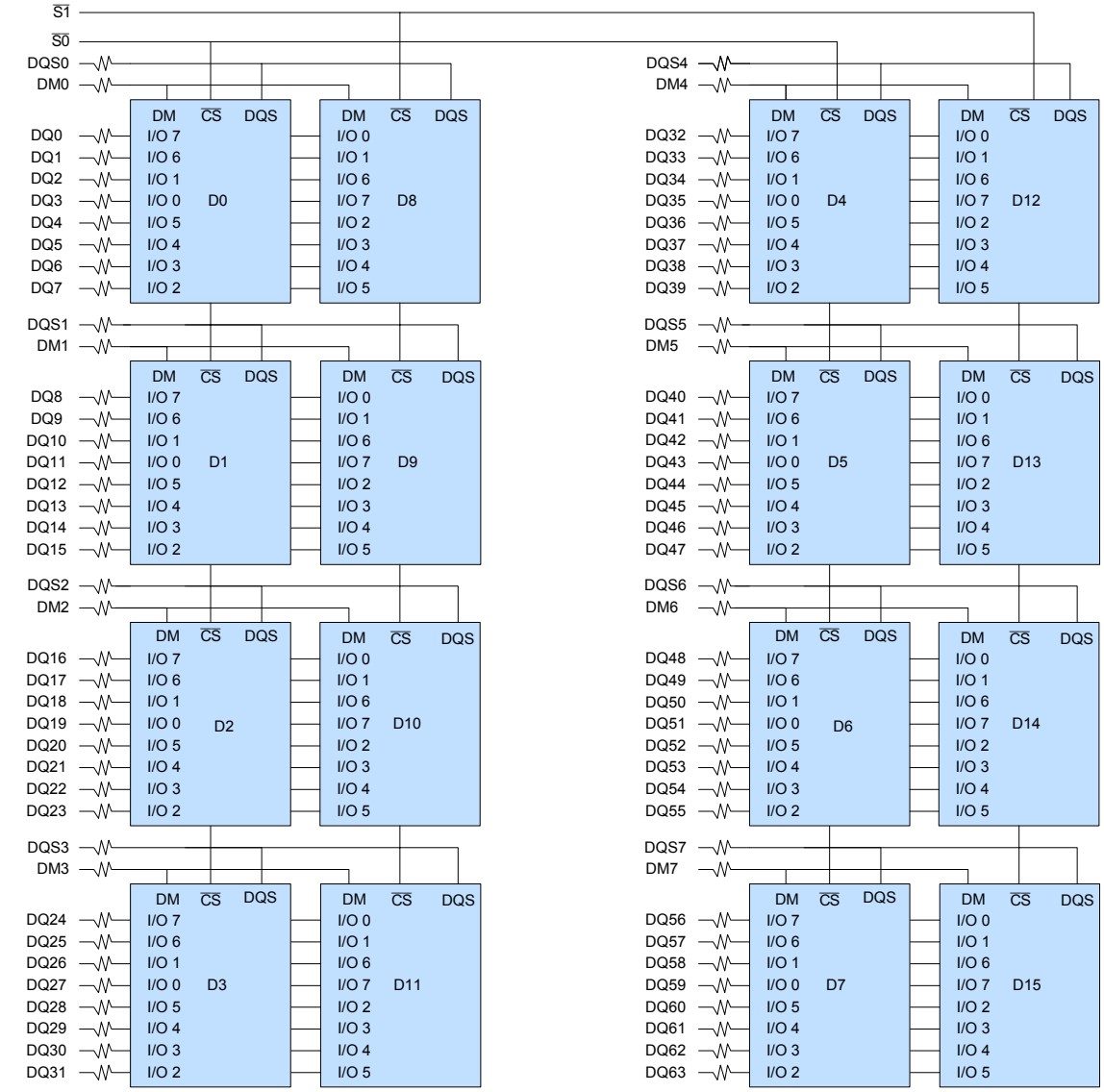
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREF	2	VREF	51	VSS	52	VSS	101	A9	102	A8	151	DQ42	152	DQ46
3	VSS	4	VSS	53	DQ19	54	DQ23	103	VSS	104	VSS	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	VDD	156	VDD
7	DQ1	8	DQ5	57	VDD	58	VDD	107	A5	108	A4	157	VDD	158	$\overline{CK1}$
9	VDD	10	VDD	59	DQ25	60	DQ29	109	A3	110	A2	159	VSS	160	CK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	VSS	162	VSS
13	DQ2	14	DQ6	63	VSS	64	VSS	113	VDD	114	VDD	163	DQ48	164	DQ52
15	VSS	16	VSS	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	VDD	118	$\overline{RAS}$	167	VDD	168	VDD
19	DQ8	20	DQ12	69	VDD	70	VDD	119	$\overline{WE}$	120	$\overline{CAS}$	169	DQS6	170	DM6
21	VDD	22	VDD	71	NC	72	NC	121	$\overline{S0}$	122	$\overline{S1}$	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	NC	74	NC	123	DU	124	DU	173	VSS	174	VSS
25	DQS1	26	DM1	75	VSS	76	VSS	125	VSS	126	VSS	175	DQ51	176	DQ55
27	VSS	28	VSS	77	DQS8	78	NC	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	NC	80	NC	129	DQ33	130	DQ37	179	VDD	180	VDD
31	DQ11	32	DQ15	81	VDD	82	VDD	131	VDD	132	VDD	181	DQ57	182	DQ61
33	VDD	34	VDD	83	NC	84	NC	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CK0	36	VDD	85	DU	86	DU	135	DQ34	136	DQ38	185	VSS	186	VSS
37	$\overline{CK0}$	38	VSS	87	VSS	88	VSS	137	VSS	138	VSS	187	DQ58	188	DQ62
39	VSS	40	VSS	89	CK2	90	VSS	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	$\overline{CK2}$	92	VDD	141	DQ40	142	DQ44	191	VDD	192	VDD
43	DQ17	44	DQ21	93	VDD	94	VDD	143	VDD	144	VDD	193	SDA	194	SA0
45	VDD	46	VDD	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	DU	98	DU	147	DQS5	148	DM5	197	VDDSPD	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	VSS	150	VSS	199	VDDID	200	DU

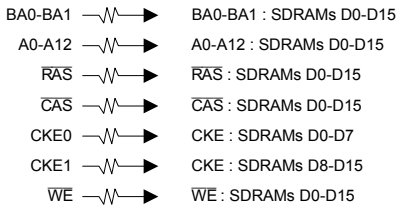
Note: All pin assignments are consistent for all 8-byte unbuffered versions.

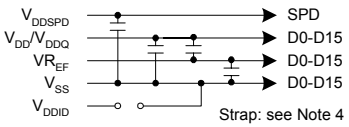
Input/Output Functional Description

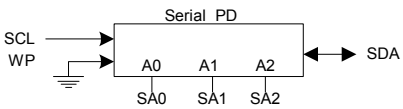
Symbol	Type	Polarity	Function
CK0, CK1, CK2, $\overline{CK0}$, $\overline{CK1}$, $\overline{CK2}$	(SSTL)	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of CK. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	(SSTL)	Active High	Activates the DDR SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	(SSTL)	Active Low	Enables the associated DDR SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by S0; Bank 1 is selected by S1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	(SSTL)	Active Low	When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL-2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0, BA1	(SSTL)	-	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP A11, A12	(SSTL)	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge.
DQ0 - DQ63	(SSTL)	-	Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs.
DQS0 - DQS7, DQS9 – DQS16	(SSTL)	Active High	Data strobes: Output with read data, input with write data. Edge aligned with read data, centered on write data. Used to capture write data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
SA0 – SA2		-	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA		-	This bi-directional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply.

Functional Block Diagram (2 Bank, 32Mx8 DDR SDRAMs)









Notes :

1. DQ-to-I/O wring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships are maintained as shown.
3. DQ/DQS/DM/DQS resistors are 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): V_{DD} is not equal to V_{DDQ}.

Serial Presence Detect -- Part 1 of 2

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 2.5V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		DDR333 -6K	DDR266B -75B	DDR333 -6K	DDR266B -75B	
0	Number of Serial PD Bytes Written during Production	128		80		
1	Total Number of Bytes in Serial PD device	256		08		
2	Fundamental Memory Type	SDRAM DDR		07		
3	Number of Row Addresses on Assembly	13		0D		
4	Number of Column Addresses on Assembly	10		0A		
5	Number of DIMM Bank	2		02		
6	Data Width of Assembly	X64		40		
7	Data Width of Assembly (cont')	X64		00		
8	Voltage Interface Level of this Assembly	SSTL 2.5V		04		
9	DDR SDRAM Device Cycle Time at CL=2.5	6ns	7.5ns	60	75	
10	DDR SDRAM Device Access Time from Clock at CL=2.5	0.7ns	0.75ns	70	75	
11	DIMM Configuration Type	Non-Parity		00		
12	Refresh Rate/Type	SR/1x(7.8us)		82		
13	Primary DDR SDRAM Width	X8		08		
14	Error Checking DDR SDRAM Device Width	N/A		00		
15	DDR SDRAM Device Attr: Min CLK Delay, Random Col Access	1 Clock		01		
16	DDR SDRAM Device Attributes: Burst Length Supported	2,4,8		0E		
17	DDR SDRAM Device Attributes: Number of Device Banks	4		04		
18	DDR SDRAM Device Attributes: CAS Latencies Supported	2/2.5	2/2.5	0C	0C	
19	DDR SDRAM Device Attributes: CS Latency	0		01		
20	DDR SDRAM Device Attributes: WE Latency	1		02		
21	DDR SDRAM Device Attributes:	Differential Clock		20		
22	DDR SDRAM Device Attributes: General	+/-0.2V Voltage Tolerance		00		
23	Minimum Clock Cycle at CL=2	7.5ns	10ns	75	A0	
24	Maximum Data Access Time from Clock at CL=2	0.70ns	0.75ns	70	75	
25	Minimum Clock Cycle Time at CL=1	N/A		00		
26	Maximum Data Access Time from Clock at CL=1	N/A		00		
27	Minimum Row Precharge Time (t_{RP})	18ns	20ns	48	50	
28	Minimum Row Active to Row Active delay (t_{RRD})	12ns	15ns	30	3C	
29	Minimum RAS to CAS delay (t_{RCD})	18ns	20ns	48	50	
30	Minimum RAS Pulse Width (t_{RAS})	42ns	45ns	2A	2D	
31	Module Bank Density	256MB		40		
32	Address and Command Setup Time Before Clock	0.75ns	0.9ns	75	90	
33	Address and Command Hold Time After Clock	0.75ns	0.9ns	75	90	
34	Data Input Setup Time Before Clock	0.45ns	0.5ns	45	50	
35	Data Input Hold Time After Clock	0.45ns	0.5ns	45	50	
36-61	Reserved	Undefined		00		
62	SPD Revision	Initial	Initial	00	00	
63	Checksum Data			0B	C0	

Serial Presence Detect -- Part 2 of 2

64Mx64 SDRAM DIMM based on 32Mx8, 4Banks, 8K Refresh, 2.5V DDR SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		DDR333 -6K	DDR266B -75B	DDR333 -6K	DDR266B -75B	
64-71	Manufacturer's JEDEC ID Code	NANYA		7F7F7F0B00000000		
72	Module Manufacturing Location	N/A		00		
73-90	Module Part number	N/A	N/A	00	00	
91-92	Module Revision Code	N/A		00		
93-94	Module Manufacturing Data	Year/Week Code		yy/ww		1, 2
95-98	Module Serial Number	Serial Number		00		
99-255	Reserved	Undefined		00		

1. yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex)
2. ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{IN}, V_{OUT}	Voltage on I/O pins relative to Vss	-0.5 to VDDQ+0.5	V
V_{IN}	Voltage on Input relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.5 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.5 to +3.6	V
T_A	Operating Temperature (Ambient)	0 to +70	°C
T_{STG}	Storage Temperature (Plastic)	-55 to +150	°C
P_D	Power Dissipation	16	W
I_{OUT}	Short Circuit Output Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Capacitance

Parameter	Symbol	Max.	Units	Notes
Input Capacitance: CK0, $\overline{CK0}$, CK1, $\overline{CK1}$, CK2, $\overline{CK2}$	C_{I1}	24	pF	1
Input Capacitance: A0-A11, BA0, BA1, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, CKE0, $\overline{S0}$	C_{I2}	60	pF	1
Input Capacitance: SA0-SA2, SCL	C_{I4}	9	pF	1
Input Capacitance: CKE0, CKE1, $\overline{S0}$, $\overline{S1}$	C_{I5}	30	pF	1
Input/Output Capacitance DQ0-63; DQS0-7, 9-16	C_{IO1}	14	pF	1, 2
Input/Output Capacitance: SDA	C_{IO3}	11	pF	

1. V_{DDQ} = V_{DD} = 2.5V ± 0.2V, f = 100 MHz, T_A = 25 °C, V_{OUT} (DC) = V_{DDQ}/2, V_{OUT} (Peak to Peak) = 0.2V.
2. DQS inputs are grouped with I/O pins reflecting the fact that they are matched in loading to DQ and DQS to facilitate trace matching at the board level.

DC Electrical Characteristics and Operating Conditions

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	Supply Voltage	2.3	2.7	V	1
V_{DDQ}	I/O Supply Voltage	2.3	2.7	V	1
V_{SS}, V_{SSQ}	Supply Voltage, I/O Supply Voltage	0	0	V	
V_{REF}	I/O Reference Voltage	0.49 x V_{DDQ}	0.51 x V_{DDQ}	V	1, 2
V_{TT}	I/O Termination Voltage (System)	V_{REF} – 0.04	V_{REF} + 0.04	V	1, 3
V_{IH} (DC)	Input High (Logic1) Voltage	V_{REF} + 0.15	V_{DDQ} + 0.3	V	1
V_{IL} (DC)	Input Low (Logic0) Voltage	-0.3	V_{REF}- 0.15	V	1
V_{IN} (DC)	Input Voltage Level, CK and $\overline{CK}$ Inputs	-0.3	V_{DDQ} + 0.3	V	1
V_{ID} (DC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.30	V_{DDQ} + 0.6	V	1, 4
I_I	Input Leakage Current Any input 0V ≤ V_{IN} ≤ V_{DD}; (All other pins not under test = 0V)	-10	10	uA	1
I_{OZ}	Output Leakage Current (DQs are disabled; 0V ≤ V_{out} ≤ V_{DDQ}	-10	10	uA	1
I_{OH}	Output High Current (V_{OUT} = V_{DDQ} -0.373V, min V_{REF}, min V_{TT})	-16.8	-	mA	1
I_{OL}	Output Low Current (V_{OUT} = 0.373, max V_{REF}, max V_{TT})	16.8	-	mA	1

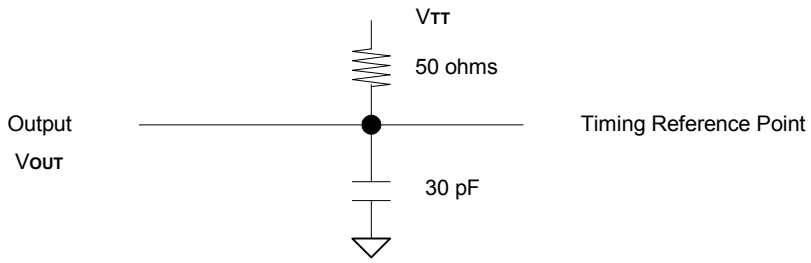
1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} is not applied directly to the DIMM. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
4. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

AC Characteristics

(Notes 1-5 apply to the following Tables; Electrical Characteristics and DC Operating Conditions, AC Operating Conditions, Operating, Standby, and Refresh Currents, and Electrical Characteristics and AC Timing.)

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical, AC and DC characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load. Refer to the AC Output Load Circuit below.
4. AC timing and I_{DD} tests may use a V_{IL} to V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK, $\overline{CK}$), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals is 1V/ns in the range between V_{IL} (AC) and V_{IH} (AC) unless otherwise specified.
5. The AC and DC input level specifications are as defined in the SSTL_2 Standard (i.e. the receiver effectively switches as a result of the signal crossing the AC input level, and remains in that state as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.

AC Output Load Circuits



AC Operating Conditions

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
V_{IH} (AC)	Input High (Logic 1) Voltage.	V_{REF} + 0.31		V	1, 2
V_{IL} (AC)	Input Low (Logic 0) Voltage.		V_{REF} - 0.31	V	1, 2
V_{ID} (AC)	Input Differential Voltage, CK and $\overline{CK}$ Inputs	0.62	V_{DDQ} + 0.6	V	1, 2, 3
V_{IX} (AC)	Input Differential Pair Cross Point Voltage, CK and $\overline{CK}$ Inputs	(0.5*V_{DDQ}) - 0.2	(0.5*V_{DDQ}) + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics)

Symbol	Parameter/Condition	PC2700 (-6K)	PC2100 (-75B)	Unit	Notes
I_{DD0}	Operating Current: one bank; active/precharge; t_{RC} = t_{RC} (MIN); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1100	920	mA	1, 2
I_{DD1}	Operating Current: one bank; active/read/precharge; Burst = 2; t_{RC} = t_{RC} (MIN); CL=2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA; address and control inputs changing once per clock cycle	1250	1080	mA	1, 2
I_{DD2P}	Precharge Power-Down Standby Current: all banks idle; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	210	180	mA	1, 2
I_{DD2N}	Idle Standby Current: CS ≥ V_{IH} (MIN); all banks idle; CKE ≥ V_{IH} (MIN); t_{CK} = t_{CK} (MIN); address and control inputs changing once per clock cycle	550	480	mA	1, 2
I_{DD3P}	Active Power-Down Standby Current: one bank active; power-down mode; CKE ≤ V_{IL} (MAX); t_{CK} = t_{CK} (MIN)	220	190	mA	1, 2
I_{DD3N}	Active Standby Current: one bank; active/precharge; CS ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	720	620	mA	1, 2
I_{DD4R}	Operating Current: one bank; Burst = 2; reads; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 2.5; t_{CK} = t_{CK} (MIN); I_{OUT} = 0mA	1900	1700	mA	1, 2
I_{DD4W}	Operating Current: one bank; Burst = 2; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL=2.5; t_{CK} = t_{CK} (MIN)	1460	1200	mA	1, 2
I_{DD5}	Auto-Refresh Current: t_{RC} = t_{RFC} (MIN)	2100	1800	mA	1, 2, 4
I_{DD6}	Self-Refresh Current: CKE ≤ 0.2V	48	48	mA	1, 2
I_{DD7}	Operating Current: four bank; four bank interleaving with BL = 4, address and control inputs randomly changing; 50% of data changing at every transfer; t_{RC} = t_{RC} (min); I_{OUT} = 0mA.	3100	2500	mA	1, 2

1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate = 1V/ ns.
3. Enables on-chip refresh and address counters.
4. Current at 7.8 µs is time averaged value of I_{DD5} at t_{RFC} (MIN) and I_{DD2P} over 7.8 µs.

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 1 of 2)

Symbol	Parameter		-6K		-75B		Unit	Notes
			Min.	Max.	Min.	Max.		
tAC	DQ output access time from CK/$\overline{CK}$		-0.7	+0.7	-0.75	+0.75	ns	1-4
tDQSCK	DQS output access time from CK/$\overline{CK}$		-0.7	+0.7	-0.75	+0.75	ns	1-4
tCH	CK high-level width		0.45	0.55	0.45	0.55	tCK	1-4
tCL	CK low-level width		0.45	0.55	0.45	0.55	tCK	1-4
tCK	Clock cycle time	CL=2.5	6	12	7.5	12	ns	1-4
tCK		CL=2	7.5	12	10	12	ns	1-4
tDH	DQ and DM input hold time		0.45		0.5		ns	1-4, 15, 16
tDS	DQ and DM input setup time		0.45		0.5		ns	1-4, 15, 16
tDIPW	DQ and DM input pulse width (each input)		1.75		1.75		ns	1-4
tHZ	Data-out high-impedance time from CK/$\overline{CK}$		-0.7	+0.7	-0.75	+0.75	ns	1-4, 5
tLZ	Data-out low-impedance time from CK/$\overline{CK}$		-0.7	+0.7	-0.75	+0.75	ns	1-4, 5
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)			0.45		0.5	ns	1-4
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time		tCH or tCL		tCH or tCL		tCK	1-4
tQH	Data output hold time from DQS		tHP - tQHS		tHP - tQHS		tCK	1-4
tQHS	Data hold Skew Factor			0.55ns		0.75ns	tCK	1-4
tDQSS	Write command to 1st DQS latching transition		0.75	1.25	0.75	1.25	tCK	1-4
tDQSL,H	DQS input low (high) pulse width (write cycle)		0.35		0.35		tCK	1-4
tDSS	DQS falling edge to CK setup time (write cycle)		0.2		0.2		tCK	1-4
tDSH	DQS falling edge hold time from CK (write cycle)		0.2		0.2		tCK	1-4
tMRD	Mode register set command cycle time		2		2		tCK	1-4
tWPRES	Write preamble setup time		0		0		ns	1-4, 7
tWPST	Write postamble		0.40	0.60	0.40	0.60	tCK	1-4, 6
tWPRE	Write preamble		0.25		0.25		tCK	1-4
tIH	Address and control input hold time (fast slew rate)		0.75		0.9		ns	2-4, 9, 11, 12
tIS	Address and control input setup time (fast slew rate)		0.75		0.9		ns	2-4, 9, 11, 12
tIH	Address and control input hold time (slow slew rate)		0.8		1.0		ns	2-4, 10, 11, 12, 14

AC Timing Specifications for DDR SDRAM Devices Used on Module

(TA = 0 °C ~ 70 °C; V_{DDQ} = 2.5V ± 0.2V; V_{DD} = 2.5V ± 0.2V, See AC Characteristics) (Part 2 of 2)

Symbol	Parameter	-6K		-75B		Unit	Notes
		Min.	Max.	Min.	Max.		
tIS	Address and control input setup time (slow slewrate)	0.8		1.0		ns	2-4, 10-12, 14
tIPW	Input pulse width	2.2		2.2		ns	2-4, 12
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK	1-4
tRPST	Read postamble	0.40	0.60	0.40	0.60	tCK	1-4
tRAS	Active to Precharge command	42	120,000	45	120,000	ns	1-4
tRC	Active to Active/Auto-refresh command period	60		65		ns	1-4
tRFC	Auto-refresh to Active/Auto-refresh command period	72		75		ns	1-4
tRCD	Active to Read or Write delay	18		20		ns	1-4
tRAP	Active to Read Command with Autoprecharge	18		20		ns	1-4
tRP	Precharge command period	18		20		ns	1-4
tRRD	Active bank A to Active bank B command	12		15		ns	1-4
tWR	Write recovery time	15		15		ns	1-4
tDAL	Auto precharge write recovery + precharge time	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	1-4, 13
tWTR	Internal write to read command delay	1		1		tCK	1-4
tPDEX	Power down exit time	6		7.5		ns	1-4
tXSNR	Exit self-refresh to non-read command	75		75		ns	1-4
tXSRD	Exit self-refresh to read command	200		200		tCK	1-4
tREFI	Average Periodic Refresh Interval		7.8		7.8	µs	1-4, 8

AC Timing Specification Notes

1. Input slew rate = 1V/ns.
2. The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross: the input reference level for signals other than CK/$\overline{CK}$ is V_{REF}.
3. Inputs are not recognized as valid until V_{REF} stabilizes.
4. The Output timing reference level, as measured at the timing reference point indicated in AC Characteristics (Note 3) is V_{TT}.
5. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
6. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
7. The specific requirement is that DQS be valid (high, low, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from high to low at this time, depending on tDQSS.
8. A maximum of eight Auto refresh commands can be posted to any given DDR SDRAM device.
9. For command/address input slew rate >= 1.0 V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
10. For command/address input slew rate >= 0.5 V/ns and < 1.0 V/ns. Slew rate is measured between V_{OH} (AC) and V_{OL} (AC).
11. CK/$\overline{CK}$ slew rates are >= 1.0 V/ns.
12. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester characterization.
13. For each of the terms in parentheses, if not already an integer, round to the next highest integer. t CK is equal to the actual system clock cycle time. For example, for PC2100 at CL= 2.5, t DAL = (15ns/7.5ns) +(20ns/7.0ns) = 2 + 3 = 5.
14. An input setup and hold time derating table is used to increase t IS and t IH in the case where the input slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (t_{IS})	Delta (t_{IH})	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+50	0	ps	1, 2
0.3 V/ns	+100	0	ps	1, 2

1. Input slew rate is based on the lesser of the slew rates determined by either V_{IH} (AC) to V_{IL} (AC) or V_{IH} (DC) to V_{IL} (DC), similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

15. An input setup and hold time derating table is used to increase t DS and t DH in the case where the I/O slew rate is below 0.5 V/ns.

Input Slew Rate	Delta (t_{DS})	Delta (t_{DH})	Unit	Note
0.5 V/ns	0	0	ps	1, 2
0.4 V/ns	+75	+75	ps	1, 2
0.3 V/ns	+150	+150	ps	1, 2

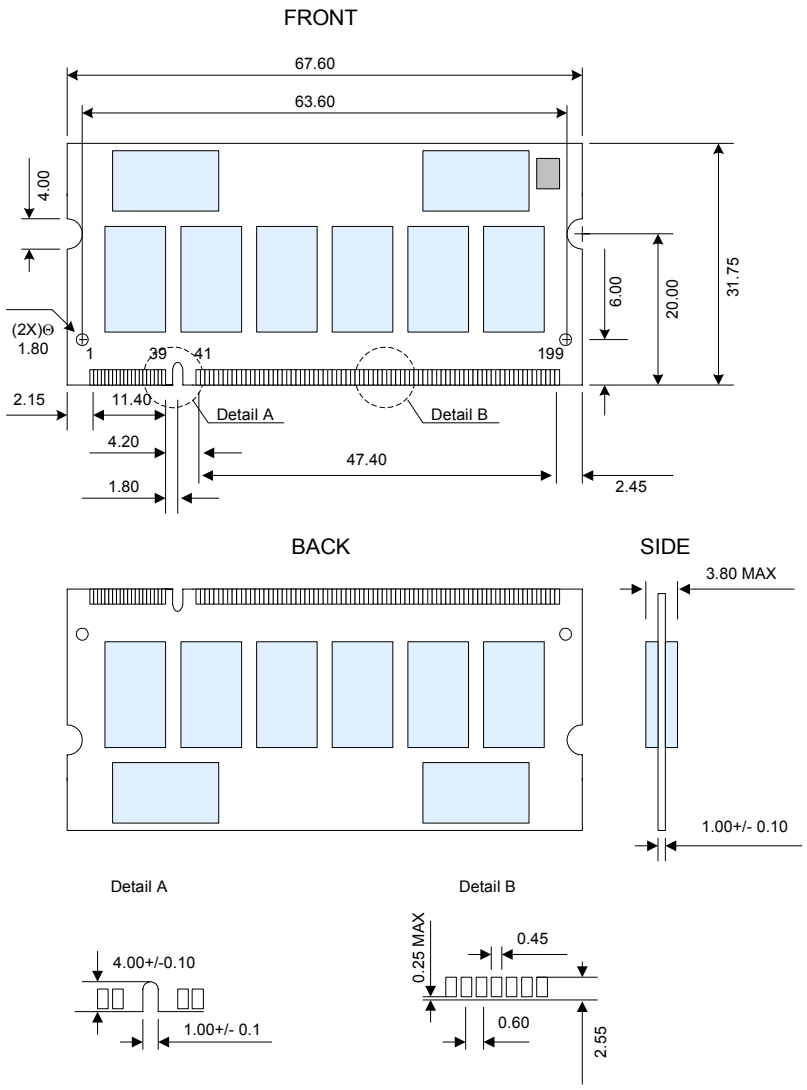
1. I/O slew rate is based on the lesser of the slew rates determined by either V_{IH} (AC) to V_{IL} (AC) or V_{IH} (DC) to V_{IL} (DC), similarly for rising transitions.
2. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

16. An I/O Delta Rise, Fall Derating table is used to increase t DS and t DH in the case where DQ, DM, and DQS slew rates differ.

Delta Rise and Fall Rate	Delta (t_{DS})	Delta (t_{DH})	Unit	Note
0.0 ns/V	0	0	ps	1-4
0.25 ns/V	+50	+50	ps	1-4
0.5 ns/V	+100	+100	ps	1-4

1. Input slew rate is based on the lesser of the slew rates determined by either V_{IH} (AC) to V_{IL} (AC) or V_{IH} (DC) to V_{IL} (DC), similarly for rising transitions.
2. Input slew rate is based on the larger of AC to AC delta rise, fall rate and DC to DC delta rise, fall rate.
3. The delta rise, fall rate is calculated as: [1/(slew rate 1)] - [1/(slew rate 2)]
   For example: slew rate 1 = 0.5 V/ns; slew rate 2 = 0.4 V/ns. Delta rise, fall = (1/0.5) - (1/0.4) [ns/V] = -0.5 ns/V
   Using the table above, this would result in an increase in t_{DS} and t_{DH} of 100 ps.
4. These derating parameters may be guaranteed by design or tester characterization and are not necessarily tested on each device.

Package Dimensions



Note: All dimensions are typical with tolerances of +/- 0.15 unless otherwise stated.

Units: Millimeters (Inches)

Revision Log

Rev	Date	Modification
0.1	01/2003	Preliminary Release
1.0	03/2003	Updated IDD values in Operating, Standby, and Refresh Currents Table
		Official Release