128Mbit DDR SDRAM

1M x 32Bit x 4 Banks
Double Data Rate Synchronous RAM
With Bi-directional Data Strobe and DLL
(144-Ball FBGA)

Nanya Technology Corp.

TABLE OF CONTENTS

1M x32Bit x4Banks Double Data Rate Synchronous RAM with Bi-directional Data Strobe and DLL

GENERAL DESCRIPTION

For 1M x 32Bit x 4 Bank DDR SDRAM

The NT5DT4M32EF is 134,217,728 bits of double data rate synchronous dynamic RAM organized as 4 x 1,048,576 bits by 32 I/Os. Synchronous features with Data Strobe allow extremely high performance up to 3.2GB/s/chip. I/O transactions are possible on both edges of the clock. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

FEATURES

- VDD = 2.5V±5% , VDDQ = 2.5V±5%
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 3, 4 (clock)
  - -. Burst length (2, 4, 8 and Full page)
  - -. Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the rising edge of the system clock
- Differential clock input(CK & /CK)
- Data I/O transaction on both edges of Data strobe
- 4 DQS (1 DQS/Byte)
- DLL aligns DQ and DQS transaction with Clock transaction
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & self refresh
- 32ms refresh period (4K cycle)
- 144-Ball FBGA package
- Maximum clock frequency up to 400MHz
- Maximum data rate up to 800Mbps/pin

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	Package
NT5DS4M32EF-25	400MHz	800Mbps/pin	SSTL_2	144-Ball FBGA
NT5DS4M32EF-28	350MHz	700Mbps/pin		
NT5DS4M32EF-33	300MHz	600Mbps/pin		
NT5DS4M32EF-4	250MHz	500Mbps/pin		

PIN CONFIGURATION (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	DQS0	DM0	VSSQ	DQ3	DQ2	DQ0	DQ31	DQ29	DQ28	VSSQ	DM3	DQS3
B	DQ4	VDDQ	NC	VDDQ	DQ1	VDDQ	VDDQ	DQ30	VDDQ	NC	VDDQ	DQ27
C	DQ6	DQ5	VSSQ	VSSQ	VSSQ	VDD	VDD	VSSQ	VSSQ	VSSQ	DQ26	DQ25
D	DQ7	VDDQ	VDD	VSS	VSSQ	VSS	VSS	VSSQ	VSS	VDD	VDDQ	DQ24
E	DQ17	DQ16	VDDQ	VSSQ	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	VSSQ	VDDQ	DQ15	DQ14
F	DQ19	DQ18	VDDQ	VSSQ	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	VSSQ	VDDQ	DQ13	DQ12
G	DQS2	DM2	NC	VSSQ	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	VSSQ	NC	DM1	DQS1
H	DQ21	DQ20	VDDQ	VSSQ	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	*VSS Thermal*	VSSQ	VDDQ	DQ11	DQ10
J	DQ22	DQ23	VDDQ	VSSQ	VSS	VSS	VSS	VSS	VSSQ	VDDQ	DQ9	DQ8
K	/CAS	/WE	VDD	VSS	A10	VDD	VDD	RFU1	VSS	VDD	NC	NC
L	/RAS	NC	NC	BA1	A2	A11	A9	A5	RFU2	CK	/CK	MCL
M	/CS	NC	BA0	A0	A1	A3	A4	A6	A7	A8/AP	CKE	VREF

NOTE :

1. RFU1 is reserved for A12
2. RFU2 is reserved for BA2
3. VSS Thermal balls are optional

PIN Description

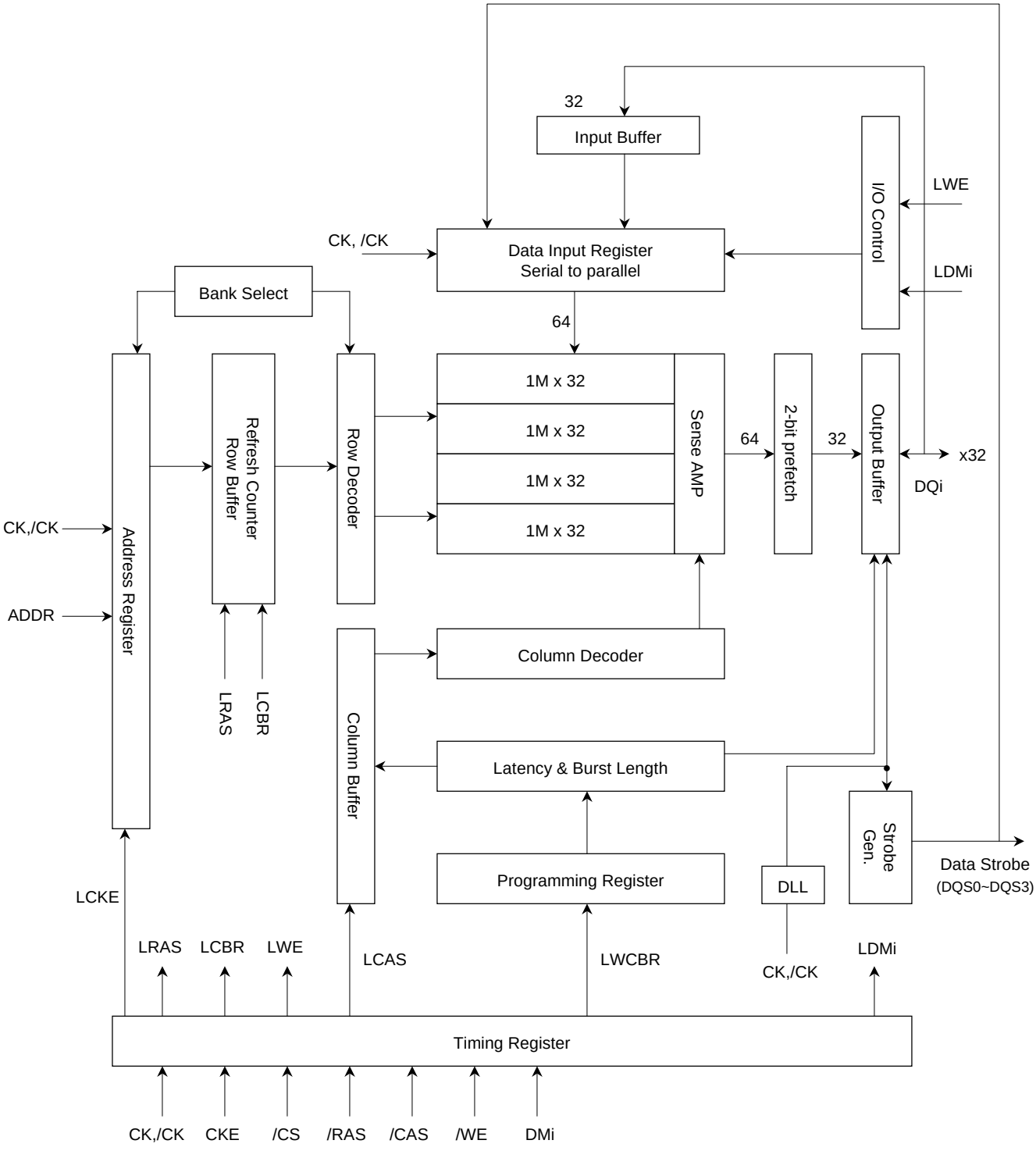
CK, /CK	Differential Clock Input	**BA_0, BA_1**	Bank Select Address
CKE	Clock Enable	**A_0 ~ A_{11}**	Address Input
/CS	Chip Select	**DQ_0 ~ DQ_{31}**	Data Input/Output
/RAS	Row Address Strobe	**V_{DD}**	Power
/CAS	Column Address Strobe	**V_{SS}**	Ground
/WE	Write Enable	**V_{DDQ}**	Power for DQ's
DQS	Data Strobe	**V_{SSQ}**	Ground for DQ's
DM	Data Mask	**MCL**	Must Connect Low
RFU	Reserved for Future Use		

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

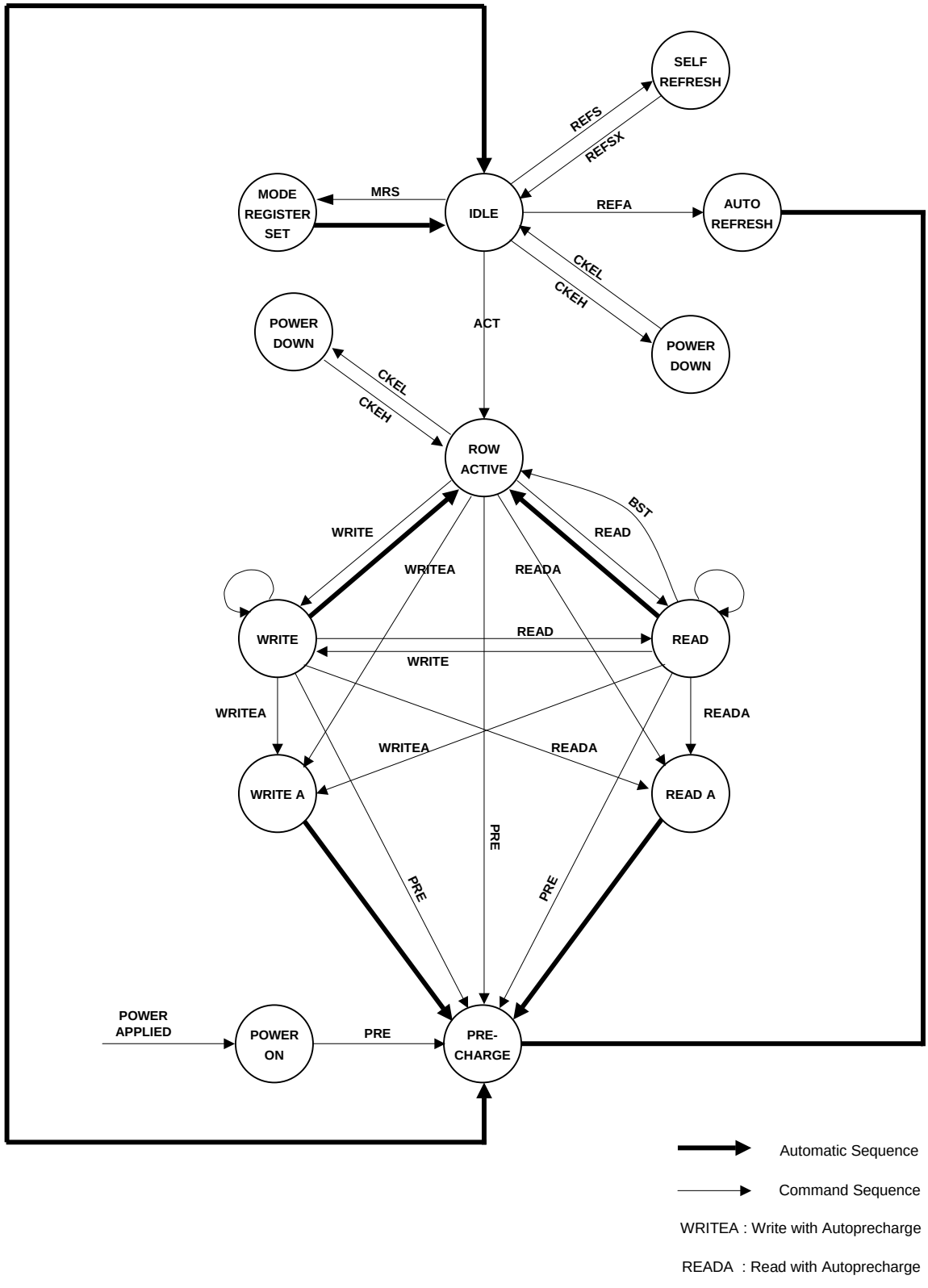
Symbol	Type	Function
CK, /CK#	Input	The differential system clock inputs. All of the input are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	CKE high activates and CKE low deactivates the internal clock,input buffers and output drivers. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
/CS	Input	/CS enables(registered Low) and disables(registered High) the command decoder. When /CS is registered High,new commands are ignored but previous operations are continued.
/RAS	Input	Latches row addresses on the positive going edge of the CK with /RAS low. Enables row access & precharge.
/CAS	Input	Latches Column addresses on the positive going edge of the CK with /CAS low. Enables column access.
/WE	Input	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
DQS_0 ~DQS_3	Input,Output	Data inputs and outputs are synchronized with both edge of DQS. DQS_0 for DQ_0~DQ_7, DQS_1 for DQ_8~DQ_{15}, DQS_2 for DQ_{16}~DQ_{23}, DQS_3 for DQ_{24}~DQ_{31}
DM_0 ~ DM_3	Input	Data-In mask. Data-In is masked by DM Latency=0 when DM is high in burst write. DM_0 for DQ_0 ~ DQ_7, DM_1 for DQ_8 ~ DQ_{15}, DM_2 for DQ_{16} ~ DQ_{23}, DM_3 for DQ_{24} ~ DQ_{31}.
DQ_0 ~ DQ_{31}	Input,Output	Data inputs and outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Select which bank is to be active.
A_0 ~ A_{11}	Input	Row,Column addresses are multiplexed on the same pin. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_7. Column address CA_8 is used for auto precharge.
V_{DD},V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ},V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
NC/RFU	No Connection/ Reserved for future use	This pin is recommended to be left "No Connection" on the device
MCL	Must Connect Low	Must Connect Low

: The timing reference point for the differential clocking is the cross point of CK and /CK.
For any applications using the single ended clocking, apply V_{REF} to /CK pin.

FUNCTIONAL BLOCK DIAGRAM (1Mbit x 32 I/O x 4 Bank)



SIMPLIFIED STATE DIAGRAM



FUNCTIONAL DESCRIPTION

Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VREF & VTT
2. Start clock and maintain stable condition for minimum 200µs
3. The minimum of 200µs after stable power and clock (CK,/CK), apply NOP and CKE to be high.
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL

*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.

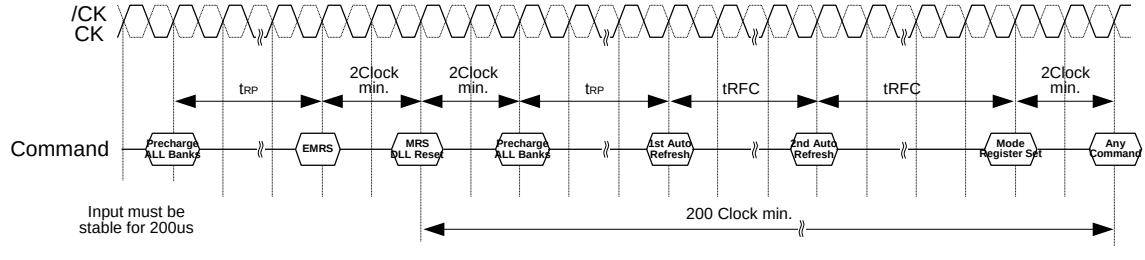
*1,2 7. Issue precharge command for all banks of the device.

8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

***1** Every "DLL Enable" command resets DLL. Therefore sequence 6 can be skipped during power-up. Instead of it, the additional 200cycles of clock input is required to lock the DLL after enabling DLL.

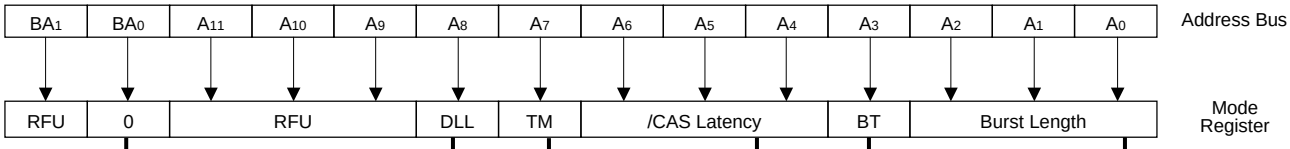
***2** Sequence of 6 & 7 is regardless of the order.

Power-Up & Initialization Sequence



Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs /CAS latency, address mode, burst length, test mode, DLL reset and various vendor specific option to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on /CS, /RAS, /CAS and WE (The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0,BA_1 in the same cycle as /CS, /RAS, /CAS and /WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0~A_2, address mode uses A_3, /CAS latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL for DLL reset. A_7, A_8, BA_0, and BA_1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, address modes and /CAS latencies.



Burst Type

A_3	Type
0	Sequential
1	Interleave

DLL

A_8	DLL Reset
0	No
1	Yes

Test Mode

A_7	Mode
0	Normal
1	Test

BA_0	Mode
0	MRS
1	EMRS

* RFU(Reserved for future use)
should stay "0" during MRS cycle.

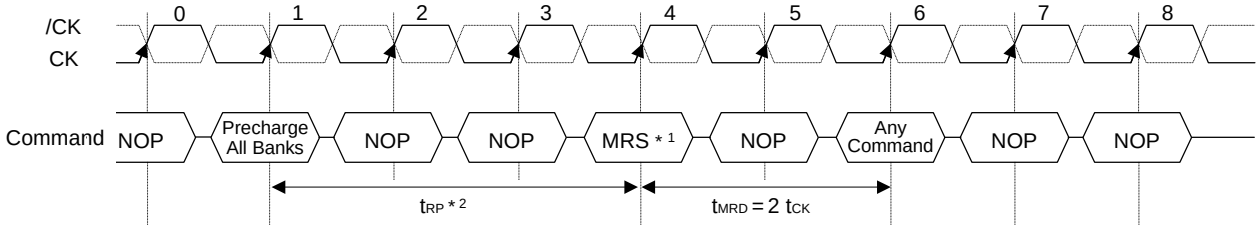
/CAS Latency

A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A_2	A_1	A_0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full page	Reserve

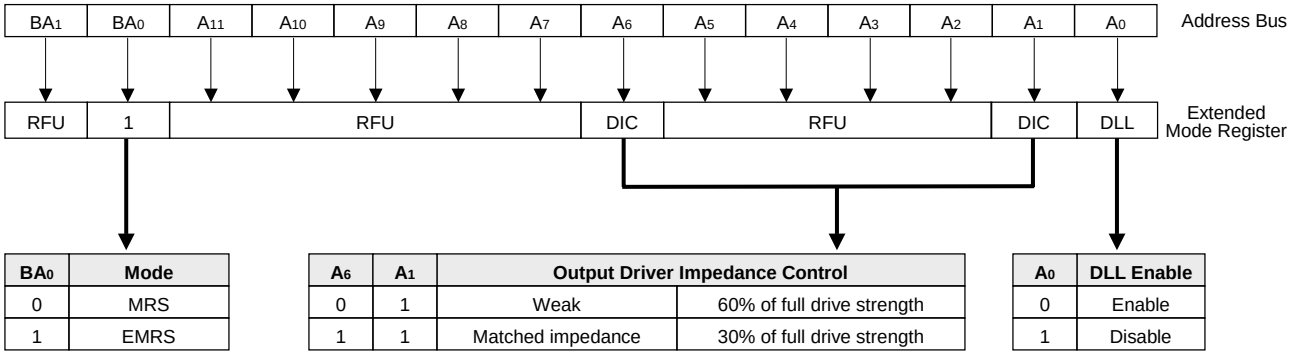
MRS Cycle



* 1 : MRS can be issued only at all banks precharge state.
* 2 : Minimum t_{RP} is required to issue MRS command.

Extended Mode Register Set (EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA_0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A_0,A_2~A_5, A_7~A_{11} and BA1 in the same cycle as /CS,/RAS,/CAS and /WE going low are written in the extended mode register. $A_1$and A_6 are used for setting driver strength to weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state A_0 is used for DLL enable or disable."High"on BA_0 is used for EMRS. All the other address pins except A_0,A_1, A_6 and BA_0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



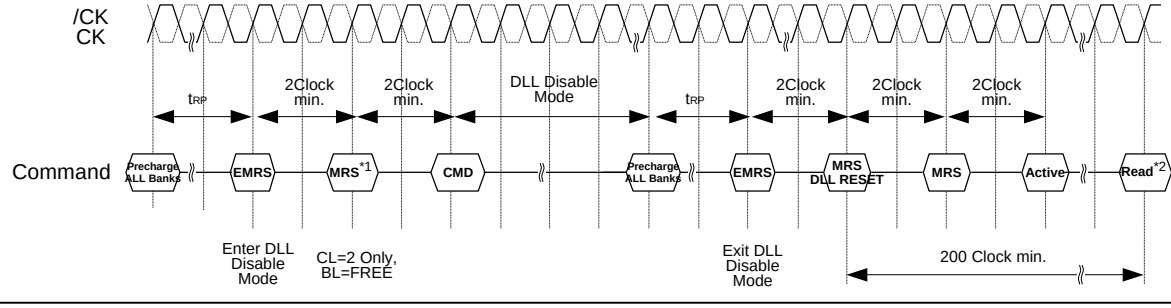
BA_0	Mode
0	MRS
1	EMRS

A_6	A_1	Output Driver Impedance Control	
0	1	Weak	60% of full drive strength
1	1	Matched impedance	30% of full drive strength

A_0	DLL Enable
0	Enable
1	Disable

• RFU(Reserved for Future Use) should stay "0" during MRS cycle.

DLL DISABLE MODE



Notes:
- DLL disable mode is operating mode for low operating frequency between 66MHz and 100MHz without DLL.
- This DLL disable mode is useful for power saving.
- All banks precharge or a bank precharge command can omit before entering and exiting DLL disable mode.

*1 : CL=2 only and BL can set any burst length at DLL disable mode.

*2 : A write command can be applied as far as tRCD is satisfied after any bank active command.
And it needs an additional 200 clock cycles for read operation after exiting DLL disable mode.

Burst Mode Operation

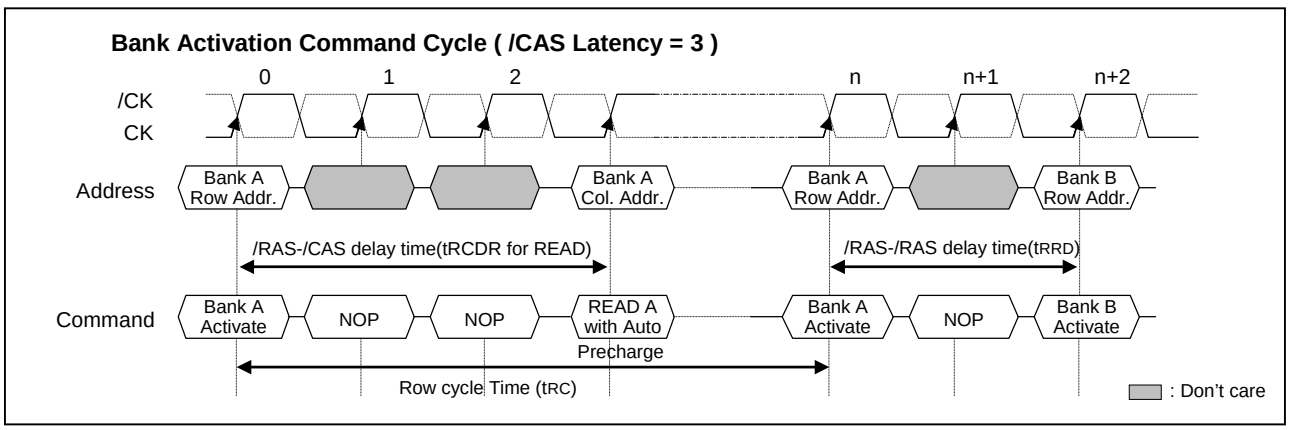
Burst mode operation is used to provide a constant flow of data to memory location (write cycle), or from memory location (read cycle). There are two parameters that define how the burst mode operates. These parameters including burst sequence and burst length are programmable and determined by address A_0 ~ A_3 during the Mode Register Set command. The burst type is used to define the sequence in which the burst data will be delivered or stored to the DDR SDRAM. Two types of burst sequences are supported, sequential and interleaved. See the below table. The burst length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The burst length can be programmed to have values of 2,4,8 or full page. For the full page operation, the starting address must be an even number and the burst stop at the end of burst.

Burst Length and Sequence

Burst Length	Starting Address(A_2,A_1,A_0)	Sequential Mode	Interleave Mode
2	xx0	0-1	0-1
	xx1	1-0	1-0
4	x00	0-1-2-3	0-1-2-3
	x01	1-2-3-0	1-0-3-2
	x10	2-3-0-1	2-3-0-1
	x11	3-0-1-2	3-2-1-0
8	000	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	001	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	010	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	011	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	100	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	101	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	110	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	111	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A_0 - A_7, A_0 = 0	Cn, Cn+1, Cn+2, …, Cn-1	Not supported

Bank Activation Command

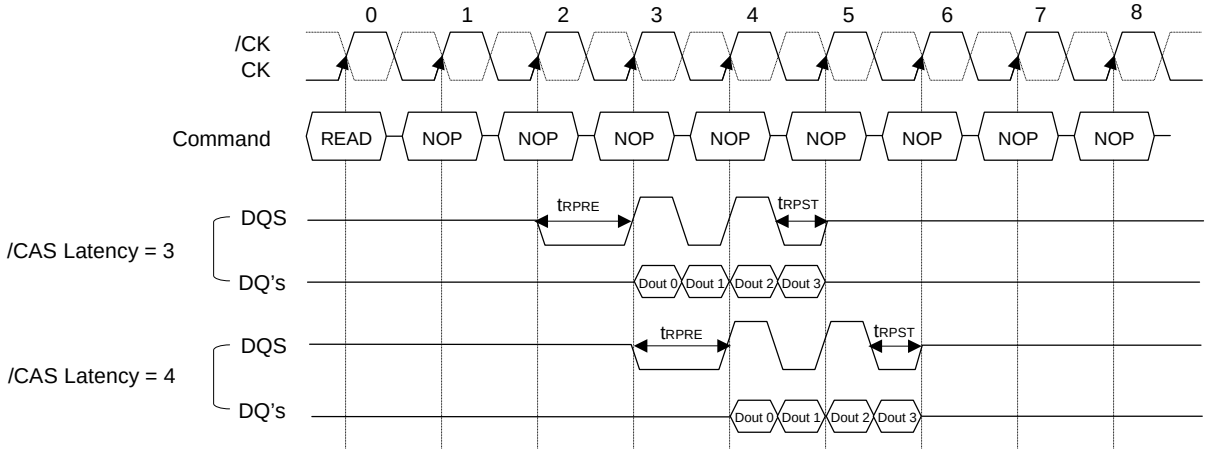
The Bank Activation command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock. The DDR SDRAM has four independent Banks, so two Bank Select Addresses(BA_0, BA_1) are supported. The Bank Activation command must be applied before any Read or Write operation is executed.The delay from the Bank Activation command to the first read or write command must meet or exceed the minimum of /RAS to /CAS delay time(tRCDR/tRCDW min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to B and vice versa) is the Bank to Bank delay time (t_{RRD} min).



Burst Read Operation

Burst Read operation in DDR SDRAM is in the same manner as the current SDRAM such that the burst read command is issued by asserting /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock after t_{RCD} from the bank activation. The address inputs (A_0~A_7) determine the starting address for the Burst. The Mode Register sets type of burst (Sequential or interleave) and burst length(2,4,8, Full page). The first output data is available after the /CAS Latency from the READ command, and the consecutive data are presented on the falling and rising edge of Data Strobe adopted by DDR SDRAM until the burst length is completed.

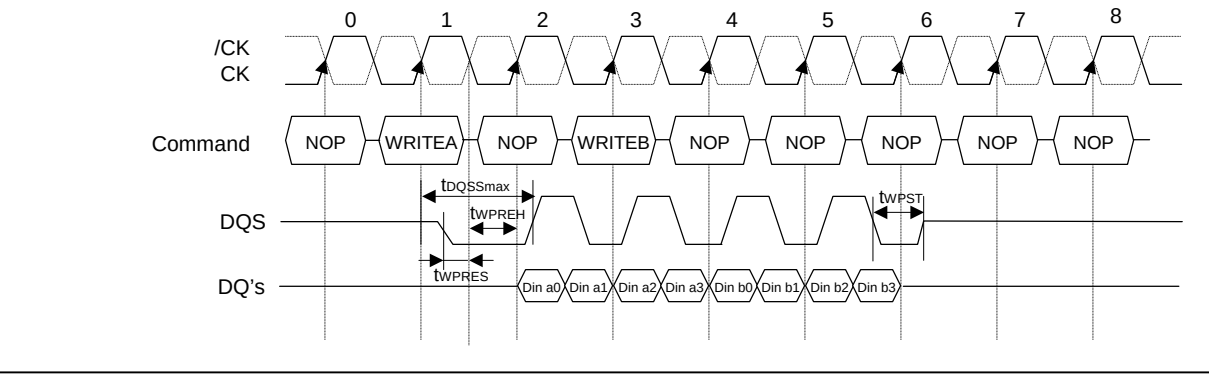
< Burst Length = 4, /CAS Latency = 3,4 >



Burst Write Operation

The Burst Write command is issued by having /CS, /CAS and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. There is no real write latency required for burst write cycle. The first data for burst write cycle must be applied at the first rising edge of the data strobe enabled after t_{DQSS} from the rising edge of the clock that the write command is issued.The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. When the burst has been finished, any additional data supplied to the DQ pins will be ignored.

< Burst Length = 4 >

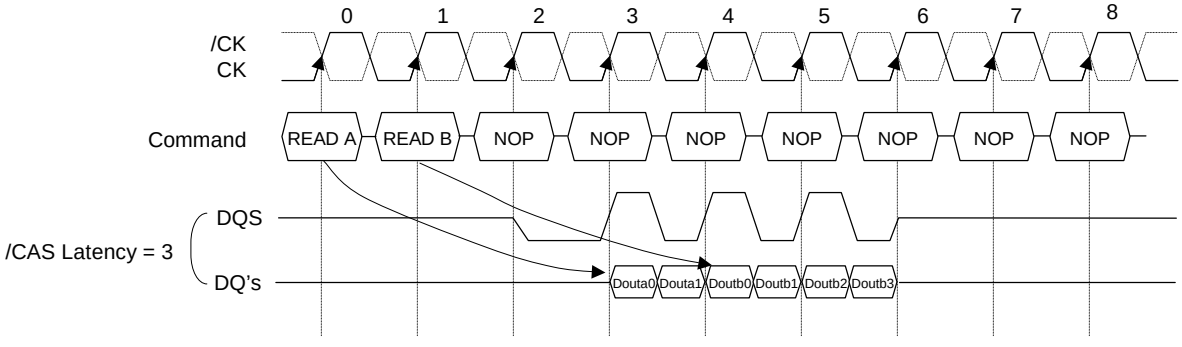


Burst Interruption

Read Interrupted by Read

Burst Read can be interrupted before completion of the burst by new Read command of any bank. When the previous burst is interrupted, the remaining address are overridden by the new address with the full burst length. The data from the previous Read command continues to appear on the outputs until the /CAS latency from the interrupting Read command is satisfied. Read to Read interval is minimum 1 tCK.

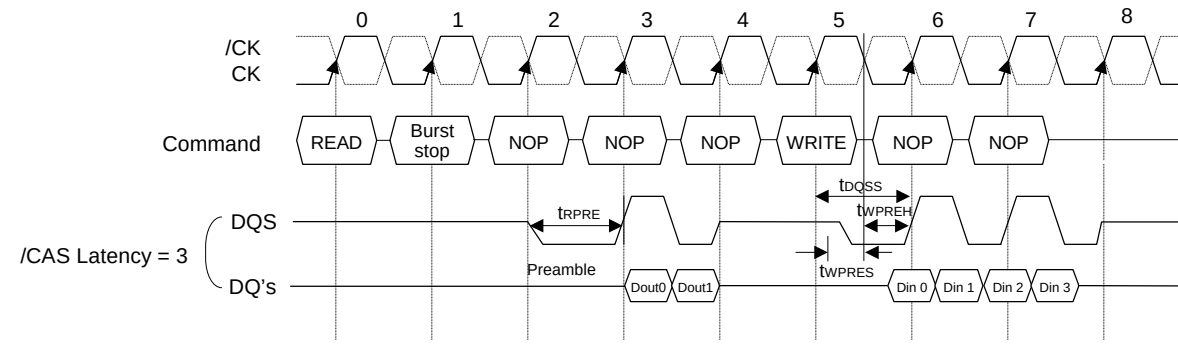
< Burst Length = 4, /CAS Latency = 3 >



Read Interrupted by Burst stop & Write

To interrupt Burst Read with a write command, Burst stop command must be asserted to avoid data contention on the I/O bus by placing the DQ's(Output drivers) in a high impedance state at least one clock cycle before the Write Command is initiated.
Once the burst stop command has been issued, the minimum delay to a write command is CL(RU). [CL is /CAS Latency and RU means round up to the nearest integer.]

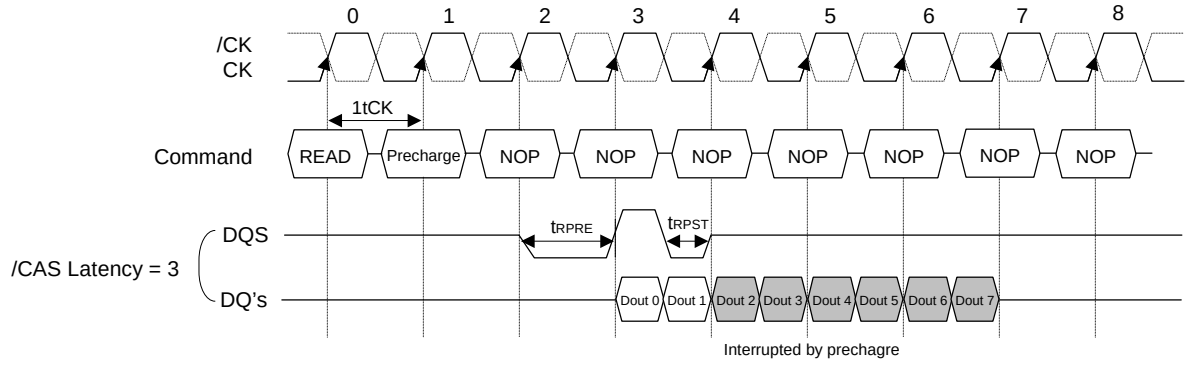
< Burst Length = 4, /CAS Latency = 3 >



Read Interrupted by Precharge

Burst Read can be interrupted by precharge of the same bank. The minimum 1 clock cycle is required for the read precharge interval. Precharge command to output disable latency is equivalent to the /CAS latency.

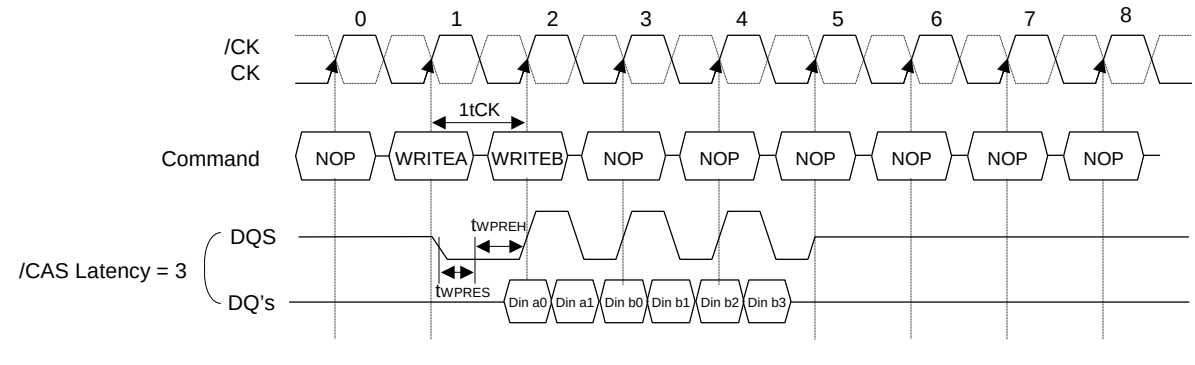
< Burst Length = 8, /CAS Latency = 3 >



Write Interrupted by Write

Burst Write can be interrupted by the new Write Command before completion of the previous burst write, with the onlyrestriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new addresses and data will be written into the device until the programmed burst length is satisfied.

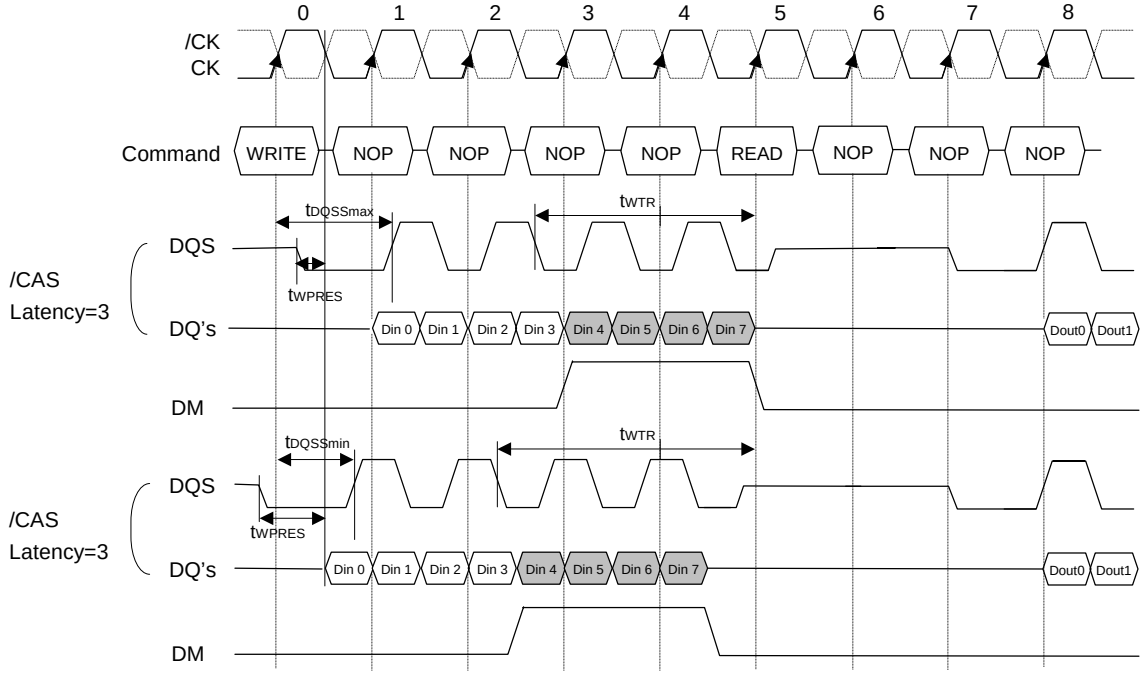
< Burst Length = 4 >



Write Interrupted by Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (tWTR) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of the write command.

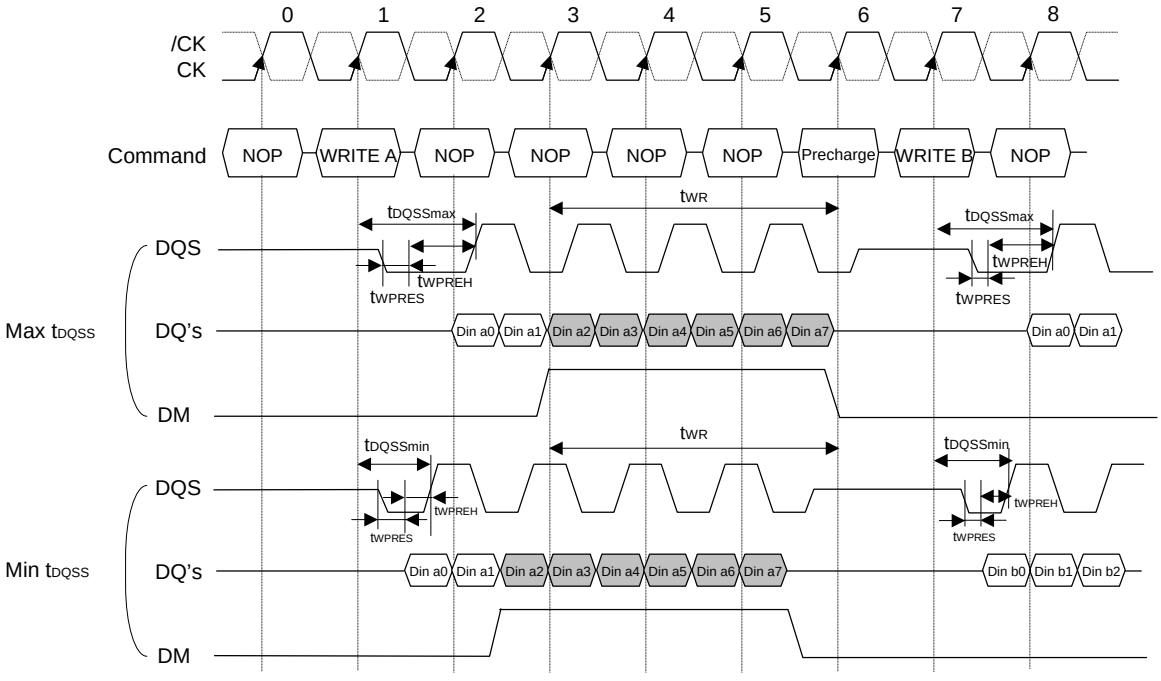
< Burst Length = 8 >



Write Interrupted by Precharge & DM

A burst Write can be interrupted by a precharge of the same bank before completion of the previous burst. A write recovery time(t_{WR}) is required from the last data to precharge command. When Precharge command is asserted, any residual data from the burst write cycle must be masked by DM.

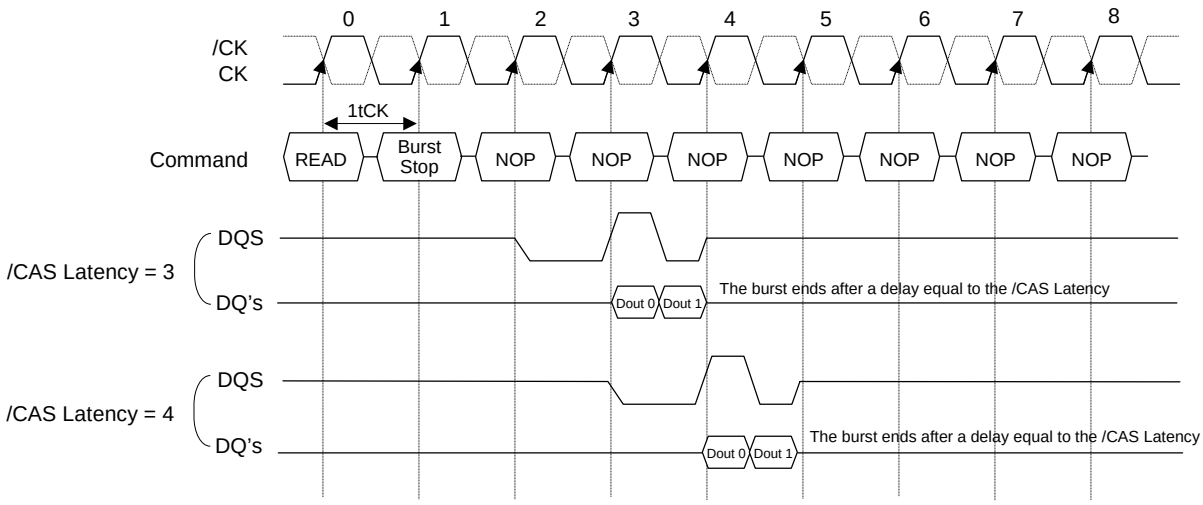
< Burst Length = 8 >



BURST STOP COMMAND

The Burst stop command is initiated by having /RAS and /CAS high with /CS and /WE low at the rising edge of the clock only. The Burst Stop command has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a burst read cycle, both the data and DQS(Data Strobe) go to a high impedance state after a delay which is equal to the /CAS Latency set in the Mode Register. The Burst Stop command, however, is not supported during a write burst operation.

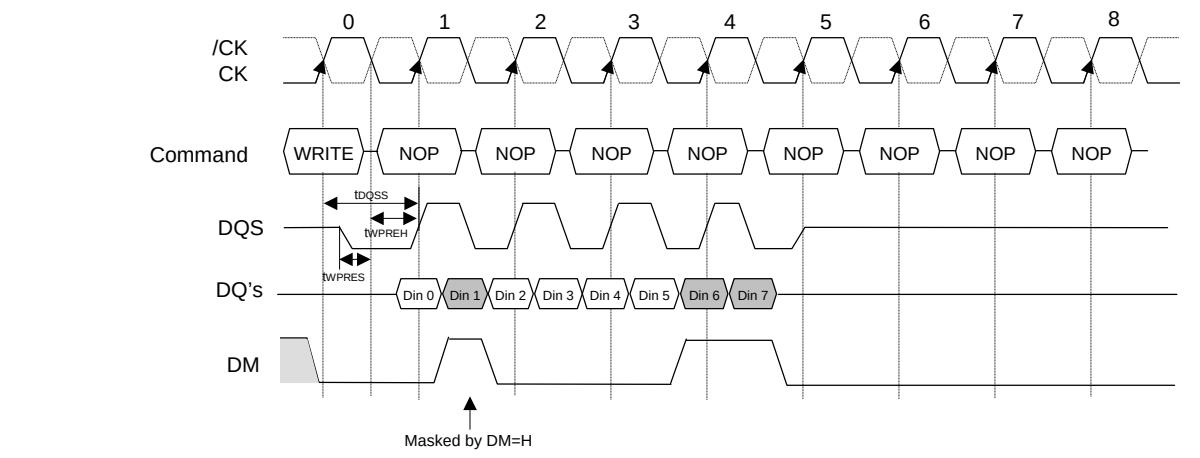
< Burst Length = 4, /CAS Latency = 3,4 >



DM FUNCTION

The DDR SDRAM has a Data mask function that can be used in conjunction with data Write cycle only, not Read cycle. When the Data Mask is activated (DM high) during write operation, the write data is masked immediately (DM to Data-mask Latency is Zero). DM must be issued at the rising edge or the falling edge of Data Strobe instead of a clock edge.

< Burst Length = 8 >

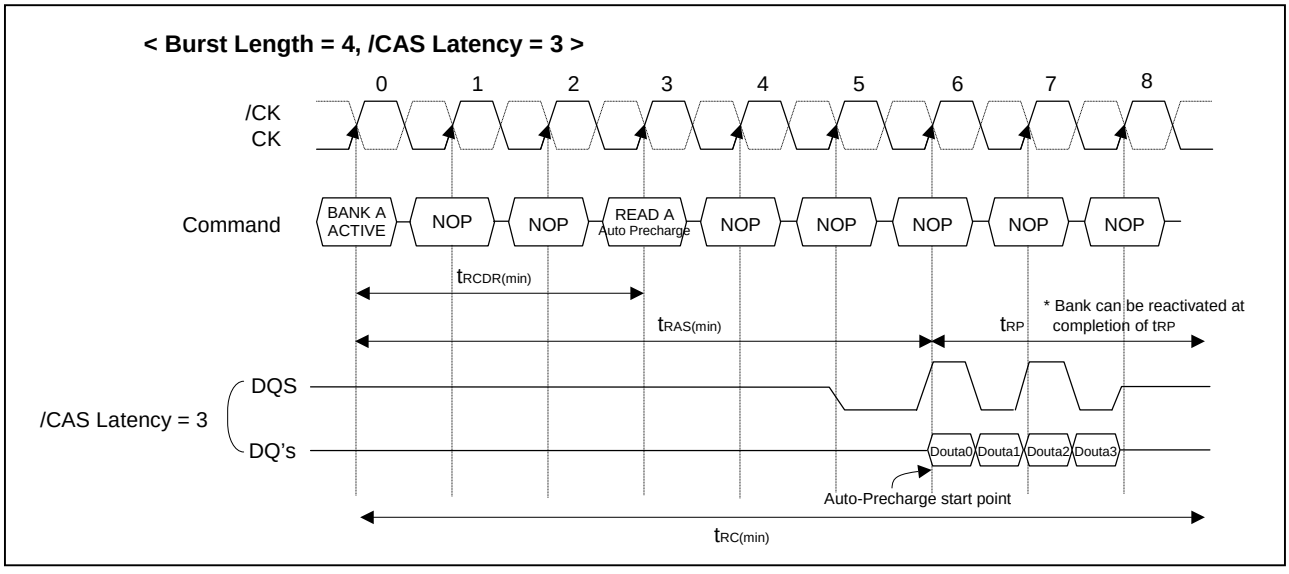


AUTO-PRECHARGE OPERATION

The Auto precharge command can be issued by having column address A_8 High when a Read or a Write command is asserted into the DDR SDRAM. If A_8 is low when Read or Write command is issued, normal Read or Write burst operation is asserted and the bank remains active after the completion of the burst sequence. When the Auto precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during read or write cycle after $t_{RAS(min)}$ is satisfied.

Read with Auto Precharge

If a Read with Auto-precharge command is initiated, the DDR SDRAM automatically starts the precharge operation on 2 clock previous to the end of burst from a Read with Auto-Precharge command when $t_{RAS(min)}$ is satisfied. If not, the start point of precharge operation will be delayed until $t_{RAS(min)}$ is satisfied. The bank started the Precharge operation once cannot be reactivated and the new command can not be asserted until the Precharge time(t_{RP}) is satisfied.



When the Read with Auto precharge command is issued, new command can be asserted at T5,T6 and T7 respectively as follows.

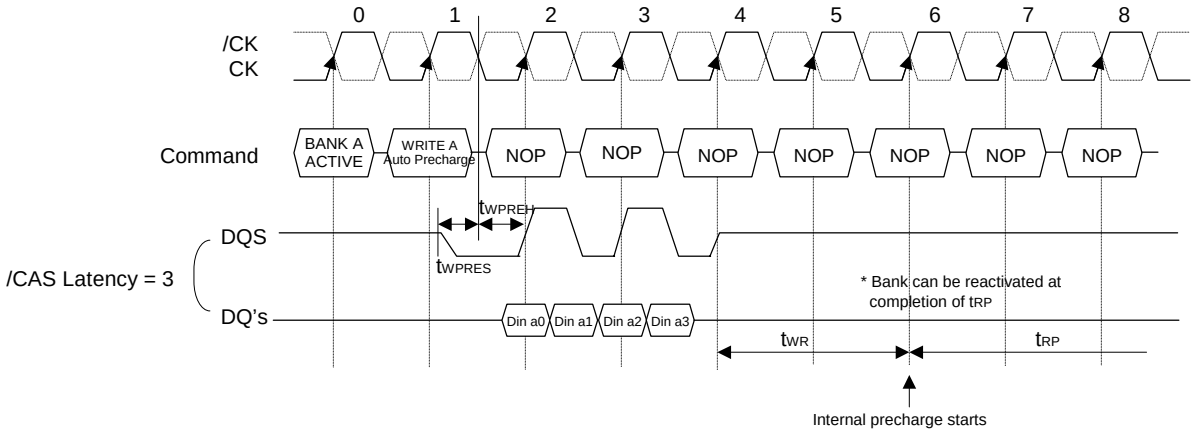
Asserted command	For same Bank			For Different Bank		
	5	6	7	5	6	7
READ	READ + No AP*1	READ + No AP	Illegal	Legal	Legal	Legal
READ+AP	READ + AP	READ + AP	Illegal	Legal	Legal	Legal
Active	Illegal	Illegal	Illegal	Legal	Legal	Legal
Precharge	Legal	Legal	Illegal	Legal	Legal	Legal

*1 : AP = Auto Precharge

Write with Auto Precharge

If A_8 is high when Write command is issued, the write with Auto-Precharge function is performed. Any new command to the same bank should not be issued until the internal precharge is completed. The internal precharge begins after keeping $t_{WR(min)}$.

< Burst Length = 4, /CAS Latency = 3 >



Asserted command	For same Bank						For Different Bank				
	2	3	4	5	6	7	2	3	4	5	6
WRITE	WRITE + No AP *1	WRITE + No AP	WRITE + No AP	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
WRITE + AP	WRITE + AP	WRITE + AP	WRITE+AP	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
READ	Illegal	READ + No AP + DM *2	READ + No AP + DM	READ + No AP	READ + No AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal
READ + AP	Illegal	READ + AP + DM	READ + AP + DM	READ + AP	READ + AP	Illegal	Illegal	Illegal	Illegal	Legal	Legal
Active	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal
Precharge	Illegal	Illegal	Illegal	Illegal	Illegal	Illegal	Legal	Legal	Legal	Legal	Legal

*1 AP = Auto Precharge
*2 DM : Refer to "Write Interrupted by Rean & DM" in page 16.

PRECHARGE COMMAND

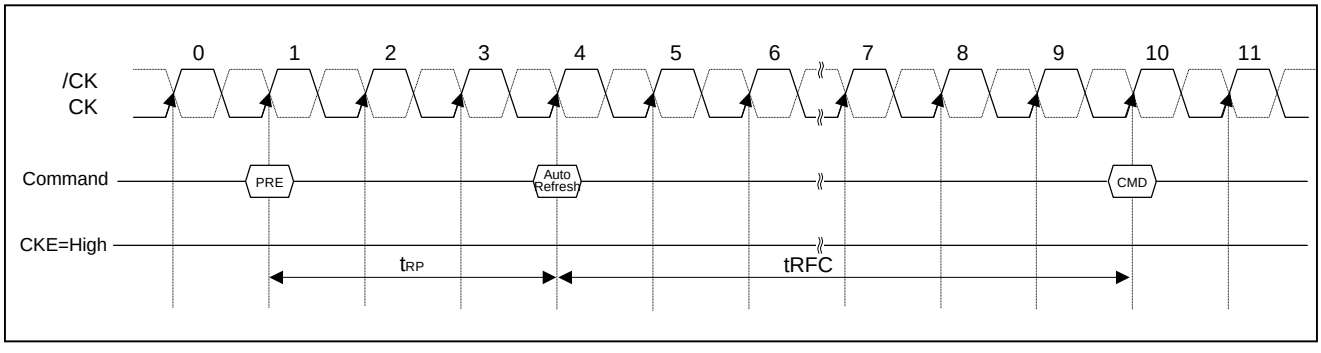
The precharge command is issued when /CS, /RAS, and /WE are low and /CAS is high at the rising edge of the clock, CK. The precharge command can be used to precharge each bank respectively or all banks simultaneously. The Bank select addresses(BA_0, BA_1) are used to define which bank is precharged when the command is initiated. For write cycle, tWR(min.) must be satisfied from the start of the last burst write cycle until the precharge command can be issued. After t_{RP} from the precharge, an active command to the same bank can be initiated.

< Bank Selection for Precharge by Bank address bits >

A8/AP	BA1	BA0	Precharge
0	0	0	Bank A Only
0	0	1	Bank B Only
0	1	0	Bank C Only
0	1	1	Bank D Only
1	X	X	All Banks

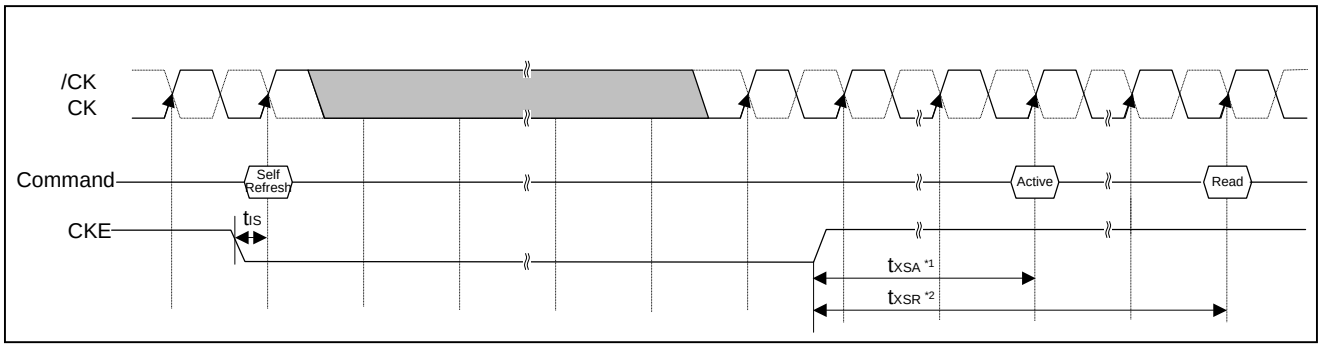
AUTO REFRESH

An Auto Refresh command is issued by having /CS, /RAS and /CAS held low with CKE and /WE high at the rising edge of the clock, CK. All banks must be precharged and idle for a $t_{RP(min)}$ before the Auto Refresh command is applied. The refresh addressing is generated by the internal refresh address counter. This makes the address bits “Don’t care” during an Auto Refresh command. When the refresh cycle has completed, all banks will be in the idle state. A delay between the Auto Refresh command and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the $tRFC_{(min)}$.



SELF REFRESH

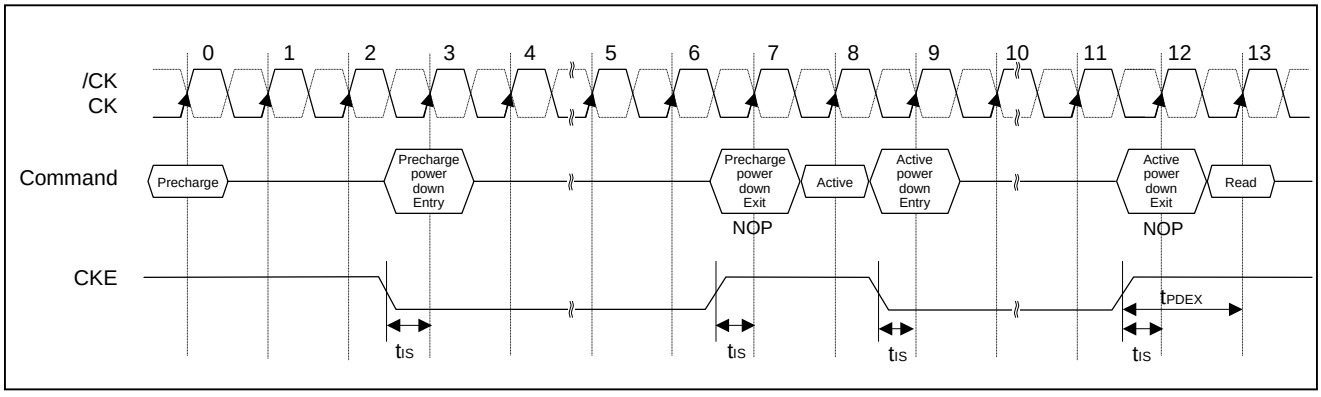
A self refresh command is defined by having /CS, /RAS, /CAS and CKE low with /WE high at the rising edge of the clock (CK). Once the self refresh command is initiated, CKE must be held low to keep the device in self refresh mode. During the self refresh operation, all inputs except CKE are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning CKE high, asserting deselect or NOP command and then asserting CKE high for longer than tXSR for locking of DLL.



*1 Exit self refresh to bank active command, a write command can be applied as far as tRCD is satisfied after any bank active command.
*2 Exit self refresh to read command.

POWER DOWN MODE

The power down is entered when CKE Low, and exited when CKE High. Once the power down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. The all banks should be in idle state prior to entering the precharge power down mode and CKE should be set high at least 1tCK+tIS prior to Row active command. During power down mode, refresh operations can't be performed, therefore the device cannot remain in power down mode longer than the refresh period(t_{REF}) of the device.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage Temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	2.0	W
Short circuit current	I_{OS}	50	mA

Note :

Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device supply Voltage	V_{DD}	2.375	2.50	2.625	V	1
Output supply Voltage	V_{DDQ}	2.375	2.50	2.625	V	1
Reference Voltage	V_{REF}	0.49* V_{DDQ}	-	0.51* V_{DDQ}	V	2
Termination Voltage	Vtt	V_{REF} -0.04	VREF	V_{REF} +0.04	V	3
Input logic high Voltage	V_{IH}	V_{REF} +0.15	-	V_{DDQ} +0.30	V	4
Input logic low Voltage	V_{IL}	-0.30	-	V_{REF} -0.15	V	5
Output logic high Voltage	V_{OH}	Vtt+0.76	-	-	V	I_{OH} = -15.2mA
Output logic low Voltage	V_{OL}	-	-	Vtt-0.76	V	I_{OL} = +15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	6

Note :

1. For -25/–28/-33/-36/-40/-45/-50, V_{DD} / V_{DDQ} = 2.5V ±5% / 2.5V ±5%
2. V_{REF} is expected to equal 0.50* V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed ±2% of the DC value. Thus, from 0.50* V_{DDQ}, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise.
3. Vtt of the transmitting device must track V_{REF} of the receiving device.
4. V_{IH}(max.) = V_{DDQ} +1.5V for a pulse and it which can not be greater than 1/3 of the cycle rate.
5. V_{IL}(mim.) =-1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
6. For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN} = 0V.

DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss=0V, V_{DD}/V_{DDQ}=2.5V±5%/ 2.5V±5%,, TA=0 to 70°C)

Parameter	Symbol	Test Condition	Version									Unit	Note
			-25	-28	-33	-36	-40	-45	-50	-55	-60		
Operating current (One Bank Active)	Icc1	Burst Length=2, tRC ≥ tRC(min) IOL=0mA, tCK=tCK(min)	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	1
Precharge Standby Current in Power-down mode	Icc2P	CKE ≤ VIL(max), tCK=tCK(min)	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	
Precharge Standby Current in Non Power-down mode	Icc2N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK=tCK(min).	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	
Active Standby Current in Power-down mode	Icc3P	CKE ≤ VIL(max), tCK=tCK(min)	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	
Active Standby Current in Non Power-down mode	Icc3N	CKE ≥ VIH(min), /CS ≥ VIH(min), tCK=tCK(min).	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	
Operating Current (Burst mode)	Icc4	IOL=0mA, tCK=tCK(min), Page Burst, All Banks activated.	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	
Refresh current	Icc5	tRC ≥ tRFC(min)	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	2
Self Refresh current	Icc6	CKE ≤ 0.2V	*TBD*									mA	
Operating Current (4Bank Interleaving)	Icc7	Burst Length=4, tRC ≥ tRC(min) IOL=0mA, tCK=tCK(min)	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	*TBD*	mA	

Notes :

1. Measured with outputs open.
2. Refresh period is 32ms.

AC INPUT OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to Vss=0V, V_{DD}/V_{DDQ}=2.5V±5%/ 2.5V±5%,, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic1) Voltage : DQ	VIH	V_{REF}+0.35	-	-	V	
Input Low (Logic0) Voltage : DQ	VIL	-	-	V_{REF} -0.35	V	
Clock input Differential Voltage ; CK and /CK	VID	0.7	-	V_{DDQ}+0.6	V	1
Clock input Crossing point Voltage ; CK and /CK	VIX	0.5* V_{DDQ} -0.2	-	0.5* V_{DDQ} +0.2	V	2

Note :

1. VID is the magnitude of the difference between the input level on CK and the input level on /CK
2. The value of VIX is expected to equal 0.5* V_{DDQ} of the transmitting device and must track variation in the DC level of the same

AC OPERATING TEST CONDITIONS

(V_{DD}=2.5V±0.125V, TA=0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for CK (for signal ended)	0.50* V_{DDQ}	V	
CK and /CK signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input levels (VIH/VIL)	V_{REF}+0.35 / V_{REF}-0.35	V	
Input timing measurement refrence level	V_{REF}	V	
Output timing measurement refrence level	Vtt	V	
Output load condition	See Fig.1		

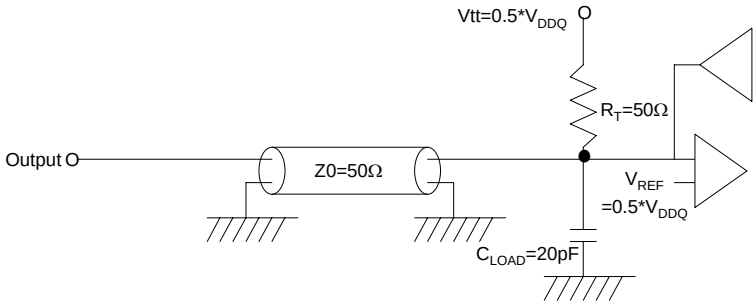


Fig.1) Output Load Circuit

CAPACITANCE (V_{DD}=2.5V, TA=25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, /CK,)	CIN1	2.0	3.0	pF
Input capacitance (A0~A11, BA0~BA1)	CIN2	2.0	3.0	pF
Input capacitance (CKE, /CS, /RAS, /CAS, /WE)	CIN3	2.0	3.0	pF
Data & DQS input/output capacitance (DQ0~DQ31)	COUT	4.0	5.0	pF
Input capacitance (DM0 ~ DM3)	CIN4	4.0	5.0	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between VDD and VSS	CDC1	0.1+0.01	uF
Decoupling Capacitance between VDDQ and VSSQ	CDC2	0.1+0.01	uF

Note :

1. VDD and VDDQ pins are separated each other.
   All VDD pins are connected in chip. All VDDQ pins are connected in chip.
2. VSS and VSSQ pins are separated each other.
   All VSS pins are connected in chip. All VSSQ pins are connected in chip.

AC CHARACTERISTICS(I)

Parameter		Symbol	-25		-28		-33		-36		-40		-45		-50		-55		-60		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK cycle time	CL=4	t_{CK}	2.5	3.6	2.8	3.6	3.3	3.6	3.6	4	-	-	-	-	-	-	-	-	-	-	ns	
	CL=3		-	-	-	-	3.3	5	3.6	5	4.0	5	4.5	5	5.0	5.5	-	-	-	-	ns	
	CL=2		-	-	-	-	-	-	-	-	4.0	10	4.5	10	5.0	10	5.5	10	6.0	10	ns	
CK high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		t_{DQSCK}	-0.6	+0.6	-0.6	+0.6	-0.6	+0.6	-0.6	+0.6	-0.6	+0.6	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Output access time from CK		t_{AC}	-0.6	+0.6	-0.6	+0.6	-0.7	+0.7	-0.7	+0.7	-0.6	+0.6	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to Dout edge		t_{DQSQ}	-	+0.35	-	+0.35	-	+0.35	-	+0.40	-	+0.40	-	+0.45	-	+0.45	-	+0.5	-	+0.5	ns	1
Read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		t_{DQSS}	0.85	1.15	0.85	1.15	0.85	1.15	0.85	1.15	0.85	1.15	0.8	1..2	0.8	1..2	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		t_{WPRES}	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	0	-	ns	
DQS-in hold time		t_{WPREH}	0.35	-	0.35	-	0.35	-	035	-	0.35	-	0.30	-	0.30	-	0.25	-	0.25	-	tCK	
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in high level width		t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width		t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Address and Control input setup		t_{IS}	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	1.1	-	1.1	-	ns	
Address and Control input hold		t_{IH}	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	1.0	-	1.0	-	1.1	-	1.1	-	ns	
DQ and DM setup time to DQS		t_{DS}	0.35	-	0.35	-	0.35	-	0.40	-	0.40	-	0.45	-	0.45	-	0.5	-	0.5	-	ns	
DQ and DM hold time to DQS		t_{DH}	0.35	-	0.35	-	0.35	-	0.40	-	0.40	-	0.45	-	0.45	-	0.5	-	0.5	-	ns	
Clock half period		t_{HP}	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Data output hold time from DQS		t_{QH}	tHP -0.35	-	tHP -0.35	-	tHP -0.35	-	tHP -0.40	-	tHP -0.40	-	tHP -0.45	-	tHP -0.45	-	tHP -0.5	-	tHP -0.5	-	ns	1

Note 1:

-. The JEDEC DDR specification currently defines the output data valid window(tDV) as the period when the data strobe and all data associated with that data strobe are coincidentally valid.

-. The previously used definition of tDV(=0.35tDK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%

-. A new AC timing term,tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces

tDV - tQHmin = tHP-X

where . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)

. X=A frequency dependent timing allowance account for tDQSQmax

AC CHARACTERISTICS(II)

Parameter	Symbol	-25		-28		-33		-36		-40		-45		-50		-55		-60		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	23	-	20	-	17	-	16	-	15	-	13	-	12	-	12	-	10	-	tCK	
Refresh cycle time	tRFC	25	-	22	-	19	-	18	-	17	-	15	-	14	-	14	-	12	-	tCK	
Row active time	tRAS	16	100K	14	100K	12	100K	11	100K	10	100K	9	100K	8	100K	8	100K	7	100K	tCK	
/RAS to /CAS delay for Read	tRCDR	8	-	7	-	6	-	5	-	5	-	4	-	4	-	4	-	3	-	tCK	
/RAS to /CAS delay for Write	tRCDW	6	-	5	-	4	-	3	-	3	-	2	-	2	-	2	-	2	-	tCK	
Row precharge time	tRP	7	-	6	-	5	-	5	-	5	-	4	-	4	-	4	-	3	-	tCK	
Row active to Row active	tRRD	4	-	4	-	3	-	3	-	3	-	2	-	2	-	2	-	2	-	tCK	
Last data in to Row precharge(@Normal)	tWR	3	-	3	-	3	-	3	-	3	-	3	-	2	-	2	-	2	-	tCK	1
Last data in to Row precharge(@Auto)	tWR_A	3	-	3	-	3	-	3	-	3	-	3	-	3	-	3	-	3	-	tCK	1
Internal Write in to Read command	tWTR	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	tDAL	9	-	8	-	7	-	7	-	7	-	6	-	6	-	6	-	5	-	tCK	
Exit self refresh to active command	tXSA	75	-	75	-	75	-	75	-	75	-	75	-	75	-	75	-	75	-	ns	2
Exit self refresh to read command	tXSR	200	-	200	-	200	-	200	-	200	-	200	-	200	-	200	-	200	-	tCK	
Power down exit time	tPDEX	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	ns	
Refresh interval time	tREF	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	us	

Note

1. For normal write operation, even numbers of Din are to be written inside DRAM
2. A write command can be applied with tRCD satisfied after this command.

-. AC parameters for DLL Disable Mode(66MHz ~ 100MHz, CL2 only) : Same as “-60” AC parameters except tCK.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DM	$BA_{0,1}$	A_8 /AP	A_{11}~A_9, A_7~A_0	Note
Register	Extended Mode Register		H	X	L	L	L	L	X	OP CODE			1,2
	Mode Register Set		H	X	L	L	L	L	X	OP CODE			
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Address			H	X	L	L	H	H	X	V	Row Address		
Read & Column Addr.	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address	4
	Auto Precharge Enable										H		4
Write & Column Addr.	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address	4
	Auto Precharge Enable										H		4,6
Burst Stop			H	X	L	H	H	L	X	X			7
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	H	H	H					
DM			H	X					V	X			8
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't care, H=Logic High, L=Logic Low)

Note : 1. OP CODE : Operand Code.
A_0 ~ A_{11} & BA_0 ~ BA_1 : Program Keys. (@EMRS/MRS)

2. EMRS/MRS can be issued only at all banks precharge state
A new command can be issued after 2 clock cycle of EMRS/MRS

3. Auto refresh function are as same as CBR refresh of DRAM.
The automatic precharge without row precharge command is meant by "Auto".
Auto/Self refresh can be issued only at all banks precharge state.

4. BA_0 ~ BA_1 : Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A_8/AP is "high" at row precharge ,BA_0 and BA_1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command cannot be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges(Write DM latency is 0).

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA_0, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A_8	PRE/PREA	NOP*4
	L	L	L	H	X	REFA	AUTO-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA, CA, A_8	READ/READA	Begin Read, Latcch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	Terminate Burst
	L	H	L	H	BA, CA, A_8	READ/READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	H	BA, CA, A_8	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A_8	WRITE/WRITEA	Terminate Burst, Latch CA, Begin new Write, Determine Precharge*3
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	Terminate Burst with DM=high precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TERM	ILLEGAL
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
PRECHARGING	H	X	X	X	X	DESEL	NOP(Idle after tRP)
	L	H	H	H	X	NOP	NOP(Idle after tRP)
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP(ROW Active after tRCD)
	L	H	H	H	X	NOP	NOP(ROW Active after tRCD)
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A_8	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A_8	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TERM	NOP
	L	H	L	H	BA, CA, A8	READ	ILLEGAL*2
	L	H	L	L	BA, CA, A8	WRITE/WRITEA	New Write, Determine AP.
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	L	H	BA, A8	PRE/PREA	ILLEGAL*2
	L	L	L	L	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	H	X	X	X	X	DESEL	NOP(Idle after tRP)
	L	H	H	H	X	NOP	NOP(Idle after tRP)
	L	H	H	L	X	TERM	NOP
	L	H	L	X	BA, CA, A8	READ/WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A8	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS :

H=High Level, L=Low Level, V=Valid, X=Don't care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

Note :

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state ; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state, May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.
6. Same bank's previous Auto precharge will not be performed. But if Bank is different, previous Auto precharge will be performed.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF-REFRESHING	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh*1
	L	H	L	H	H	H	X	Exit Self-Refresh*1
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
Both Bank Precharge POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down*2
	L	H	L	H	H	H	X	Exit Power Down*2
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Power Down)
ALL BANKS IDLE	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	H	X	X	X	X	Enter Power Down*3
	H	L	L	H	H	H	X	Enter Power Down*3
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	H	RA	Row(& Bank) Active
	H	L	L	L	L	H	X	Enter Self-Refresh *3
	H	L	L	L	L	L	OP Code	Mode Register Access
	L	X	X	X	X	X	X	Refer to Current State=Power Down
Any State other than listed above	H	H	X	X	X	X	X	Refer to Function True Table
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle *4
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle *4
	L	L	X	X	X	X	X	Maintain Clock Suspend

ABBREVIATIONS :

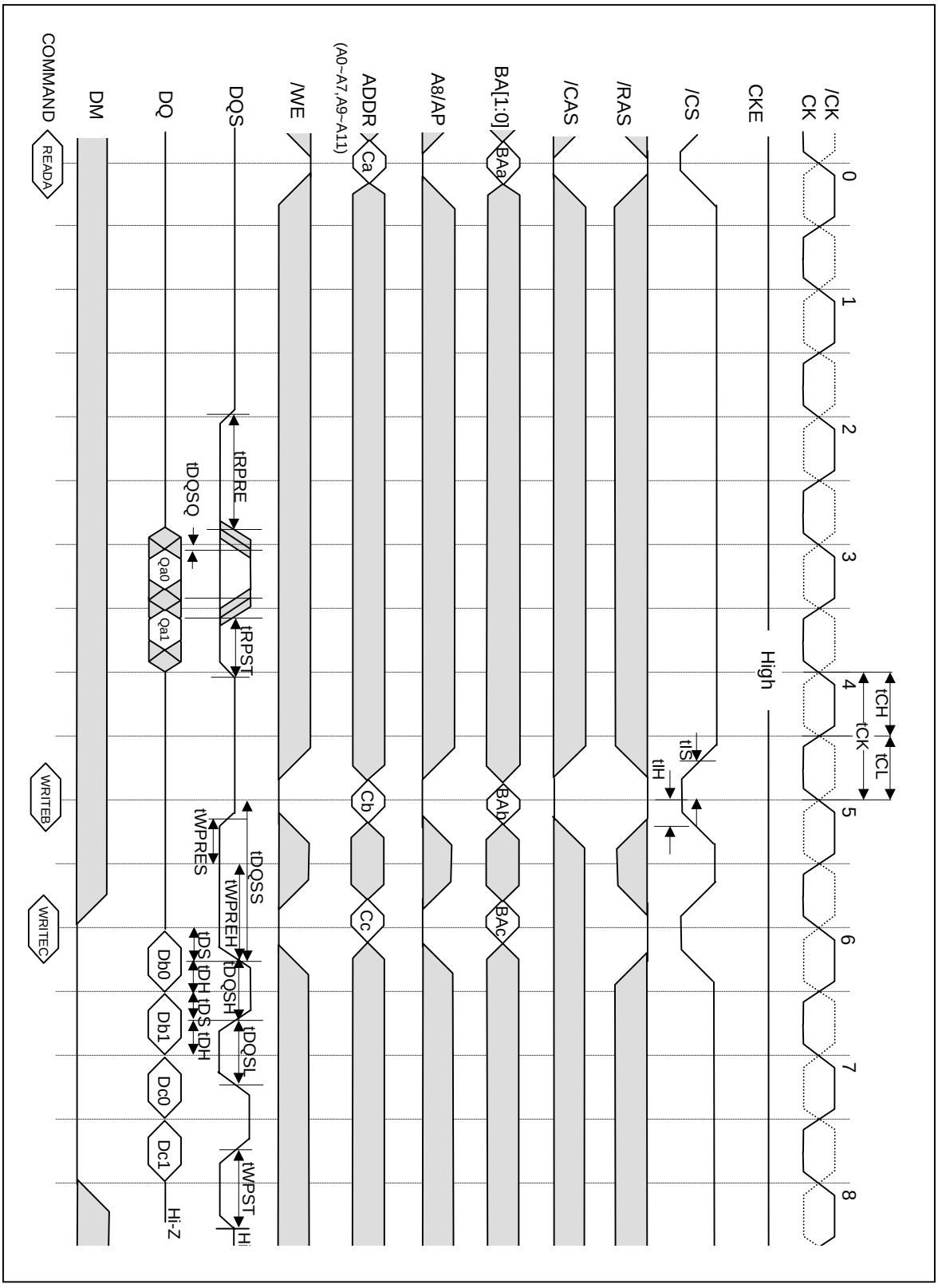
H=High Level, L=Low Level, V=Valid, X=Don't care

Note :

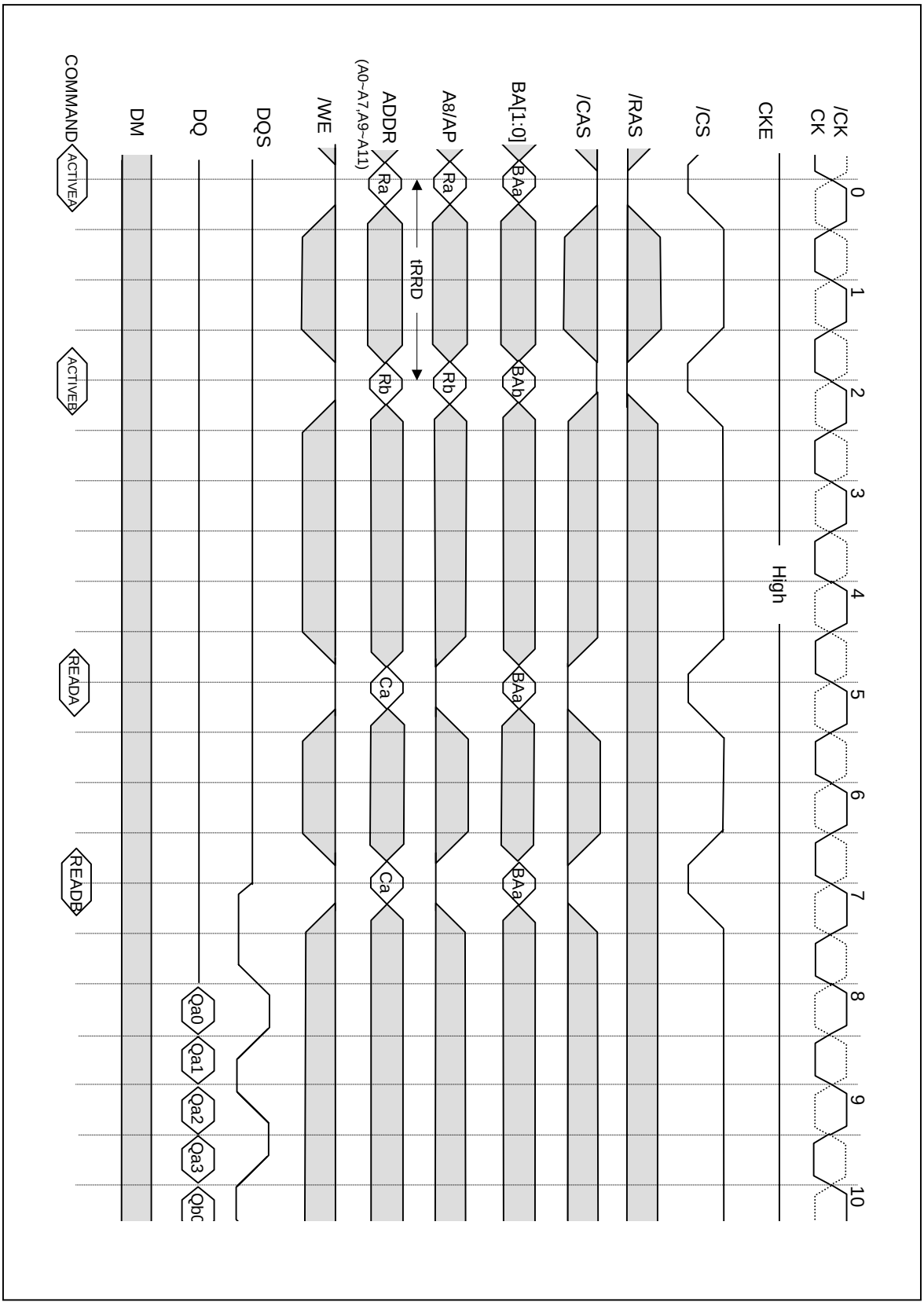
1. After CKE's low to high transition to exist self refresh mode. And a time of tRC(min) has to be elapse after CKE's low to high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restarts internal clock.
   A minimum setup time "tIS + one clock" must be satisfied before any command other than exit.
3. Power-down and self-refresh can be entered only from the all banks idle state.
4. Must be a legal command.

Timing

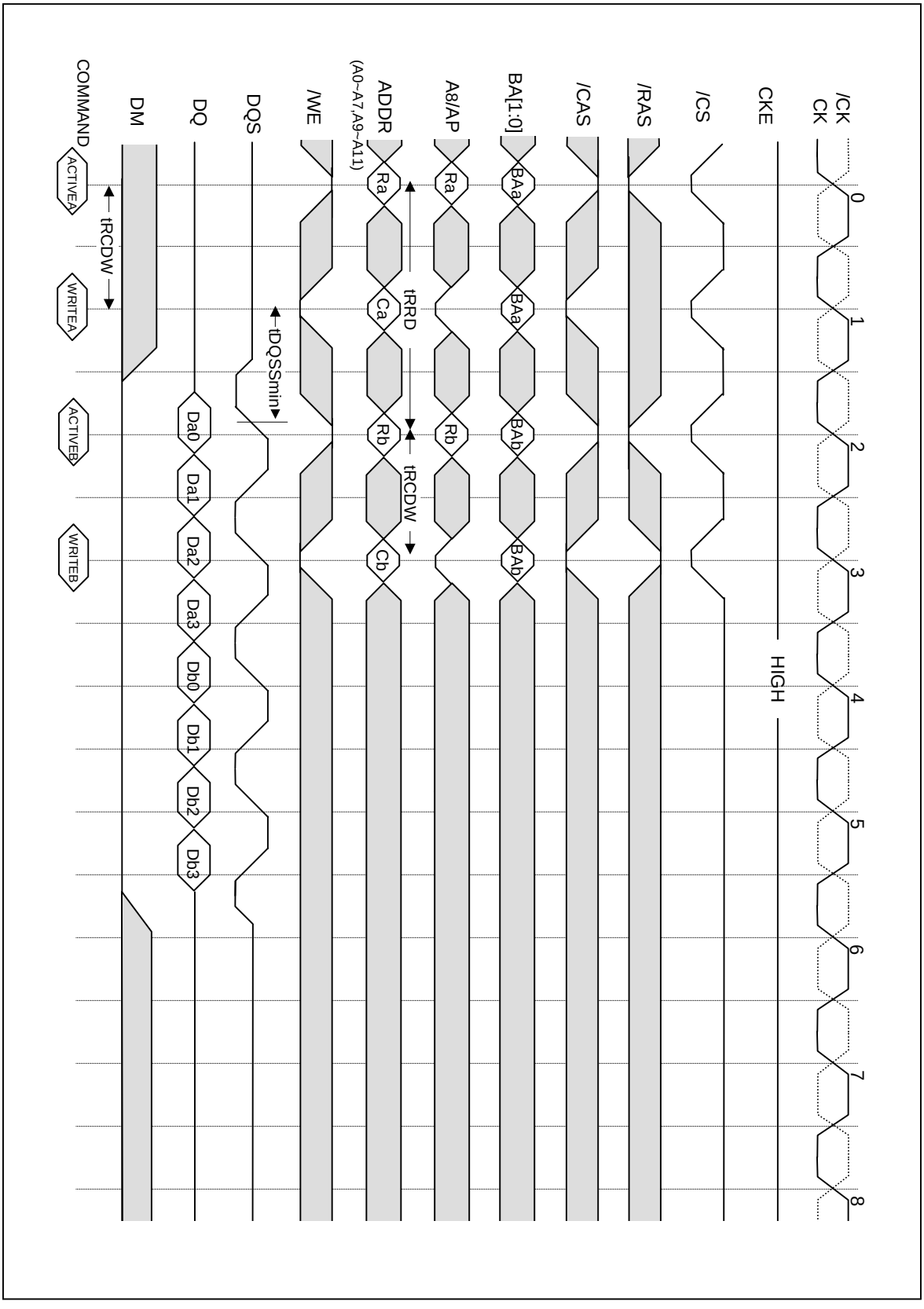
Basic Timing (Setup, Hold and Access Time @BL=2, CL=3)



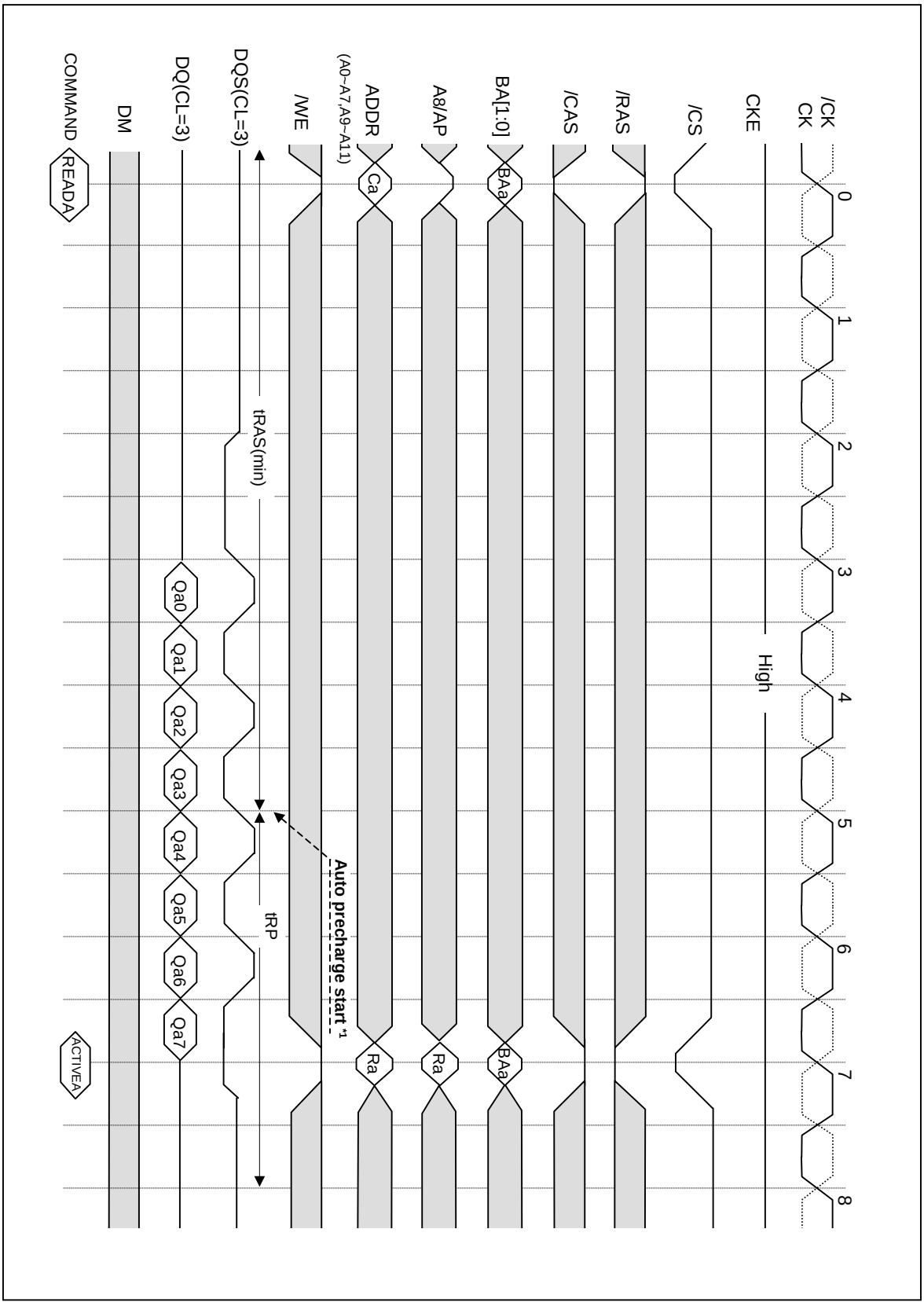
Multi Bank Interleaving READ (@BL=4, CL=3)



Multi Bank Interleaving WRITE (@BL=4, CL=3)

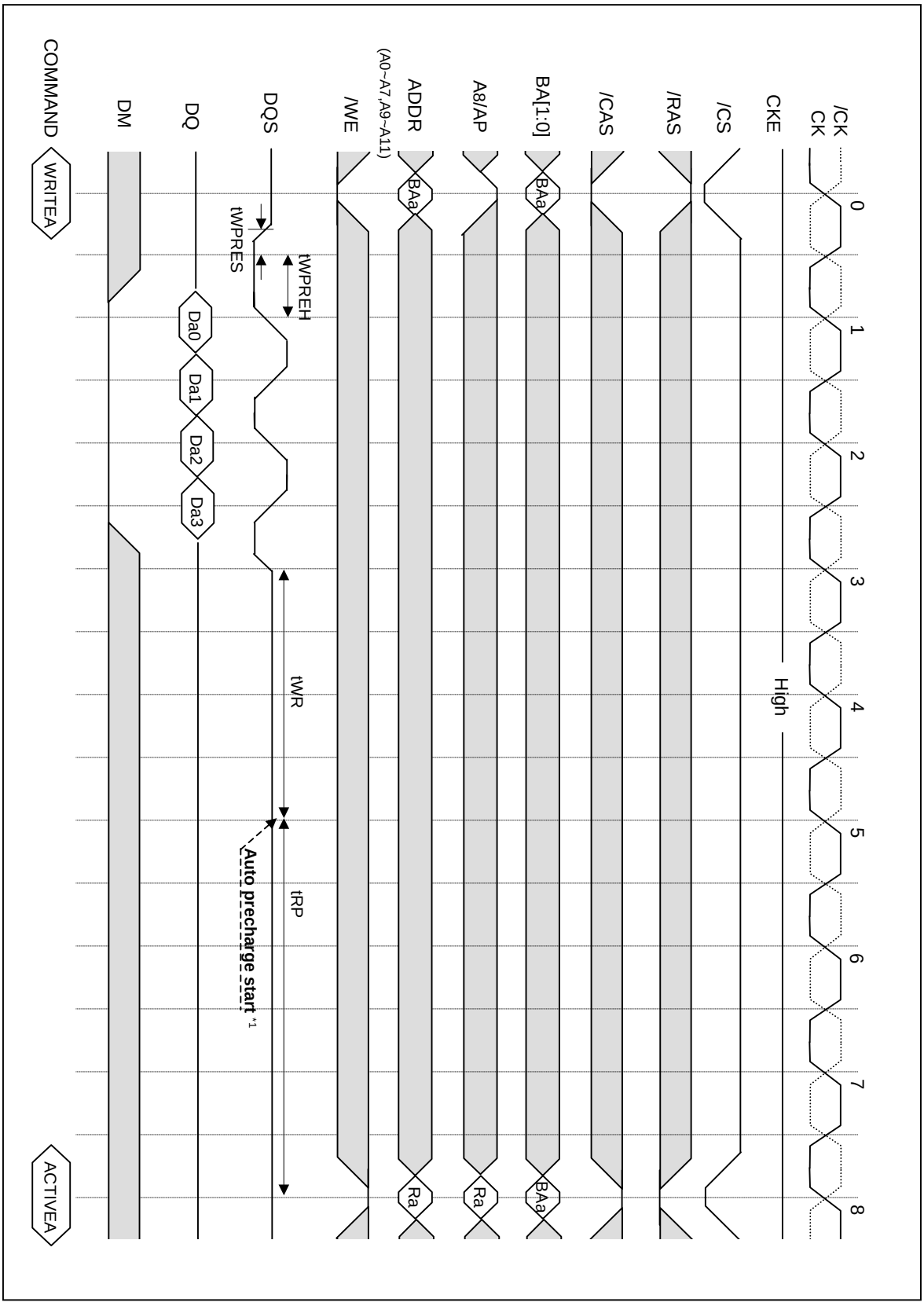


Auto Precharge after READ Burst (@BL=8)



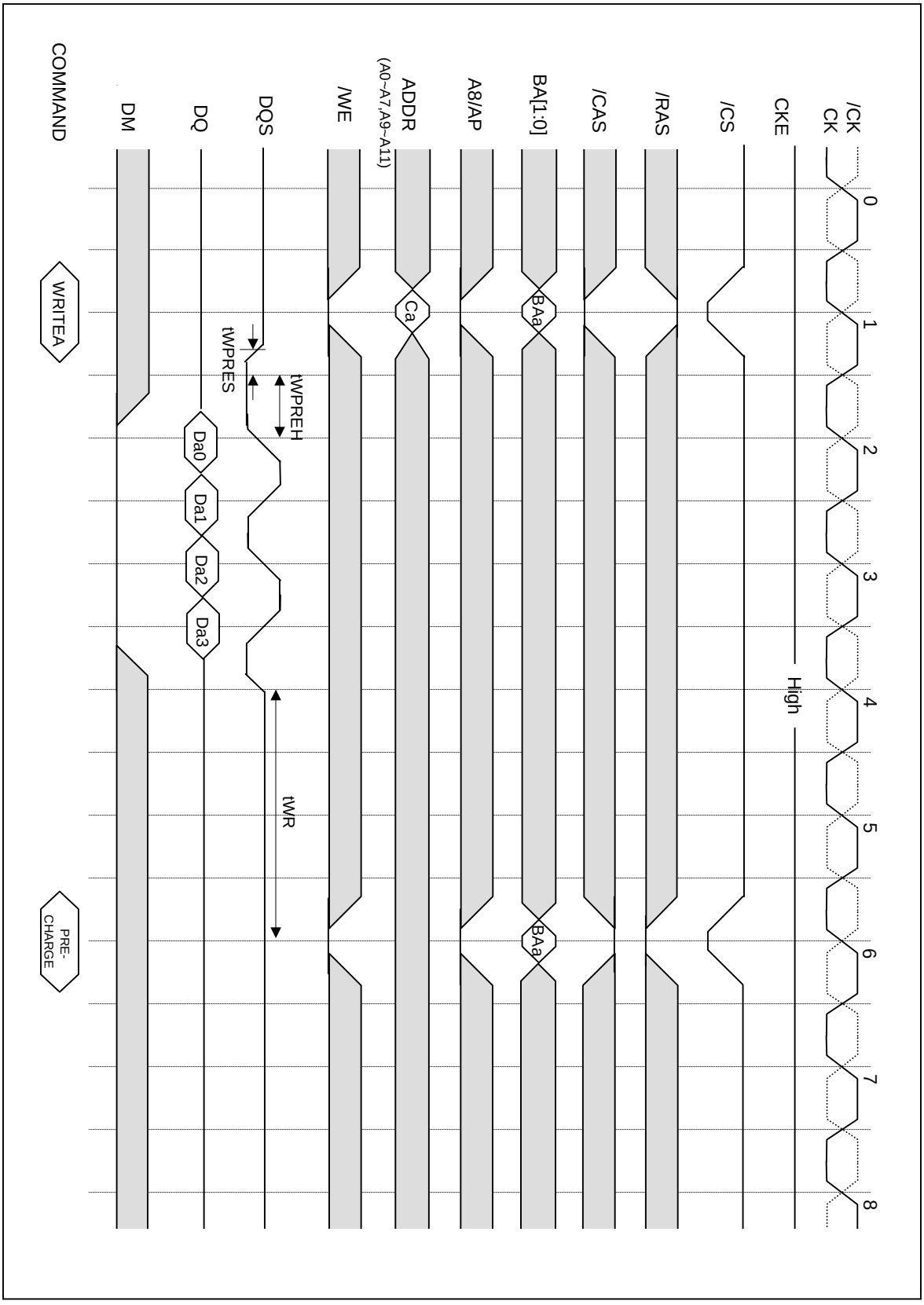
*1 The row active command of the precharged bank can be issued after tRP from this point.

Auto Precharge after WRITE Burst (@BL=4)

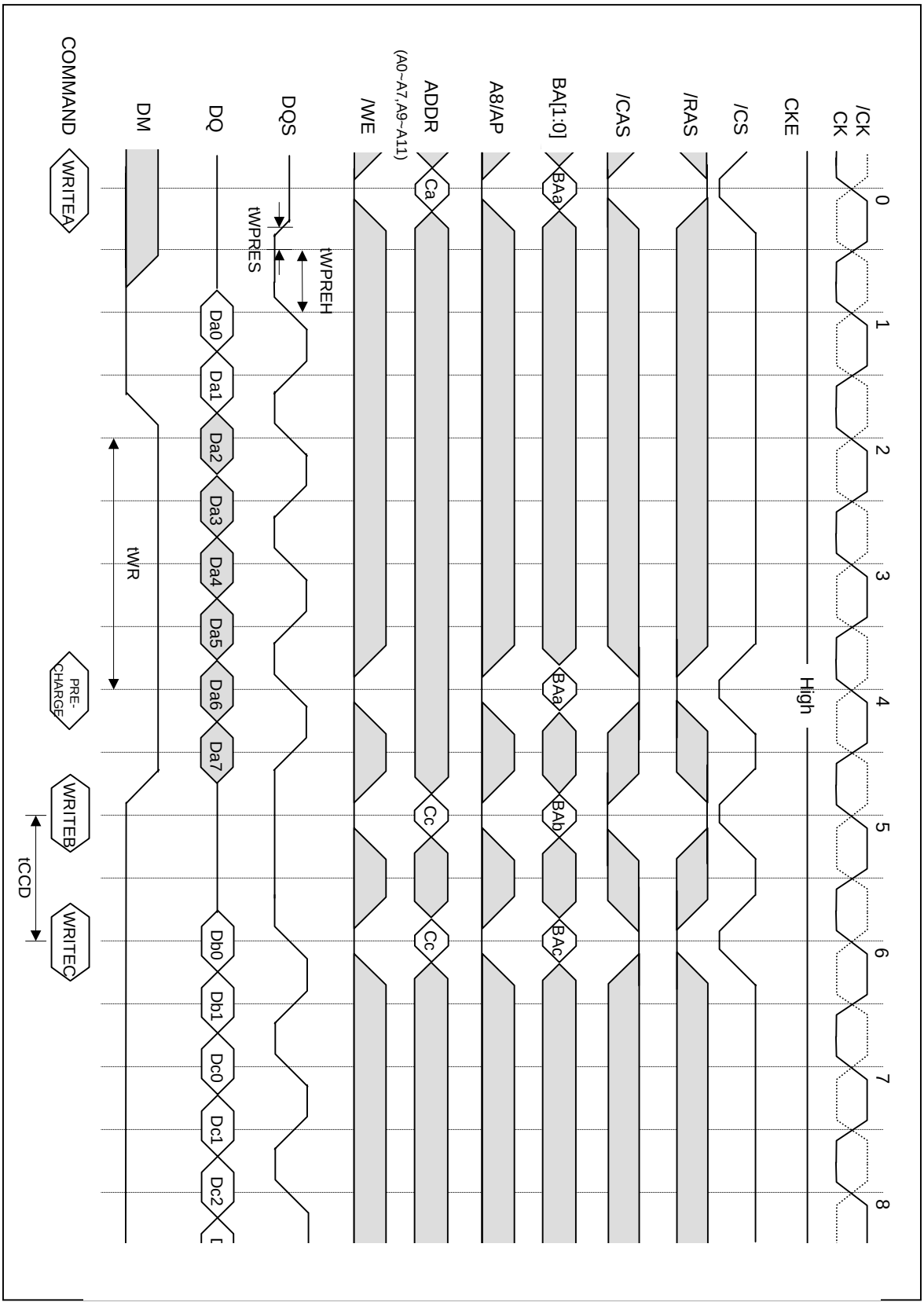


*1 The row active command of the precharged bank can be issued after tRP from this point.

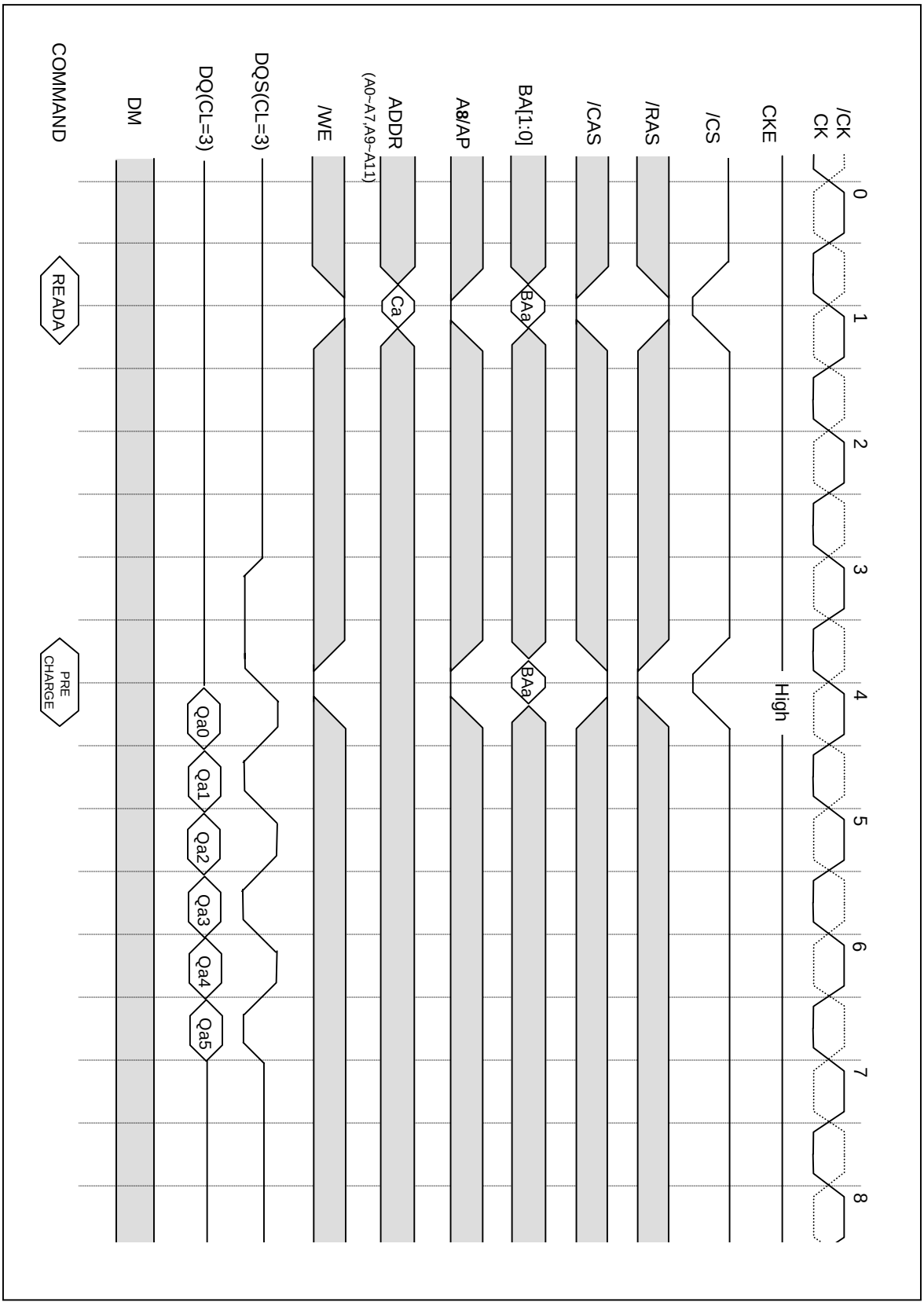
Normal WRITE Burst (@BL=4)



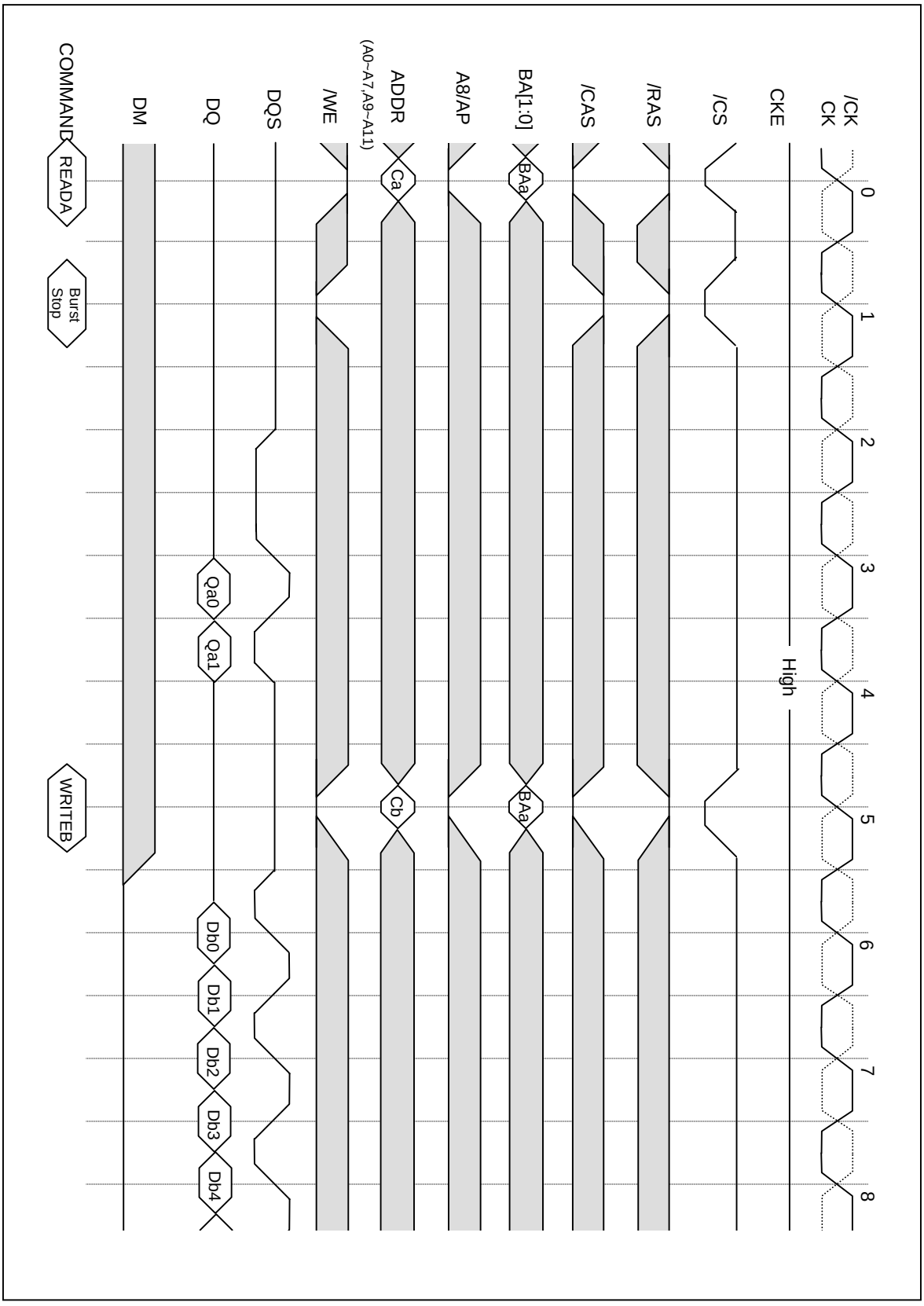
Write Interrupted by Precharge & DM (@BL=8)



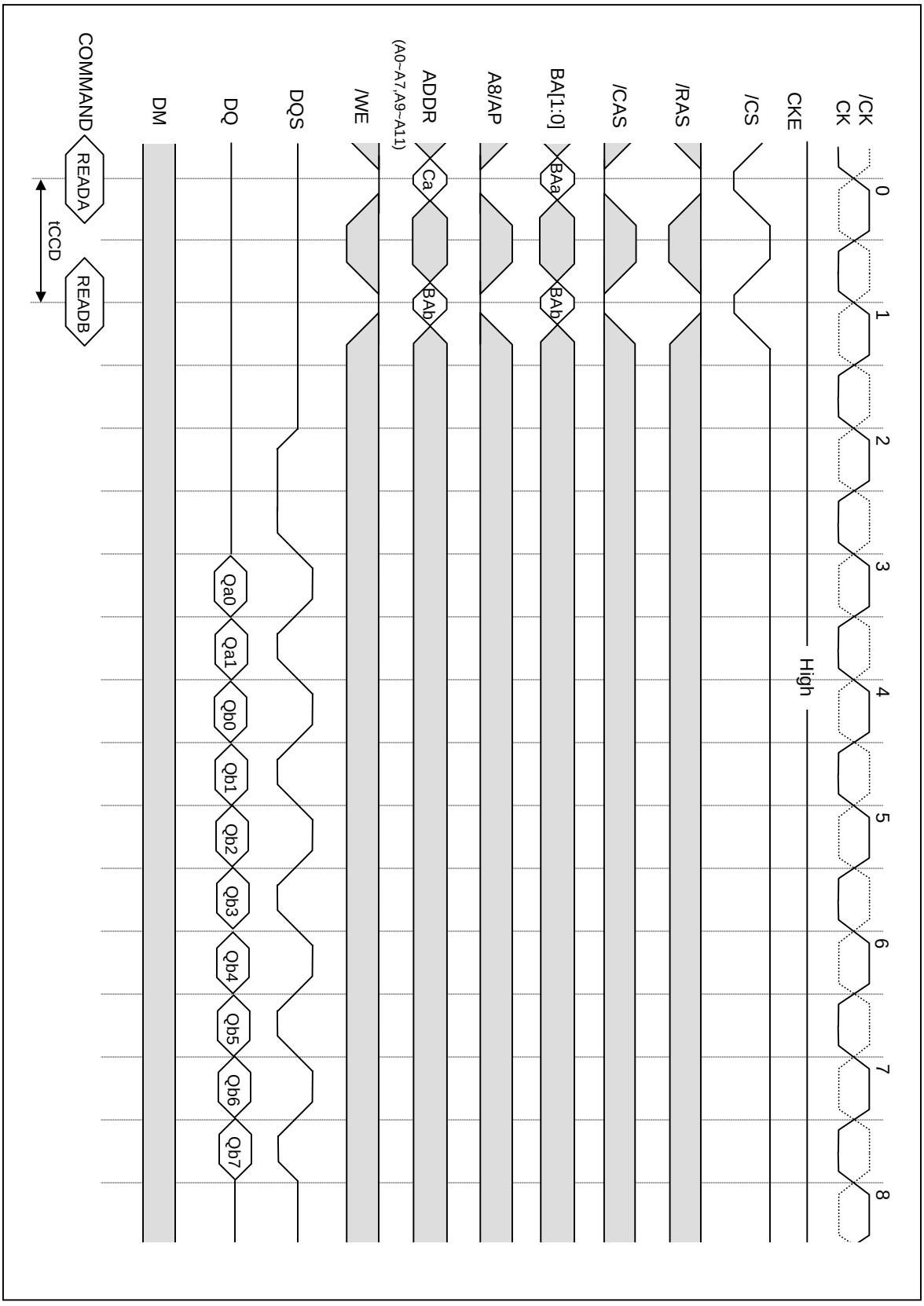
Read Interrupted by Precharge (@BL=8)



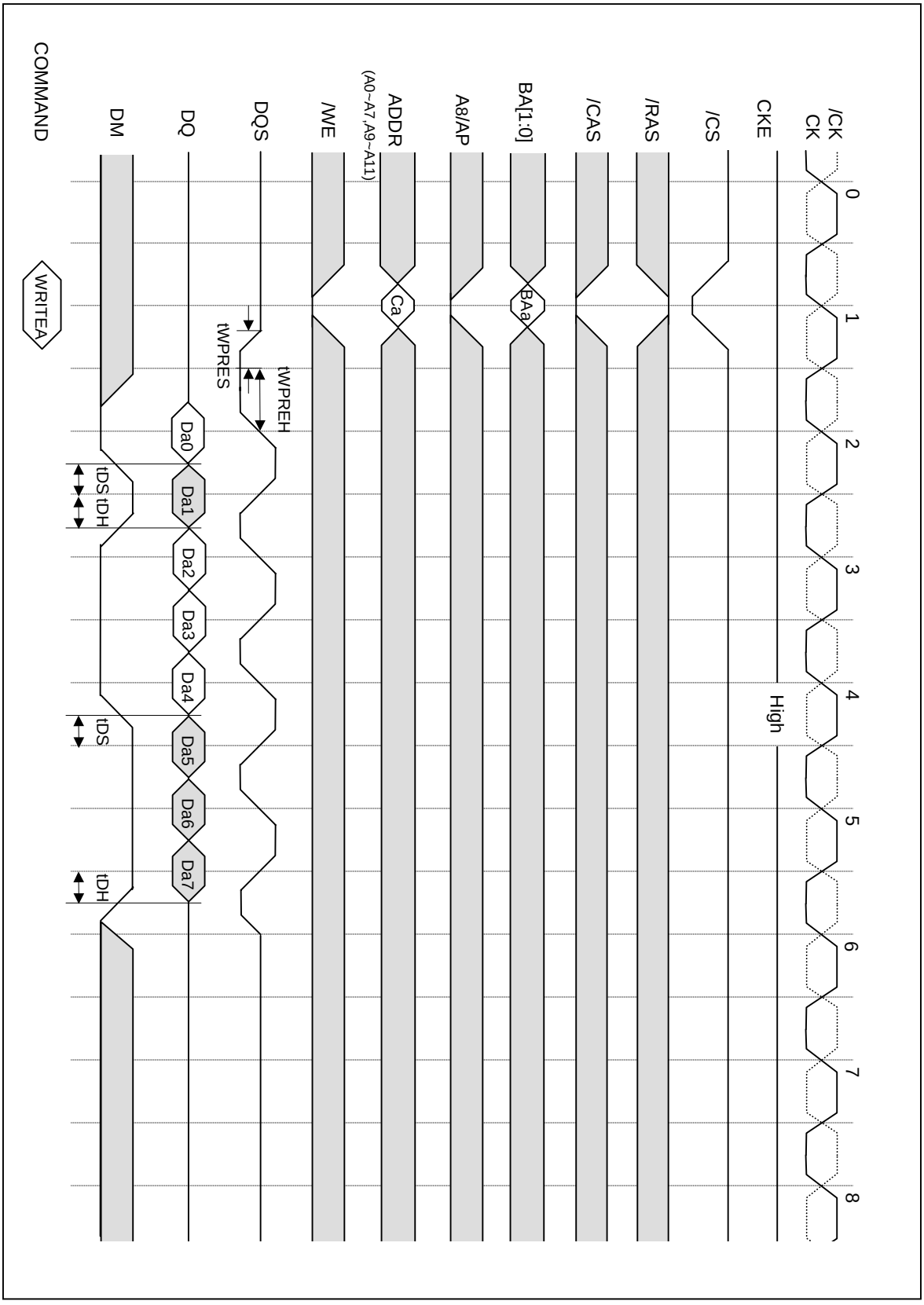
Read Interrupted by Burst stop & Write (@BL=8, CL=3)



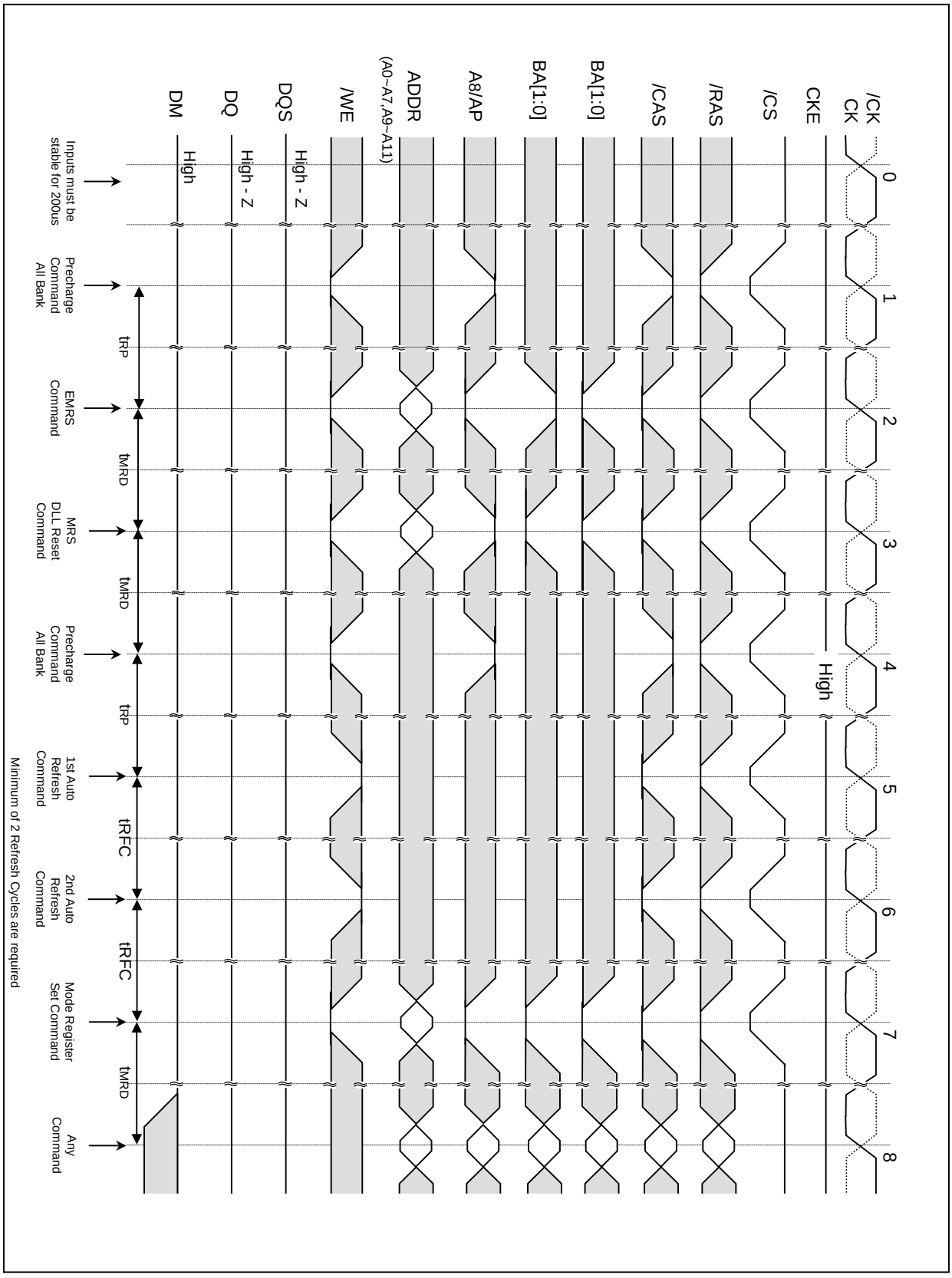
Read Interrupted by Read (@BL=8, CL=3)



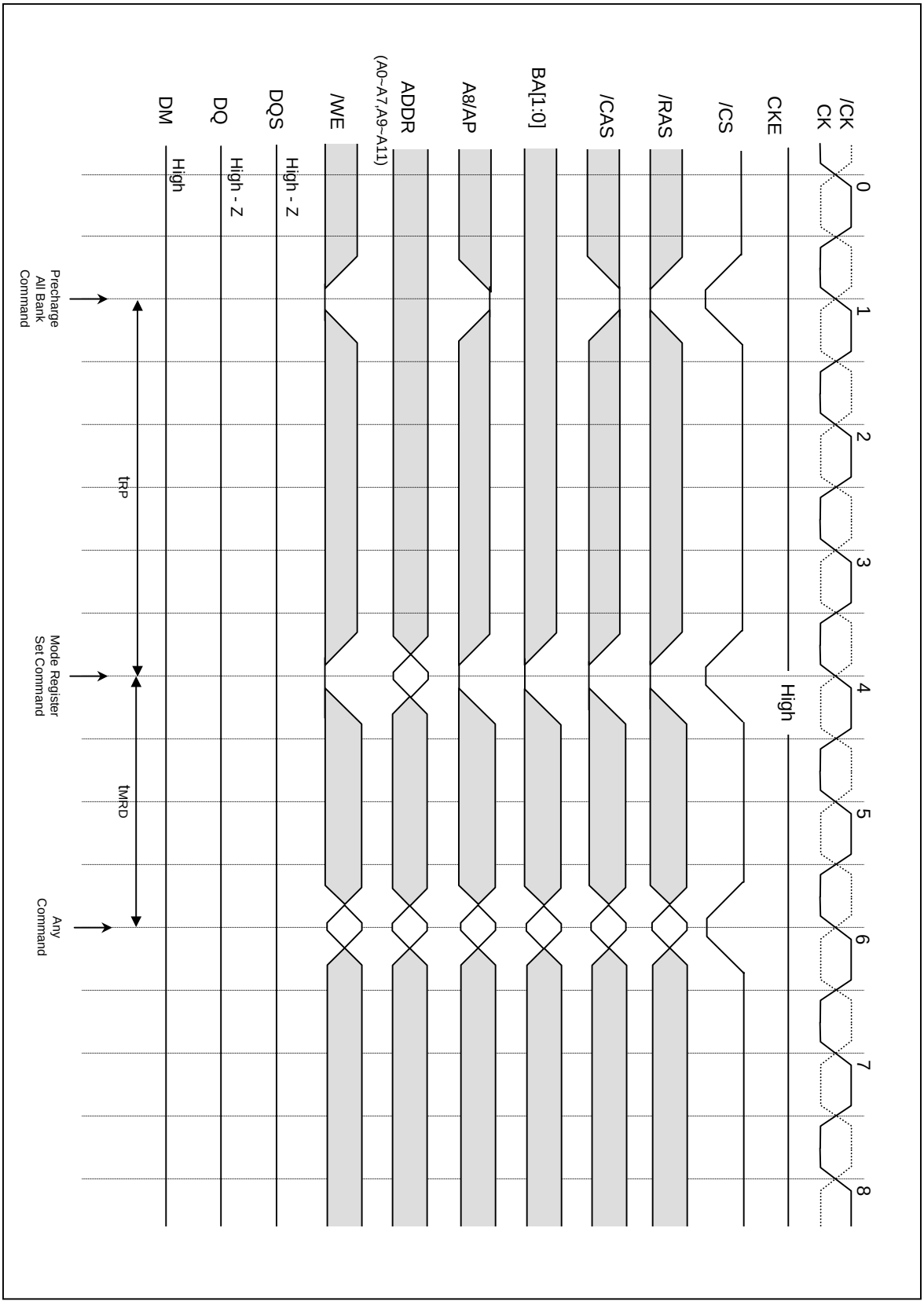
DM Function (@BL=8) only for write



Power up Sequence & Auto Refresh (CBR)



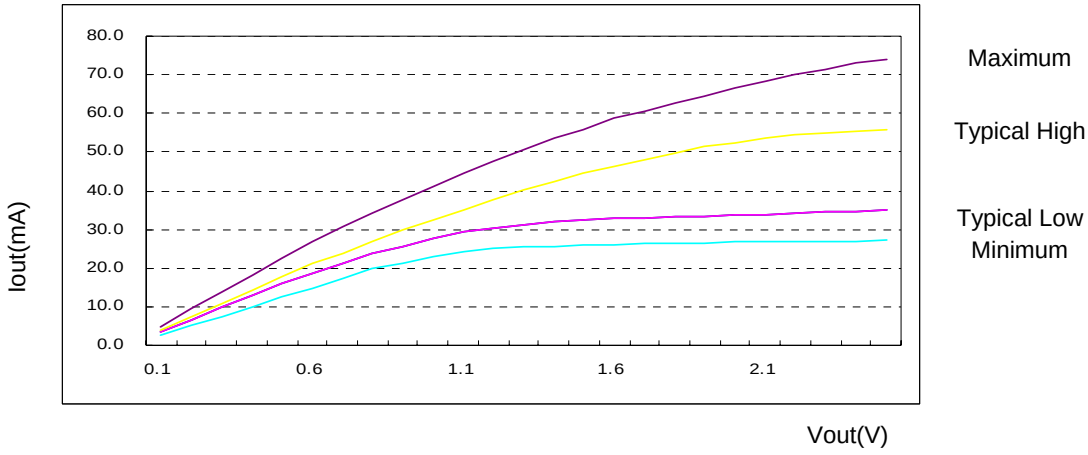
Mode Register Set



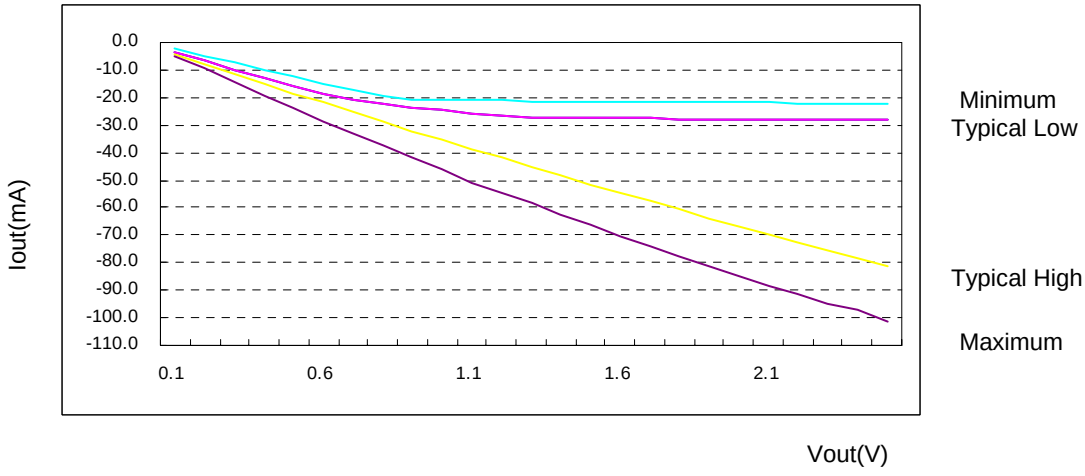
IBIS : I/V CHARACTERISTICS FOR INPUT AND OUTPUT BUFFERS

Reduced Output Driver Characteristics.

1. The nominal pulldown V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below figure.
2. The full variation in driver pulldown current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure



3. The nominal pullup V-I curve for DDR SDRAM devices will be within the inner bounding lines of the V-I curve of below figure.
4. The full variation in driver pullup current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of below figure



5. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7, for device drain to source voltage from 0 to VDDQ/2
6. The full variation in the ratio of the nominal pullup to pulldown current should be unity ±0%, for device drain to source voltages from 0 to VDDQ/2

Voltage (V)	Pulldown Current(mA)				Pullup Current(mA)			
	Typical Low	Typical High	Minimum	Maximum	Typical Low	Typical High	Minimum	Maximum
0.1	3.3	3.7	2.5	4.8	-3.3	-4.1	-2.5	-4.9
0.2	6.6	7.3	5.0	9.4	-6.6	-7.8	-5.0	-9.7
0.3	9.8	10.9	7.4	14.0	-9.8	-11.4	-7.4	-14.5
0.4	13.0	14.4	10.0	18.3	-12.9	-14.9	-10.0	-19.2
0.5	16.1	17.8	12.4	22.6	-16.1	-18.4	-12.4	-23.9
0.6	18.7	21.1	14.9	26.7	-18.5	-21.9	-14.9	-28.4
0.7	21.3	23.9	17.4	30.7	-20.5	-25.3	-17.4	-32.9
0.8	23.6	26.9	19.9	34.1	-22.2	-28.7	-19.5	-37.3
0.9	25.6	29.8	21.4	37.7	-23.6	-32.1	-20.6	-41.7
1.0	27.7	32.6	23.0	41.2	-24.8	-35.4	-20.9	-46.0
1.1	29.2	35.2	24.2	44.5	-25.8	-38.6	-21.1	-50.7
1.2	30.3	37.7	25.0	47.7	-26.6	-41.9	-21.2	-54.3
1.3	31.3	40.1	25.4	50.7	-27.0	-45.2	-21.3	-58.4
1.4	32.0	42.4	25.6	53.5	-27.2	-48.4	-21.4	-62.4
1.5	32.5	44.4	25.8	56.0	-27.4	-51.6	-21.5	-66.4
1.6	32.7	46.4	25.9	58.6	-27.5	-54.7	-21.6	-70.4
1.7	32.9	48.1	26.2	60.6	-27.6	-57.8	-21.7	-73.8
1.8	33.2	49.8	26.4	62.6	-27.7	-60.7	-21.8	-77.8
1.9	33.5	51.5	26.5	64.6	-27.8	-64.1	-21.8	-81.3
2.0	33.8	52.5	26.7	66.6	-27.9	-67.0	-21.9	-84.7
2.1	33.9	53.5	26.8	68.3	-28.0	-69.8	-21.9	-88.1
2.2	34.2	54.5	26.9	69.9	-28.1	-72.7	-22.0	-91.6
2.3	34.5	55.0	27.0	71.5	-28.2	-75.6	-22.0	-95.0
2.4	34.6	55.5	27.0	72.9	-28.2	-78.4	-22.1	-97.0
2.5	34.9	56.0	27.1	74.1	-28.3	-81.3	-22.2	-101.3

Temperature (Ambient)

Typical	25° C
Minimum	70°C
Maximum	0°C

Vdd/Vddq

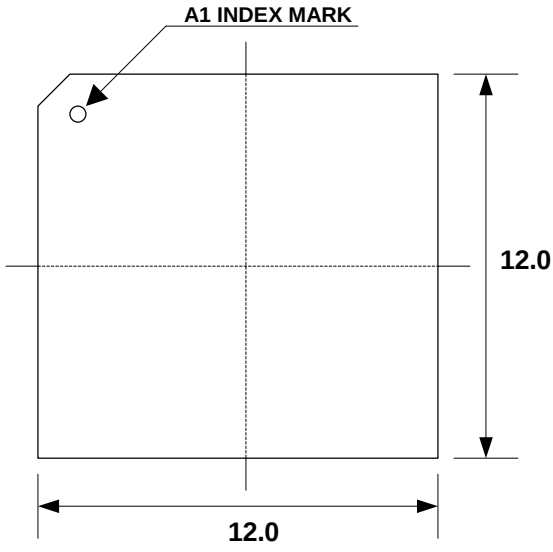
Typical	2.50V / 2.50V
Minimum	2.375V / 2.375V
Maximum	2.625V / 2.625V

The above characteristics are specified under best, worst and normal process variation/conditions

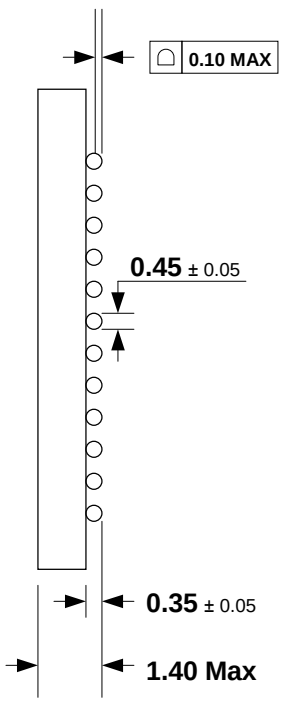
Impedance Match Output Driver Characteristics.

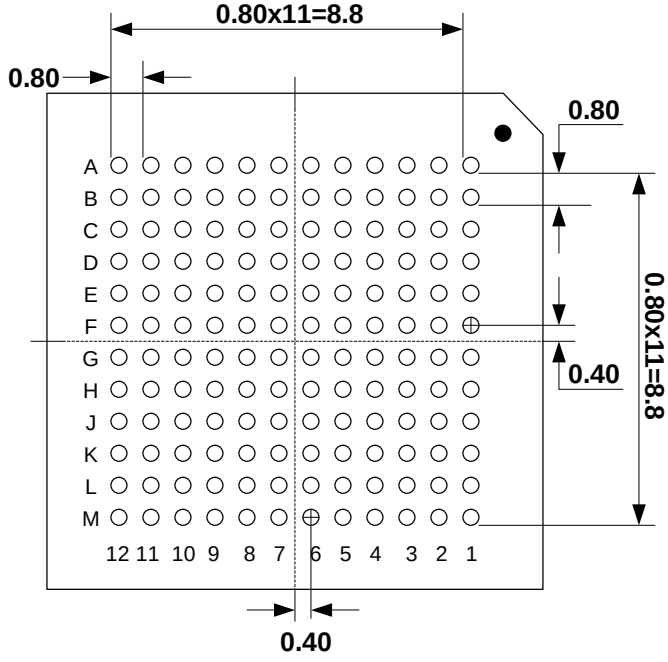
IN JEDEC

PACKAGE DIMENSIONS (144-Balla FBGA)



<Top View>





< Bottom View >