SGS-THOMSON MICROELECTRONICS

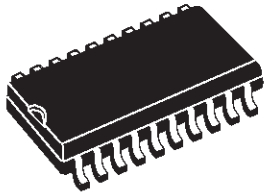
ITA6V5B3 / ITA10B3
ITA18B3 / ITA25B3

Application Specific Discretes
A.S.D.™

BIDIRECTIONAL TRANSIL™ ARRAY FOR DATALINE PROTECTION

APPLICATIONS

Differential data transmission lines protection :
- RS-232
- RS-423
- RS-422
- RS-485

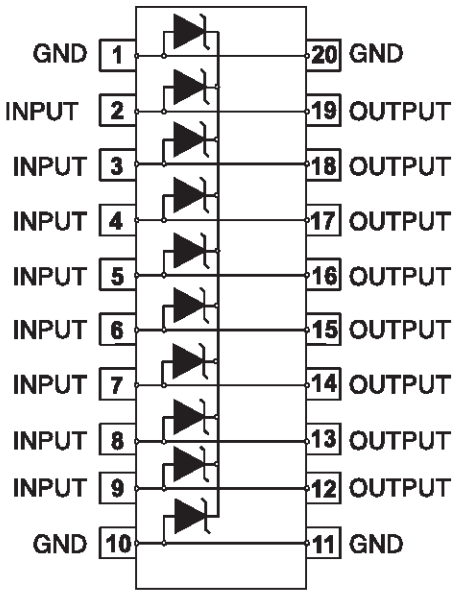


SO20

FEATURES

- HIGH SURGE CAPABILITY TRANSIL ARRAY I_{PP} = 40 A (8/20µs)
- PEAK PULSE POWER : 300 W (8/20µs)
- SEPARATED INPUT-OUTPUT
- UP TO 9 BIDIRECTIONAL TRANSIL FUNCTIONS
- LOW CLAMPING FACTOR (V_{CL} / V_{BR}) AT HIGH CURRENT LEVEL
- LOW LEAKAGE CURRENT
- ESD PROTECTION UP TO 15kV

FUNCTIONAL DIAGRAM



DESCRIPTION

Transil diode arrays provide high overvoltage protection by clamping action. Their instantaneous response to transient overvoltages makes them particularly suited to protect voltage sensitive devices such as MOS Technology and low voltage supplied IC's.

The ITA series allies high surge capability against energetic pulses with high voltage performance against ESD.

The separated input/output configuration of the device ensures improved protection against very fast transient overvoltage like ESD by elimination of the spikes induced by parasitic inductances created by external wiring.

COMPLIES WITH THE FOLLOWING STANDARDS :

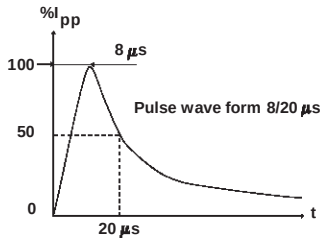
IEC 1000-4-2 : level 4
IEC 1000-4-4 : level 4
IEC 1000-4-5 : level 2

MIL STD 883C - Method 3015-6 : class 3
(human body model)

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

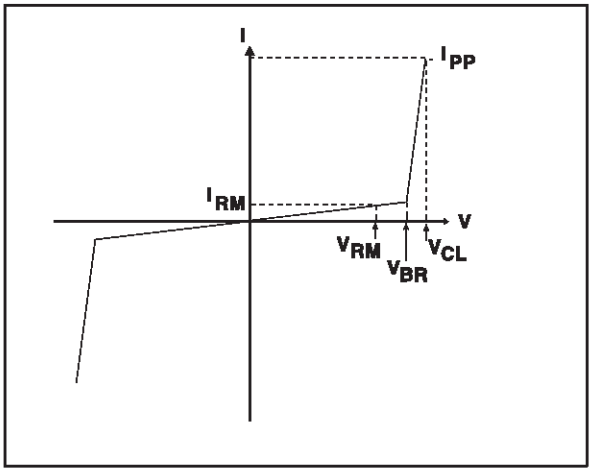
Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power dissipation (8/20µs) (see note 1)	Tj initial = T_{amb}	300	W
I_{PP}	Peak pulse current (8/20µs) (see note 1)	Tj initial = T_{amb}	40	A
I^2t	Wire I^2t value (see note 1)		0.6	A^2s
T_{stg} T_j	Storage temperature range Maximum operating junction temperature		- 55 to + 150 125	°C °C
T_L	Maximum lead temperature for soldering during 10s		260	°C

Note 1 : For surges greater than the specified maximum value, the I/O will first present a short-circuit and after an open circuit caused by the wire melting.



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Junction capacitance



Types	I_{RM} @ V_{RM} max.		V_{BR} @ I_R min. note 2		V_{CL} @ I_{PP} 8/20µs note 2		V_{CL} @ I_{PP} max. 8/20µs note 2		αT max.	C max. note 3
	µA	V	V	mA	V	A	V	A	10^{-4}/°C	pF
ITA6V5B3	**10**	**5**	**6.5**	**1**	**9.5**	**10**	**11**	**25**	**4**	**1100**
ITA10B3	4	8	10	1	13	10	17	25	8	800
ITA18B3	4	15	18	1	21	10	26	25	9	500
ITA25B3	**4**	**24**	**25**	**1**	**31**	**10**	**36**	**25**	**12**	**420**

Note 2 : Between I/O pin and ground.
Note 3 : Between two input Pins at 0V Bias.

Preferred types in bold.

Fig. 1 : Typical peak pulse power versus exponential pulse duration.

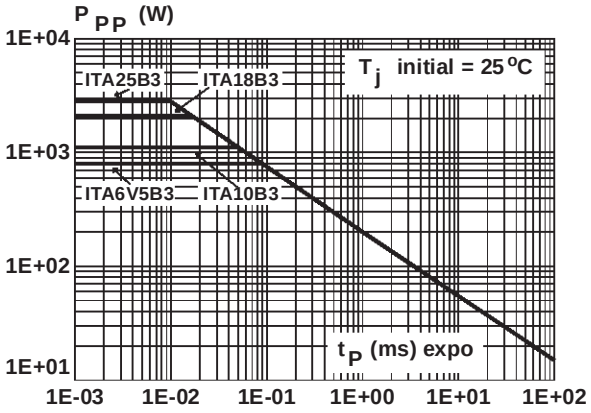


Fig. 2 : Clamping voltage versus peak pulse current (exponential waveform 8/20 µs).

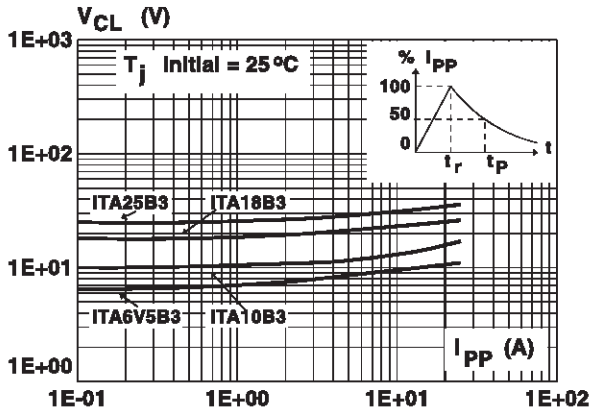


Fig. 3 : Peak current I_{DC} inducing open circuit of the wire for one input/output versus pulse duration (typical values).

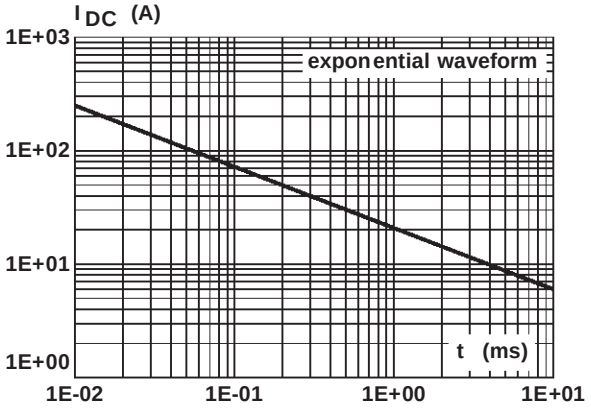


Fig. 4 : Junction capacitance versus reverse applied voltage for one input/output (typical values).

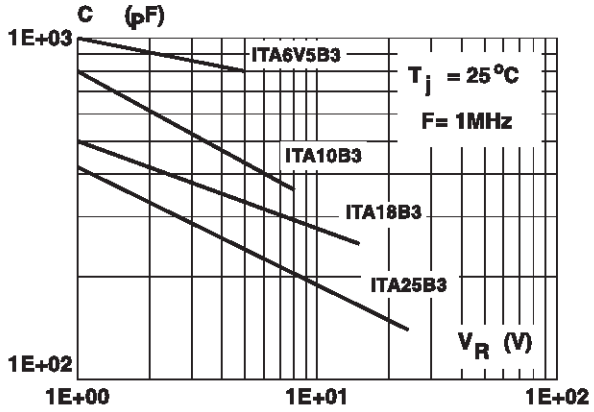
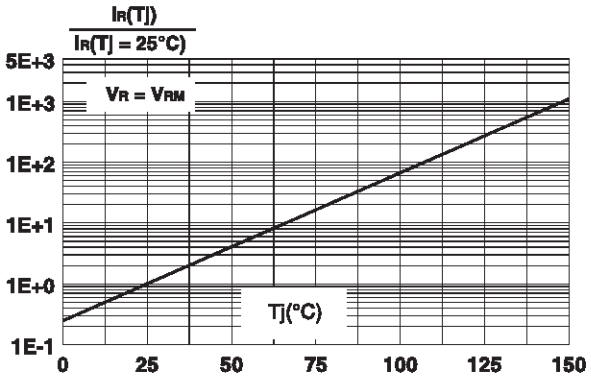


Fig. 5 : Relative variation of leakage current versus junction temperature

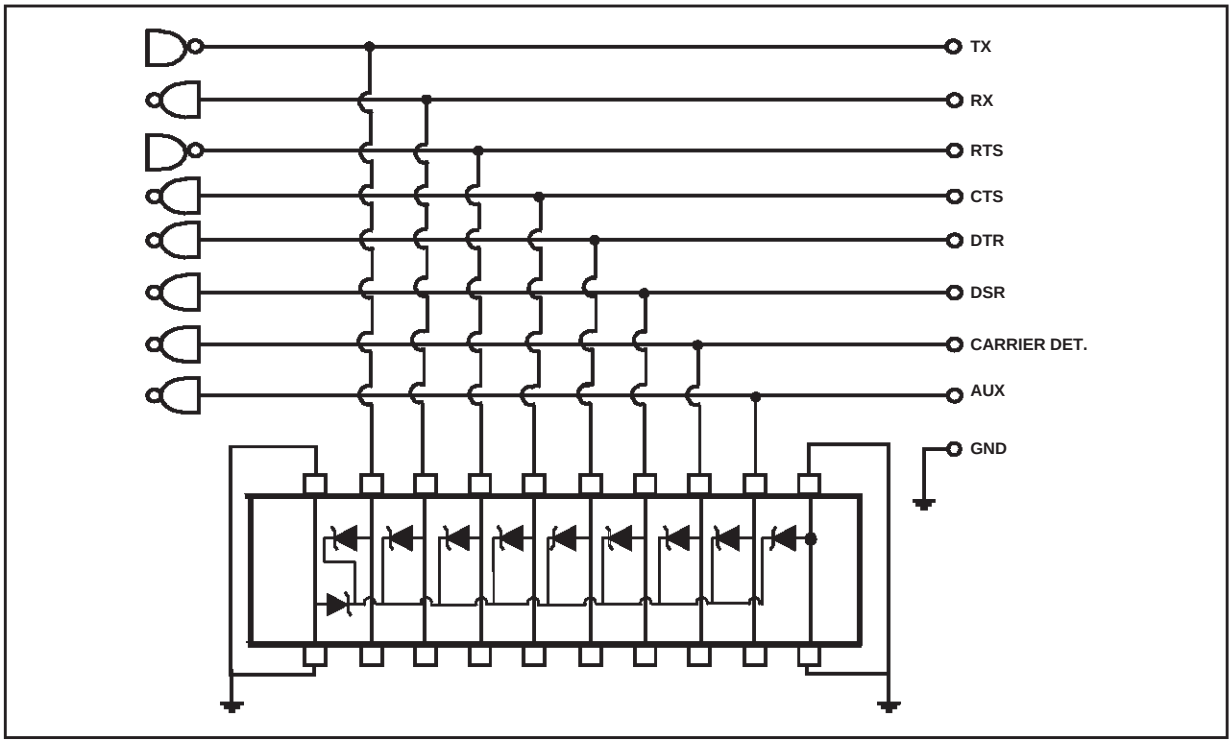


APPLICATION INFORMATION

Types	Maximum differential voltage between two input pins at 25°C
ITA6V5B3	+ / - 3.5 V
ITA10B3	+ / - 5.0 V
ITA18B3	+ / - 9.0 V
ITA25B3	+ / - 12.5 V

This monolithic Transil Array is based on 10 unidirectional Transils with a common cathode and can be configurated to offer up to 9 bidirectional functions. This imposes a maximum differential voltage between 2 input pins (see opposite table).

Typical application : RS232 junction.



APPLICATION NOTICE

Design advantage of ITAxxxB3 used with 4-point structure.

The ITAxxxB3 has been designed with a 4-point structure (separated Input/output) in order to efficiently protect against disturbances with very high di/dt rates, such as ESD.

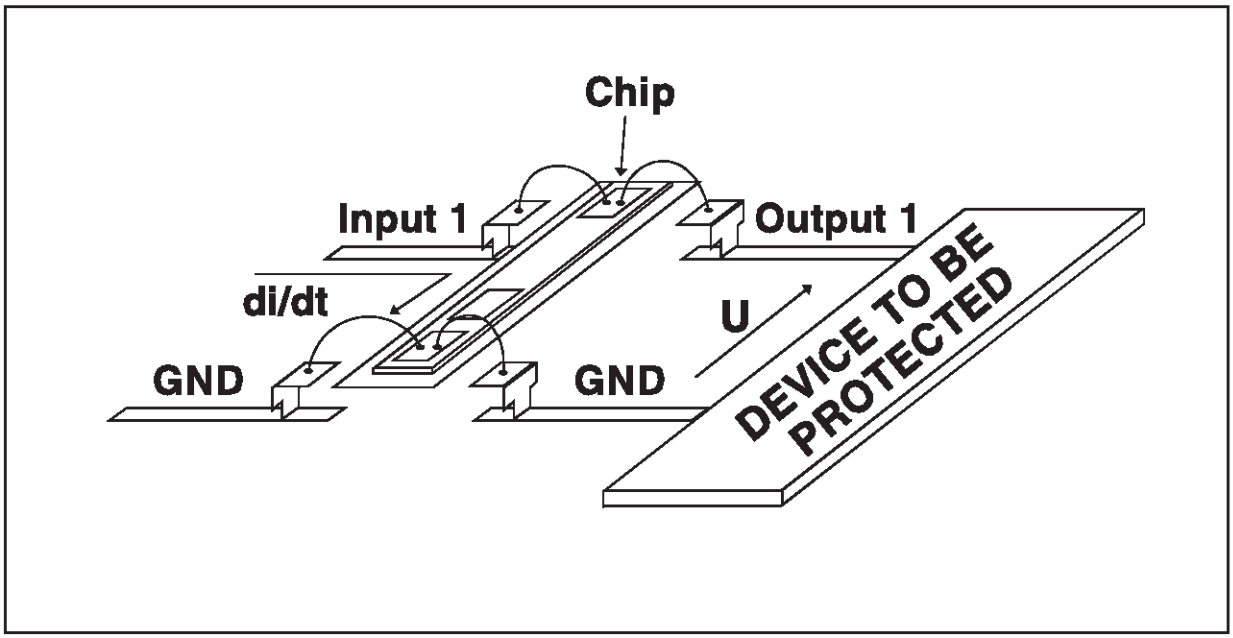
The purpose of this 4-point structure is to eliminate the overvoltage introduced by the parasitic inductances of the wiring (Ldi/dt).

Efficient protection depends not only on the component itself, but also on the circuit layout. The drawing given in figure shows the layout to be used in order to take advantage of the 4-point structure of the ITAxxxB3.

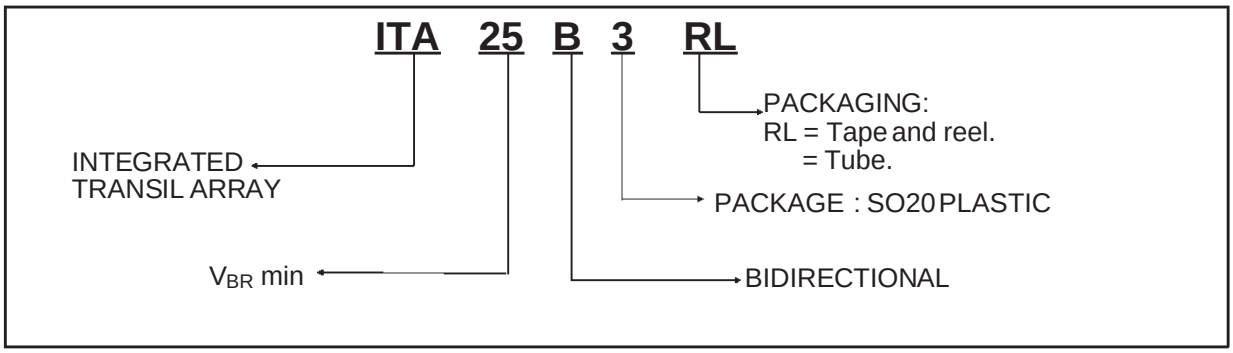
With this layout, each line to be protected passes through the protection device.

In this way, it realizes an interface between the data line and the circuit to be protected, guaranteeing an isolation between its inputs and outputs.

The 4 - point structure layout.



ORDER CODE

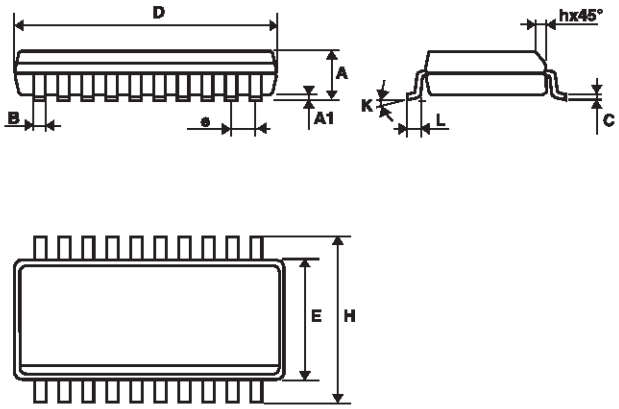


MARKING

TYPE	MARKING
ITA6V5B3	ITA6V5B2
ITA10B3	ITA10B3
ITA18B3	ITA18B3
ITA25B3	ITA25B3

PACKAGE MECHANICAL DATA

SO20 (Plastic)



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.65			0.104
A1	0.10		0.20	0.004		0.008
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13.0	0.484		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h		0.50			0.020	
L	0.50		1.27	0.020		0.050
K	8° (max)					

Packaging : standard packaging is tape and reel.

Weight : 0.55g.