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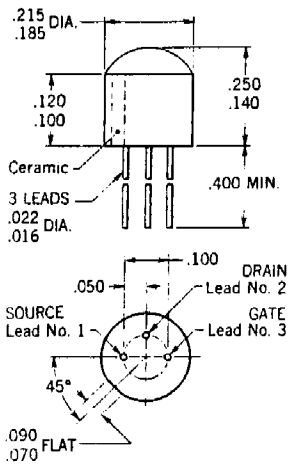
2N4342 – 2N4343 – 2N4360

P-CHANNEL FIELD EFFECT TRANSISTORS
DIFUSSED SILICON PLANAR TRANSSITORS

- **LOW NOISE VOLTAGE -- 0.08 $\mu V/\sqrt{Hz}$ (MAX) @ 100 Hz**
- **HIGH Y_{fs} -- 4000 µmhos (MIN)**
- **LOW r_{DS} (on) -- 350 Ω (MAX)**
- **LOW COST EPOXY PACKAGE**

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Operating Junction Temperature	125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature (10 seconds time limit)	260°C

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Note 2)	0.5 Watt
at 65°C Case Temperature (Note 2)	0.3 Watt
at 25°C Ambient Temperature (Note 2)	0.2 Watt

Maximum Voltages

		2N4360	2N4342 2N4343
BV_{SGO}	Source to Gate Breakdown Voltage	-20 Volts	-25 Volts
BV_{DSO}	Drain to Source Breakdown Voltage	-20 Volts	-25 Volts
BV_{DGO}	Drain to Gate Breakdown Voltage	-20 Volts	-25 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	2N4360 Min.	2N4360 Typ.	2N4360 Max.	2N4342 Min.	2N4342 Typ.	2N4342 Max.	2N4343 Min.	2N4343 Typ.	2N4343 Max.	Units	Test Conditions
e_n	**Equivalent Input Noise Voltage** (f = 100 Hz)		0.02	0.08		0.02	0.08		0.02	0.08	µV/√Hz	V_{DS} = -10 V V_{GS} = 0
NF	Noise Figure (f = 100 Hz)		0.1	1.5		0.1	1.5		0.1	1.5	dB	V_{DS} = -10 V V_{GS} = 0 R_G = 1.0 MΩ BW = 15 Hz
$\|Y_{fs}\|$	**Forward Transadmittance** (f = 1.0 kHz)	2000	4000	8000	2000	3500	6000	4000	6000	8000	µmhos	V_{DS} = -10 V V_{GS} = 0
Y_{os}	Output Admittance (f = 1.0 kHz)		35	100		25	75		35	100	µmhos	V_{DS} = -10 V V_{GS} = 0
BV_{GSS}	Gate to Source Breakdown Voltage	20			25			25			Volts	I_G = 10 µA V_{DS} = 0
I_{DSS}	**Drain Current**	3.0	10	30	4.0	7.0	12	10	18	30	mA	V_{DS} = -10 V V_{GS} = 0
V_{GS}	Gate to Source Voltage	0.7	5.0	9.0							Volts	V_{DS} = -10 V I_D = 0.3 mA
V_{GS}	Gate to Source Voltage				0.7	3.0	5.0				Volts	V_{DS} = -10 V I_D = 0.4 mA
V_{GS}	Gate to Source Voltage							1.8	6.0	9.0	Volts	V_{DS} = -10 V I_D = 1.0 mA
$V_{GS(off)}$	**Gate to Source Cutoff Voltage**			10			5.5			10	Volts	V_{DS} = -10 V I_D = 1.0 µA
I_{GSS}	Gate Reverse Current		0.15	10		0.15	10		0.15	10	nA	V_{GS} = 15 V V_{DS} = 0
I_{GSS}(65 C)	Gate Reverse Current		.002	0.5		0.002	0.5		0.002	0.5	µA	V_{GS} = 15 V V_{DS} = 0
C_{iss}	Input Capacitance (f = 1.0 MHz)		15	20		15	20		15	20	pF	V_{DS} = -10 V V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.0	5.0		3.0	5.0		3.0	5.0	pF	V_{DS} = -10 V V_{GS} = 0
$r_{DS(on)}$	**Drain "On" Resistance** (f = 1.0 kHz)		350	700		300	700		180	350	Ohms	I_D = 0 V_{GS} = 0
$R_e(Y_{fs})$	Forward Transconductance (f = 1.0 MHz)	1500	3000		1500	2500		3000	5500		µmhos	V_{DS} = -10 V V_{GS} = 0

*Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(3) Both 2N4342 and 2N4343 typical curves apply to 2N4360.