



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

2SA2127 — PNP Epitaxial Planar Silicon Transistor High-Current Switching Applications

Applications

- Voltage regulators, relay drivers, lamp drivers, electrical equipment

Features

- Adoption of MBIT process
- High current capacity and wide ASO
- Low saturation voltage

Specifications

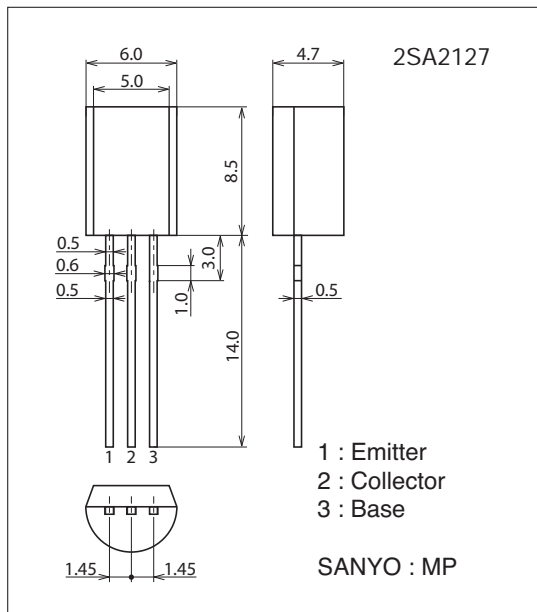
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	VCBO		-50	V
Collector-to-Emitter Voltage	VCEO		-50	V
Emitter-to-Base Voltage	VEBO		-6	V
Collector Current	IC		-2	A
Collector Current (Pulse)	ICP		-4	A
Base Current	IB		-400	mA
Collector Dissipation	PC		1	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		-55 to +150	°C

Package Dimensions

unit : mm (typ)

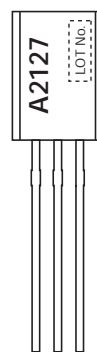
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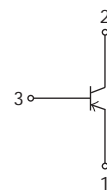
Product & Package Information

- Package : MP
- JEITA, JEDEC : SC-51, TO-92(1-WATT), TO-226AE
- Minimum Packing Quantity : 1,000 pcs./box

Marking



Electrical Connection

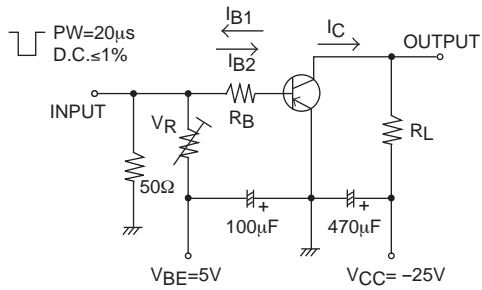


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Electrical Characteristics at $T_a=25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB} = -40\text{V}, I_E = 0\text{A}$			-1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -4\text{V}, I_C = 0\text{A}$			-1	μA
DC Current Gain	h_{FE1}	$V_{CE} = -2\text{V}, I_C = -100\text{mA}$	200		560	
	h_{FE2}	$V_{CE} = -2\text{V}, I_C = -1.5\text{A}$	40			
Gain-Bandwidth Product	f_T	$V_{CE} = -10\text{V}, I_C = -300\text{mA}$		420		MHz
Output Capacitance	C_{ob}	$V_{CB} = -10\text{V}, f = 1\text{MHz}$		16		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1\text{A}, I_B = -50\text{mA}$		-0.2	-0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -1\text{A}, I_B = -50\text{mA}$		-0.9	-1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -10\mu\text{A}, I_E = 0\text{A}$	-50			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -1\text{mA}, R_{BE} = \infty$	-50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -10\mu\text{A}, I_C = 0\text{A}$	-6			V
Turn-On Time	t_{on}	See specified Test Circuit.		35		ns
Storage Time	t_{stg}			250		ns
Fall Time	t_f			24		ns

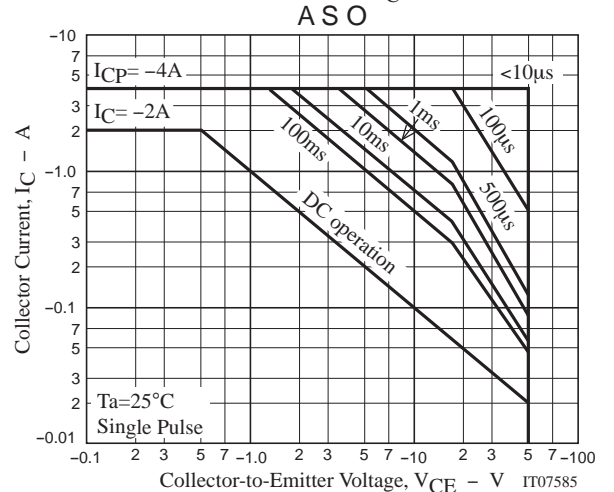
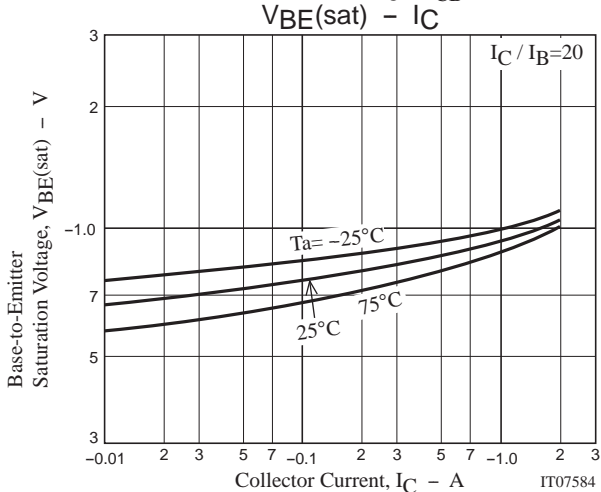
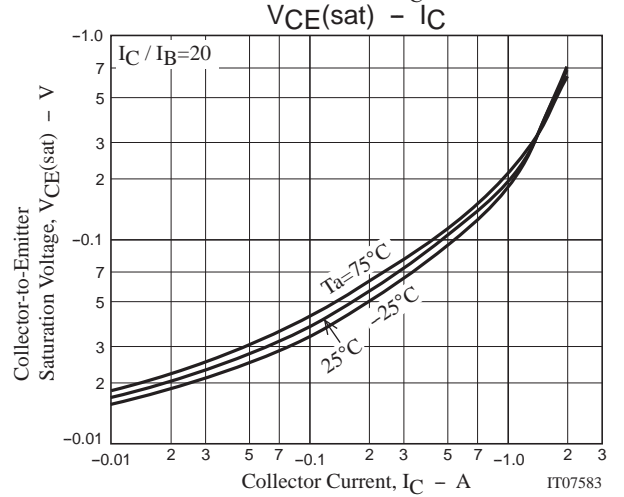
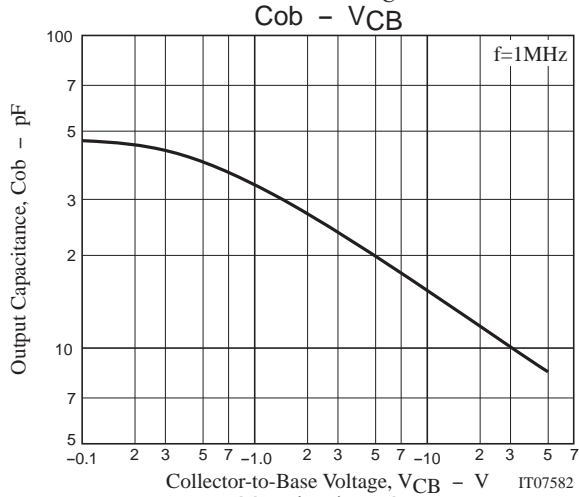
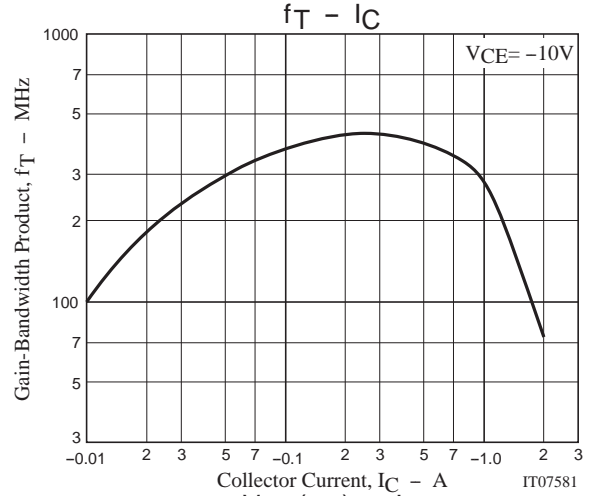
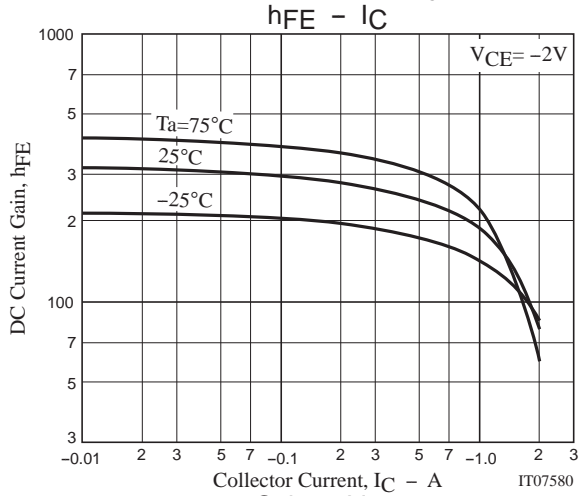
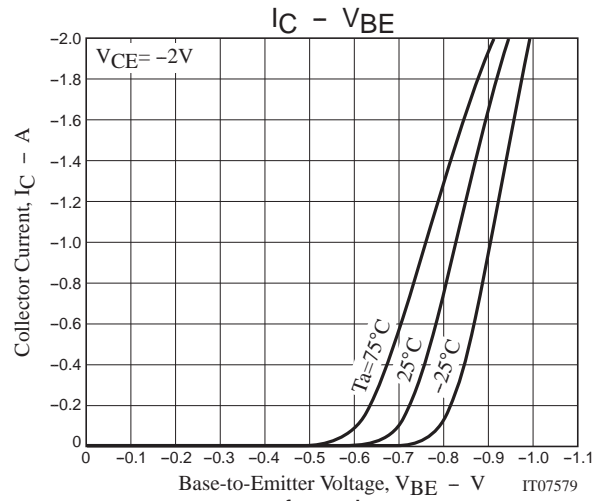
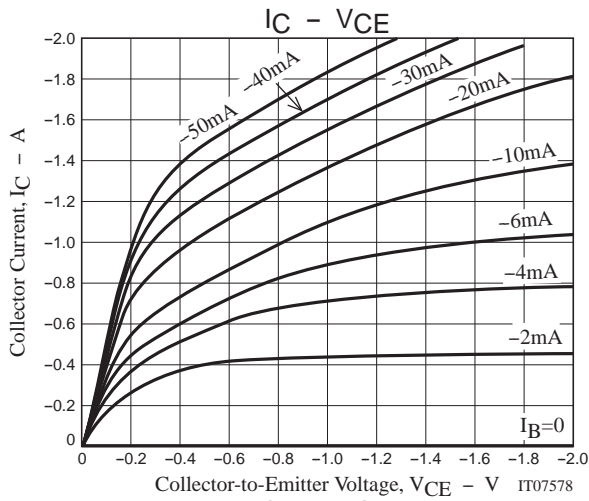
Switching Time Test Circuit

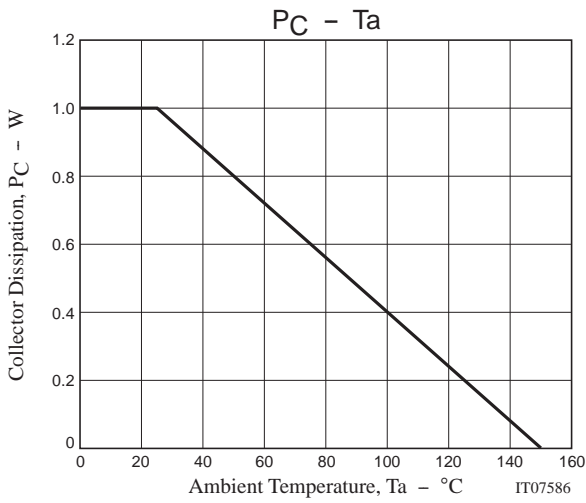


$$I_C = 10I_{B1} = -10I_{B2} = -0.5\text{A}$$

Ordering Information

Device	Package	Shipping	memo
2SA2127	MP	500pcs./bag	Pb Free
2SA2127-AE	MP	1,000pcs./box	





Taping Specification

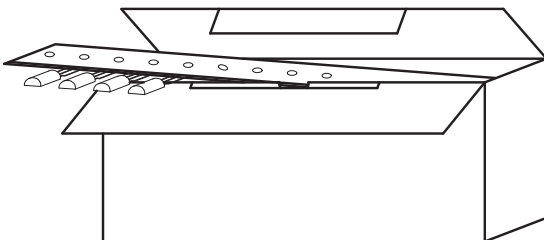
2SA2127-AE

1. Packing Format

Package Name	Packing Type	Maximum Number of devices contained (pcs)		Packing format	
		Inner BOX	number of contained	Outer Box (C-14)	Outer Box (C-15)
M P	AE/AZ	C-3 Dimensions:mm (external) 330×45×125	1,000	1 Inner Box contained (16,000pcs) Dimensions:mm (external) 500×345×195	8 Inner Box contained (8,000pcs) Dimensions:mm (external) 345×260×195
	A J	C-5 Dimensions:mm (external) 330×45×245	2,000	8 Inner Box contained (16,000pcs) Dimensions:mm (external) 500×345×195	4 Inner Box contained (8,000pcs) Dimensions:mm (external) 345×260×195

Packing method

Put zigzag folding in an inner box.



Inner box label

(unit:mm)

Type No. →	(1) TYPE 00000000	43
Lot No. →	(17) LOT 00	
Quantity →	(20) QTY 0,000 (1) LEAD FREE #	
Origin →	(2) SPECIAL *Z0722005310C* ASSEMBLY:*** (DIFFUSION:***)	

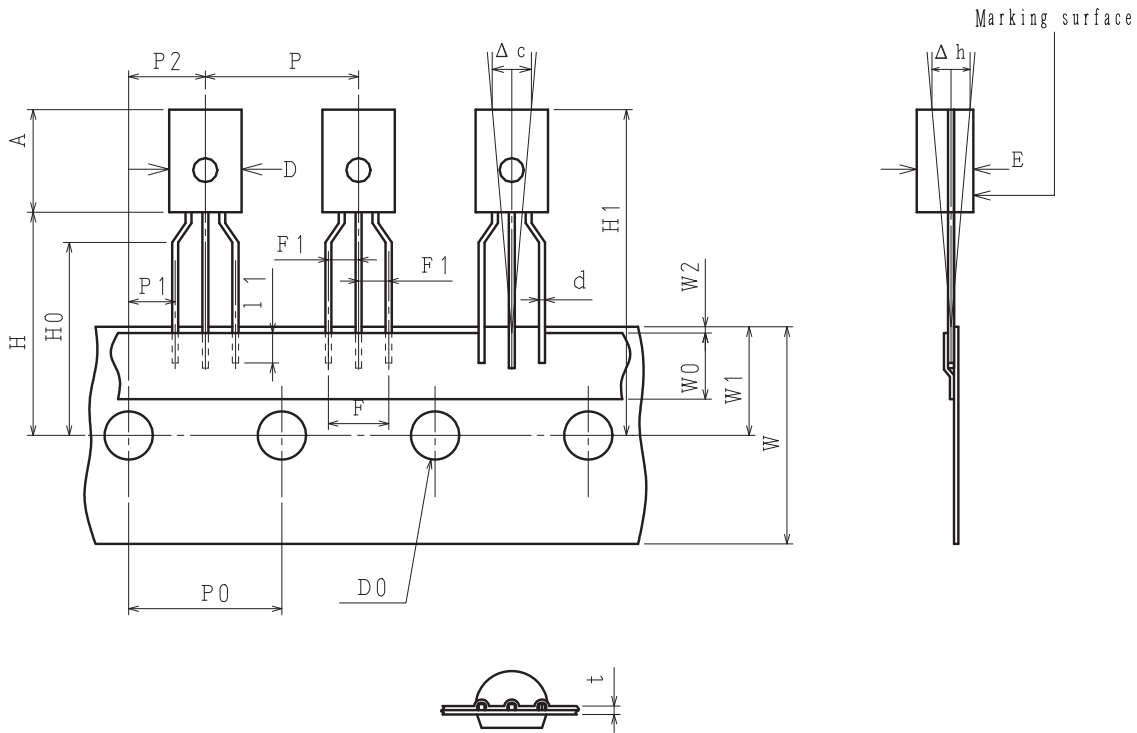
NOTE (1)

The LEAD FREE # description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping specifications

2-1. Carrier tape size



2-2. Taping size standard

unit:mm

Item	Symbol	Standard	Tolerance	Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.0	±0.2	Tape width	W	18.0	+1.0 -0.5
	E	4.7	±0.2	Adhesive tape	W0	6.0	±1.5
Work piece height	A	8.5	±0.2	Displacement of perforations	W1	9.0	±0.5
Lead wire diameter	d	0.5×0.5t	±0.1	Work piece bottom surface position	H	18.5	±1.0
Bonded lead wire	l1	2.5MIN		Insert stopper position	H0	16.0	±0.5
Pitch between products	P	12.7	±1.0	Work piece upper limit position	H1	27.0	±1.5
Pitch between perforations	P0	12.7	±0.2	Perforations diameter	D0	φ4.0	±0.2
Accumulation Pitch	P0×20	254.0	±1.0	Tape thickness	t	0.7	±0.2
Distance between lead wire	F	5.0	+0.8 -0.2	Product inclination	Δc	0	±1.5
Lead wire pitch distance	F1	2.5	+0.4 -0.1				
Product inclination	Δh	0	±2.0				
Displacement of perforations	P1	3.85	±0.3				
	P2	6.35	±0.3				
Displacement of tape	W2	0.5MAX					

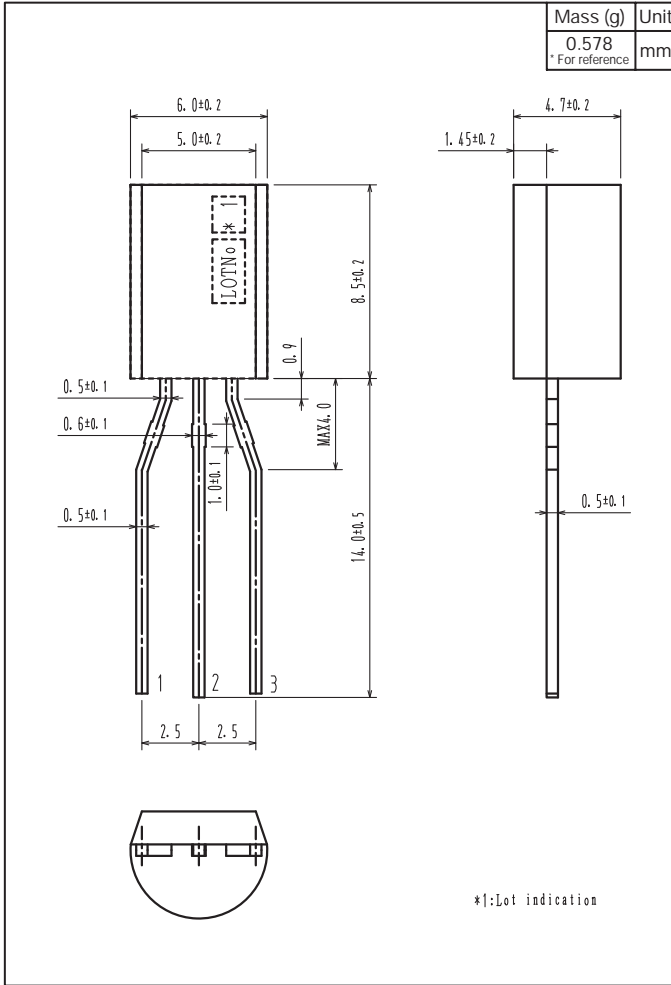
Measurement position is the bottom of the clinch

Not to be displaced to the outside of the board

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Outline Drawing

2SA2127-AE



Bag Packing Specification

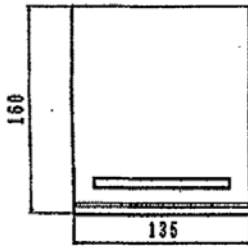
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1 . Packing condition

Storage package outline name	Maximum number of devices contained (pcs.)			Packing condition	
	Bags	Inner box	Devices contained	Outer box (A-1)	Outer box (A-2)
MP	500	B-1 Inner box dimensions : mm (external) 445×225×55	5,000	5 inner boxes contained (25,000) Outer box dimensions : mm (external) 470 × 250 × 300	3 inner boxes contained (15,000) Outer box dimensions : mm (external) 470 × 250 × 190

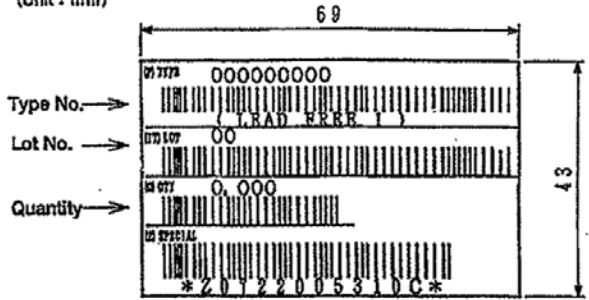
2. Bag dimensions

(Unit : mm)



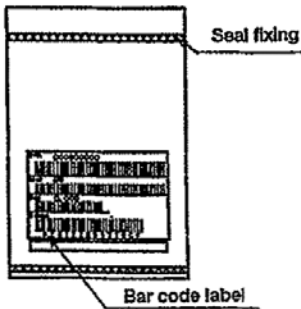
3. Bar code label

(Unit : mm)



*LEAD FREE 1 :
Lead-free External terminal surface
treatment product.

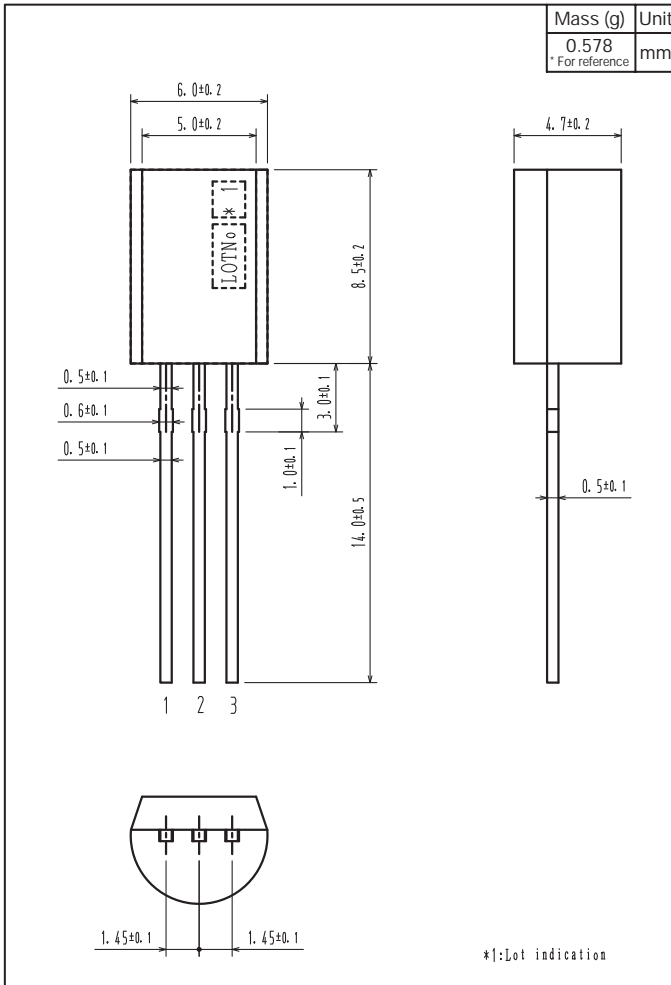
4. Housing devices in the bag



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Outline Drawing

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