

2SD1633

Silicon NPN triple diffusion planar type darlington

For voltage switching

■ Features

- High-speed switching
- Satisfactory linearity of forward current transfer ratio h_{FE}
- Full-pack package which can be installed to the heat sink with one screw

■ Absolute Maximum Ratings $T_C = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	100	V
Collector-emitter voltage (Base open)	V_{CEO}	100	V
Emitter-base voltage (Collector open)	V_{EBO}	7	V
Collector current	I_C	5	A
Peak collector current	I_{CP}	8	A
Base current	I_B	0.5	A
Collector power dissipation	P_C	30	W
		$T_a = 25^\circ\text{C}$	
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

■ Electrical Characteristics $T_C = 25^\circ\text{C} \pm 3^\circ\text{C}$

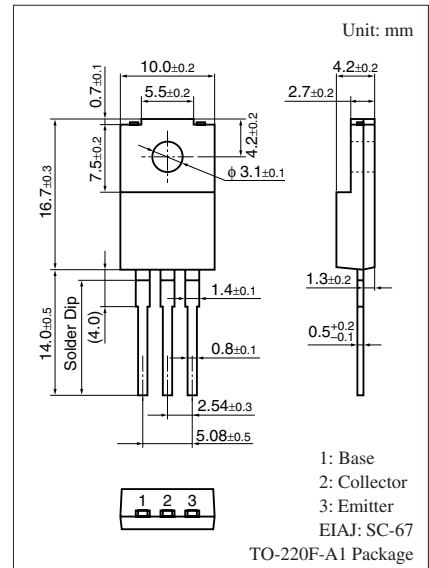
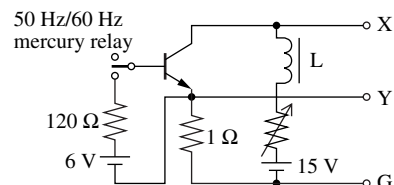
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-emitter sustaining voltage *2	$V_{CEO(SUS)}$	$I_C = 0.2\text{ A}$, $L = 25\text{ mH}$	100			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = 100\text{ V}$, $I_E = 0$			100	μA
Collector-emitter cut-off current (Base open)	I_{CEO}	$V_{CE} = 100\text{ V}$, $I_B = 0$			100	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = 7\text{ V}$, $I_C = 0$			5	mA
Forward current transfer ratio *1	h_{FE}	$V_{CE} = 3\text{ V}$, $I_C = 3\text{ A}$	1500		15000	—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = 3\text{ A}$, $I_B = 3\text{ mA}$			1.5	V
Base-emitter saturation voltage	$V_{BE(sat)}$	$I_C = 3\text{ A}$, $I_B = 3\text{ mA}$			2.0	V
Transition frequency	f_T	$V_{CE} = 10\text{ V}$, $I_C = 1\text{ A}$, $f = 1\text{ MHz}$		15		MHz
Turn-on time	t_{on}	$I_C = 3\text{ A}$, $I_{B1} = 3\text{ mA}$, $I_{B2} = -3\text{ mA}$			3	μs
Storage time	t_{stg}	$V_{CC} = 50\text{ V}$			5	μs
Fall time	t_f				3	μs

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

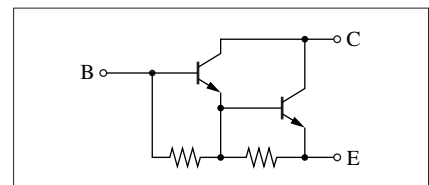
2. *1: Rank classification

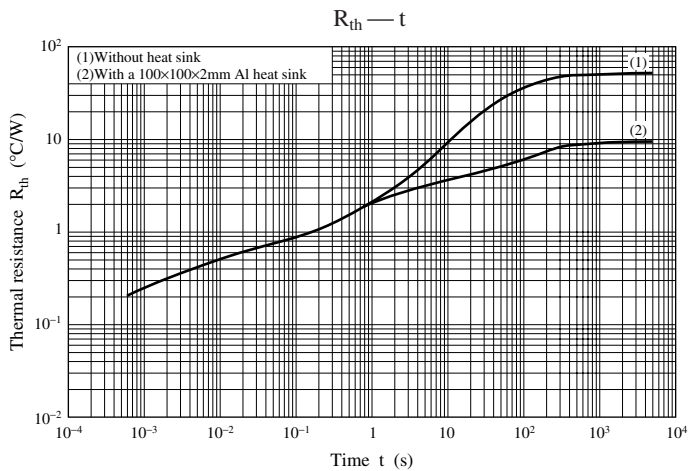
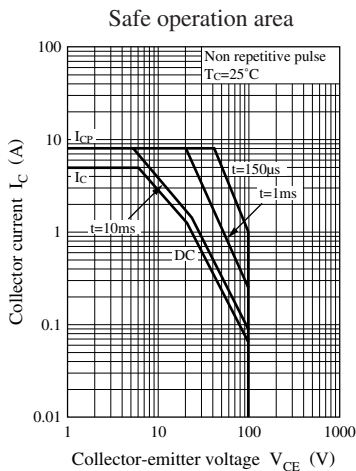
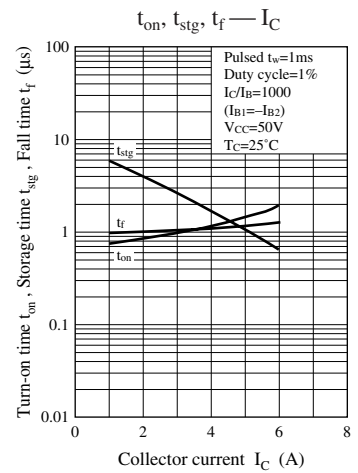
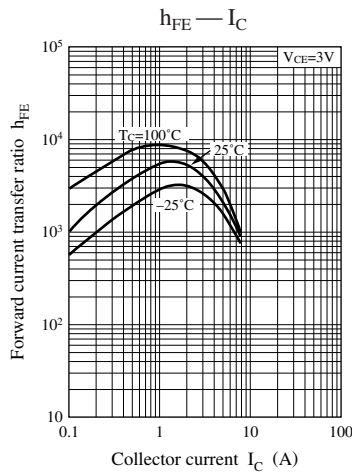
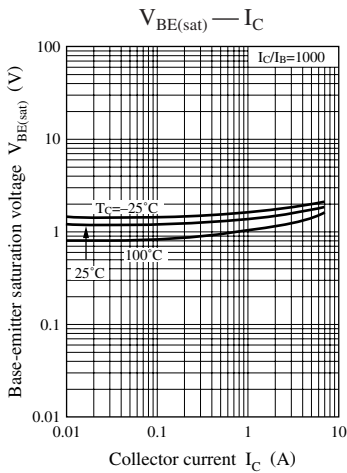
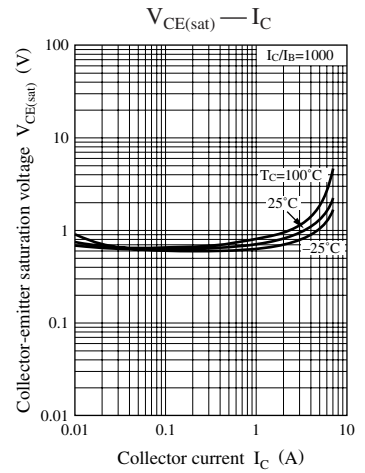
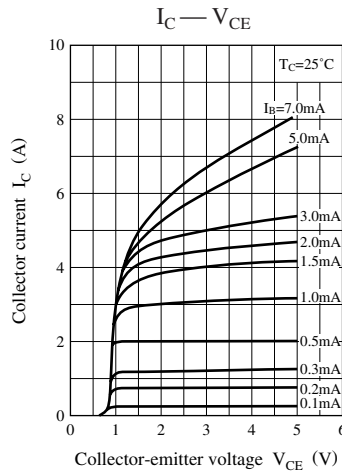
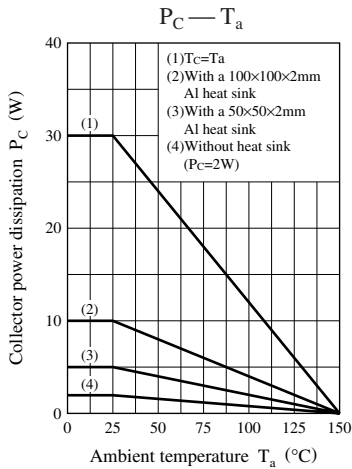
Rank	Q	P
h_{FE}	1500 to 6000	5000 to 15000

*2: $V_{CEO(SUS)}$ test circuit



Internal Connection





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