



2SJ665 — P-Channel Silicon MOSFET

General-Purpose Switching Device Applications

Features

- ON-resistance $R_{DS(on)} = 59m\Omega$ (typ.)
- Input capacitance $C_{iss} = 4200pF$ (typ.)
- 4V drive

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ C$

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		-100	V
Gate-to-Source Voltage	V_{GSS}		± 20	V
Drain Current (DC)	I_D		-27	A
Drain Current (Pulse)	I_{DP}	$PW \leq 10\mu s$, duty cycle $\leq 1\%$	-108	A
Allowable Power Dissipation	P_D	$T_c = 25^\circ C$	65	W
Channel Temperature	T_{ch}		150	$^\circ C$
Storage Temperature	T_{stg}		-55 to +150	$^\circ C$
Avalanche Energy (Single Pulse) *1	E_{AS}		48	mJ
Avalanche Current *2	I_{AV}		-27	A

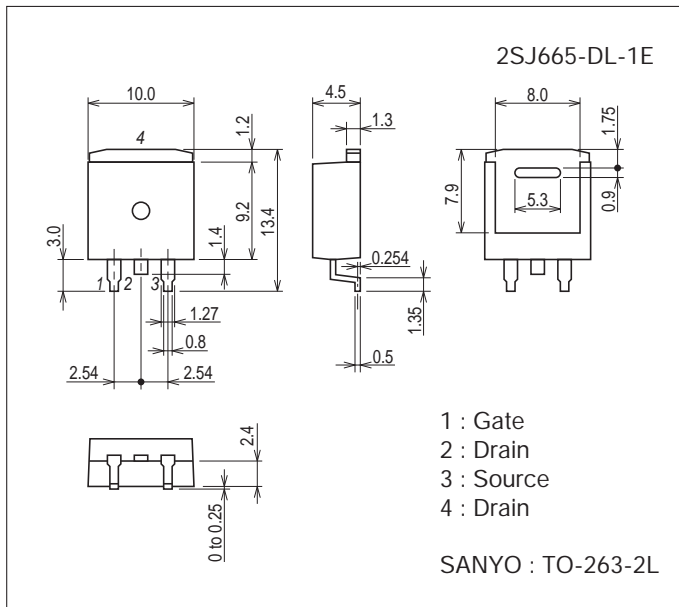
Note : *1 $V_{DD} = -30V$, $L = 100\mu H$, $I_{AV} = -27A$ (Fig.1)

*2 $L \leq 100\mu H$, single pulse

Package Dimensions

unit : mm (typ)

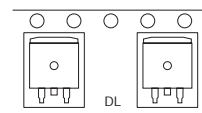
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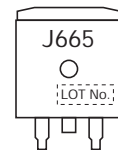
Product & Package Information

- Package : TO-263-2L
- JEITA, JEDEC : SC-83, TO-263
- Minimum Packing Quantity : 800 pcs./reel

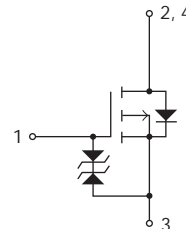
Packing Type: DL



Marking



Electrical Connection



2SJ665

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	V(BR)DSS	I _D =-1mA, V _{GS} =0V	-100			V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V			-1	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±10	μA
Cutoff Voltage	V _{GS(off)}	V _{DS} =-10V, I _D =-1mA	-1.2		-2.6	V
Forward Transfer Admittance	y _{fs}	V _{DS} =-10V, I _D =-14A	15	25		S
Static Drain-to-Source On-State Resistance	R _{DS(on)1}	I _D =-14A, V _{GS} =-10V		59	77	mΩ
	R _{DS(on)2}	I _D =-14A, V _{GS} =-4V		75	105	mΩ
Input Capacitance	C _{iss}	V _{DS} =-20V, f=1MHz		4200		pF
Output Capacitance	C _{oss}			280		pF
Reverse Transfer Capacitance	C _{rss}			220		pF
Turn-ON Delay Time	t _{d(on)}	See Fig.2		30		ns
Rise Time	t _r			150		ns
Turn-OFF Delay Time	t _{d(off)}			330		ns
Fall Time	t _f			135		ns
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-10V, I _D =-27A		74		nC
Gate-to-Source Charge	Q _{gs}			12.8		nC
Gate-to-Drain "Miller" Charge	Q _{gd}			14.7		nC
Diode Forward Voltage	V _{SD}		I _S =-27A, V _{GS} =0V		-0.98	-1.2

Fig.1 Avalanche Resistance Test Circuit

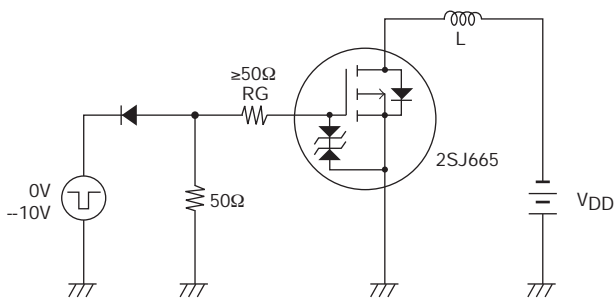
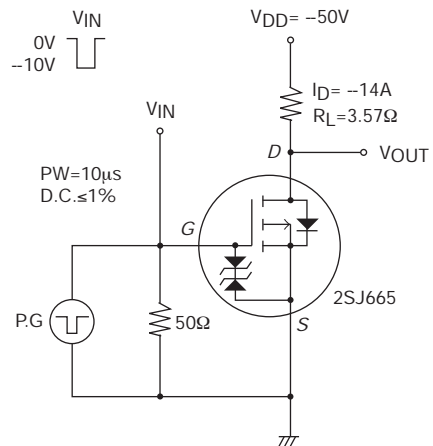
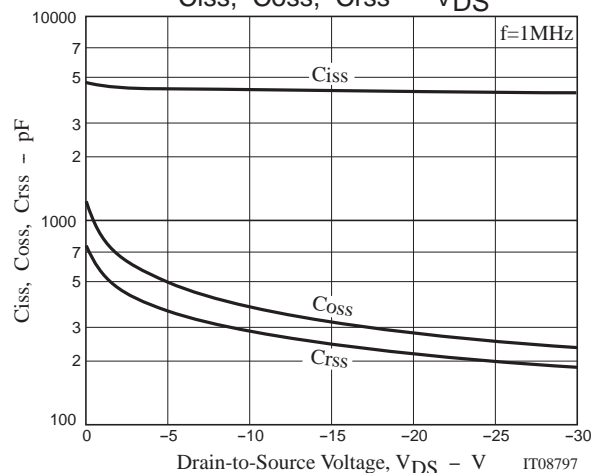
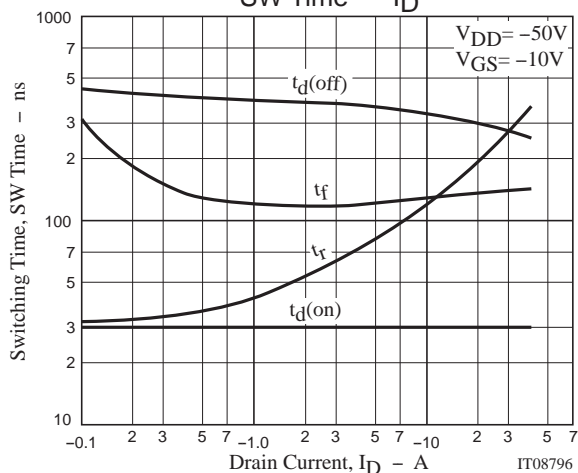
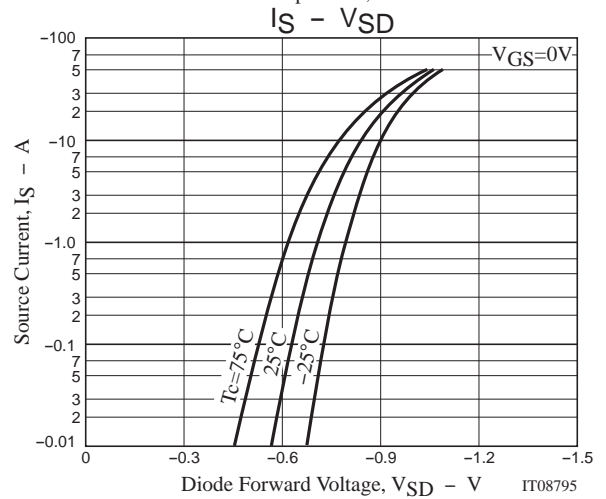
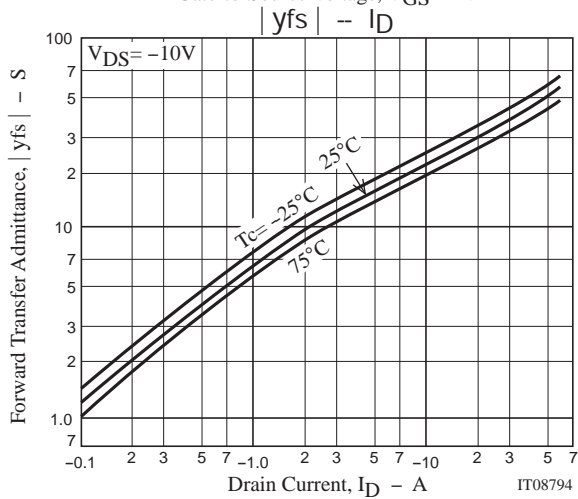
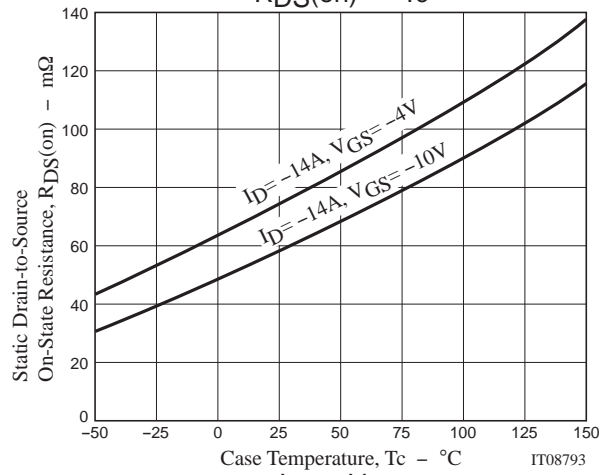
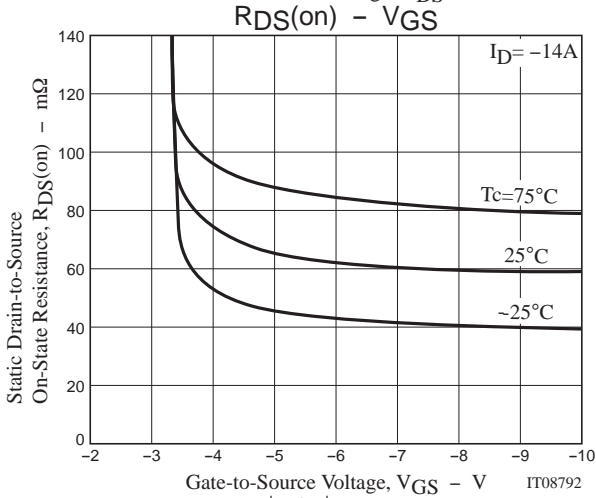
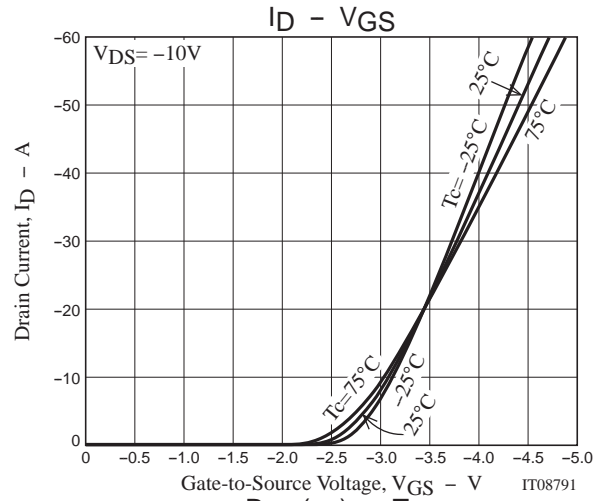
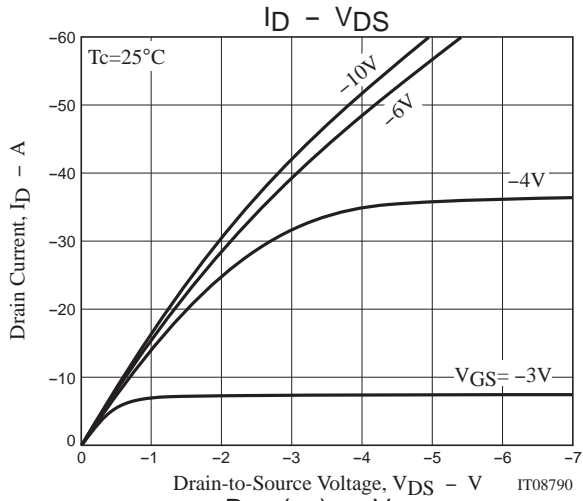


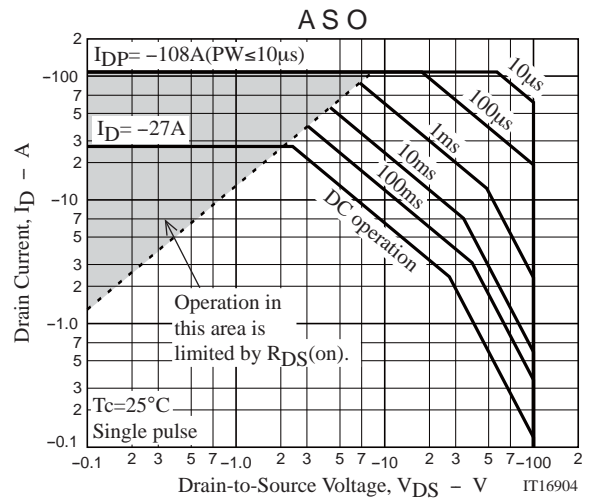
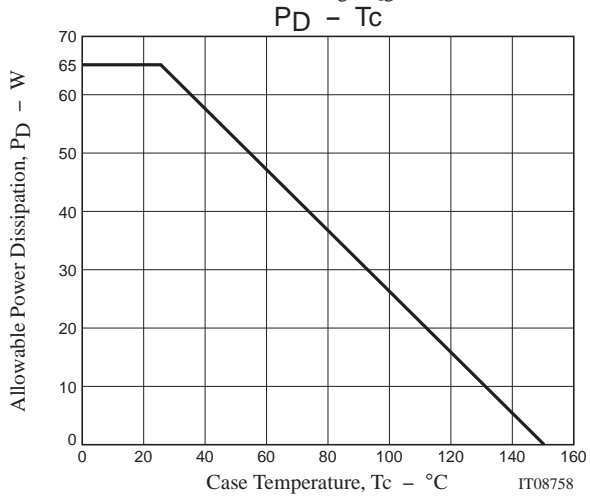
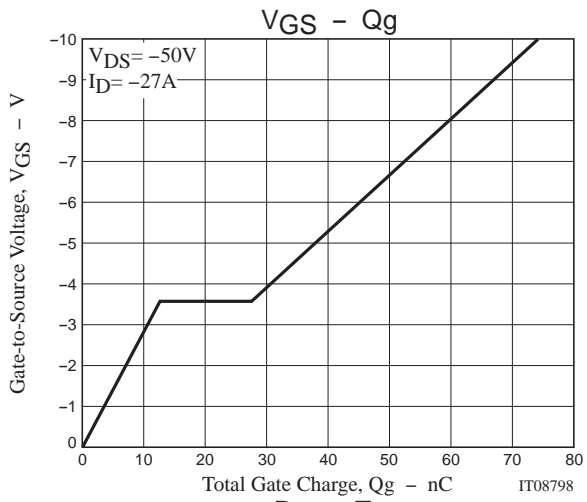
Fig.2 Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
2SJ665-DL-1E	TO-263-2L	800pcs./reel	Pb Free





Taping Specification

2SJ665-DL-1E

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)			Packing format	
	Reel	Inner box	Outer box	Inner BOX	Outer BOX
TO-263-2L	800	1600	6400	SPD-0V0011 2 reel contained Dimensions:mm (external) 351×340×68	SPD-0V0009 4 inner boxes contained Dimensions:mm (external) 390×370×318

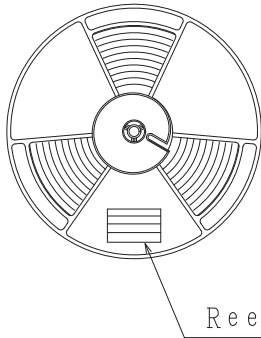
Reel label, Inner box label

Outer box label

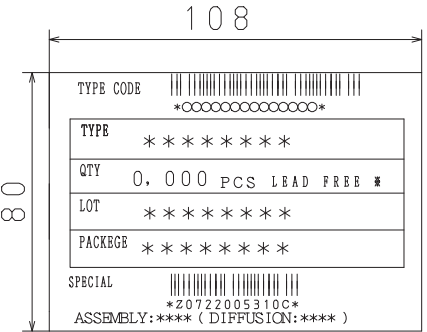
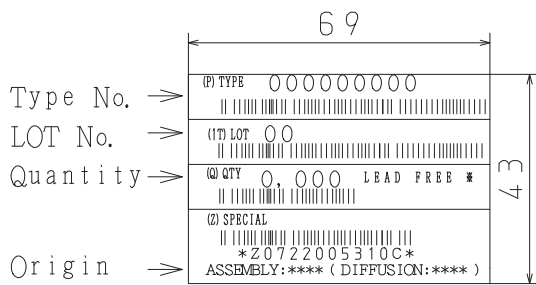
(unit:mm)

Packing method

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



Reel label



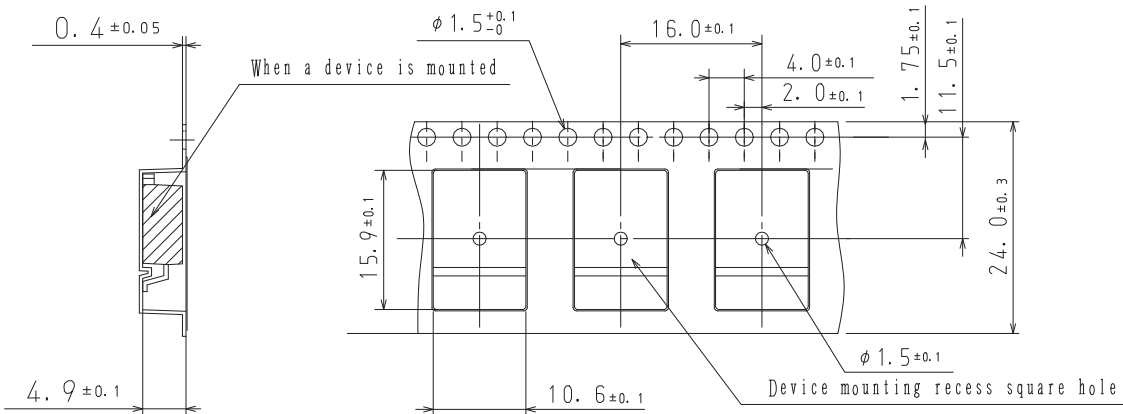
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

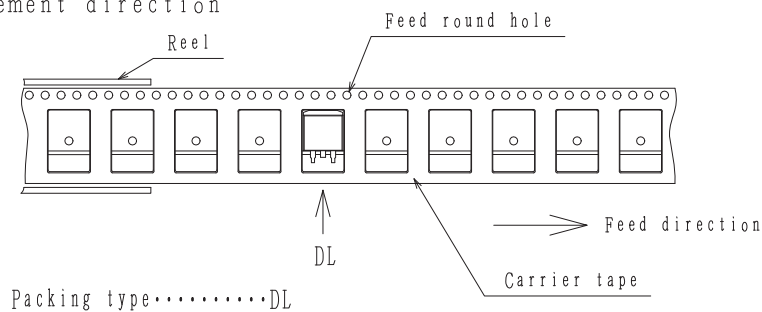
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

2. Taping configuration

2-1. Carrier tape size (unit:mm)



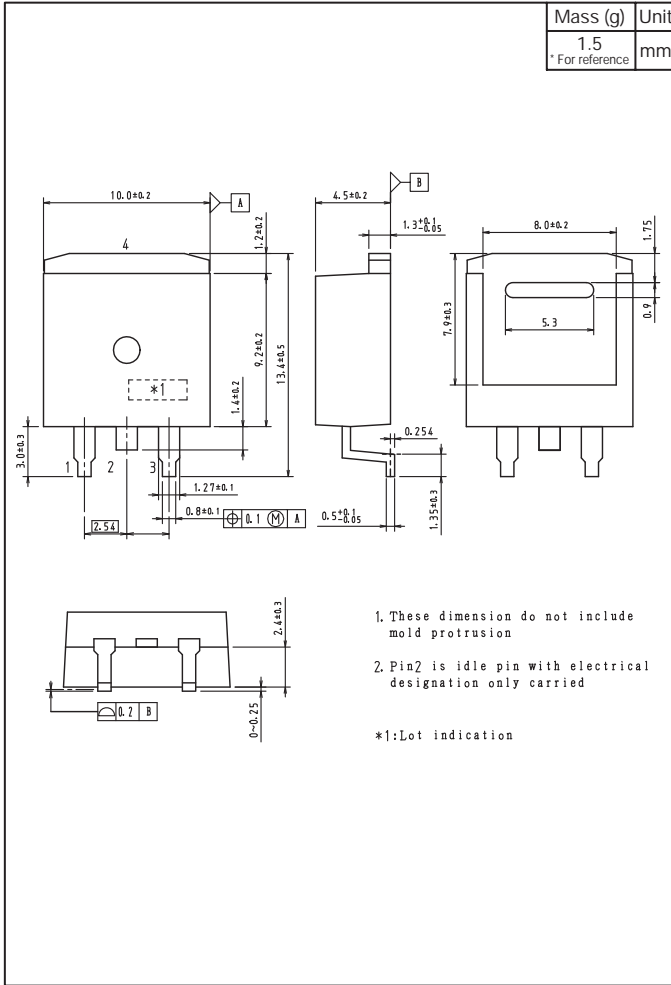
2-2. Device placement direction



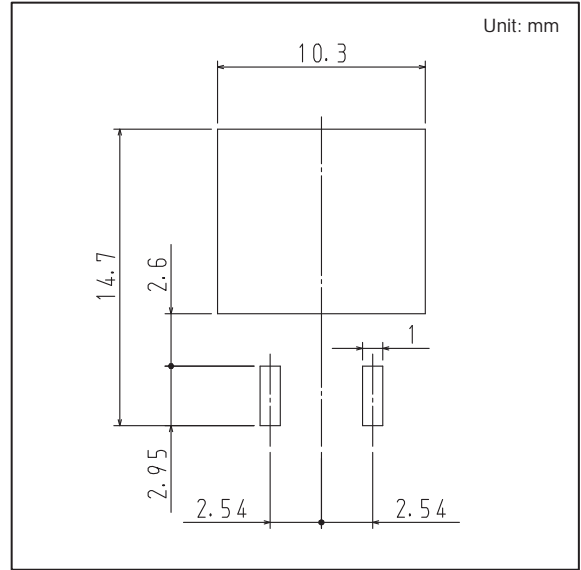
2SJ665

Outline Drawing

2SJ665-DL-1E



Land Pattern Example



Note on usage : Since the 2SJ665 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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