2SK1859

Silicon N-Channel MOS FET

HITACHI

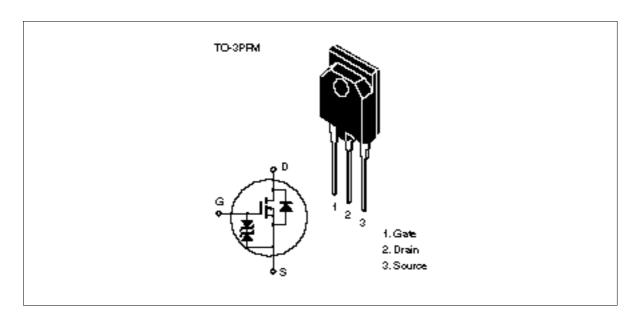
Application

High speed power switching

Features

- Low on-resistance
- High speed switching
- Low Drive Current
- No secondary breakdown
- Suitable for Switching regulator

Outline





2SK1859

Absolute Maximum Ratings $(Ta = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	900	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	6	A
Drain peak current	I _{D(pulse)} *1	15	A
Body to drain diode reverse drain current	I_{DR}	6	A
Channel dissipation	Pch*2	60	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes 1. PW 10 µs, duty cycle 1 %

2. Value at Tc = 25 °C

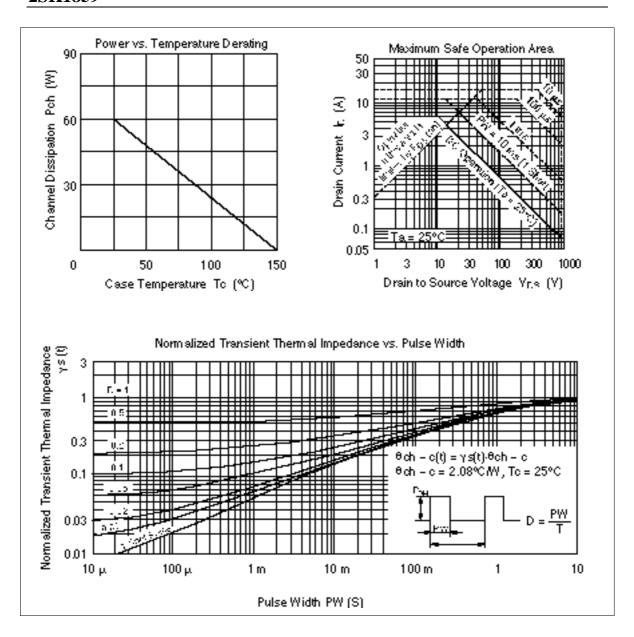
Electrical Characteristics ($Ta = 25^{\circ}C$)

Item	Symbol	Min	Тур	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	900	_	_	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	_	_	V	$I_G = \pm 100 \ \mu A, \ V_{DS} = 0$
Gate to source leak current	I _{GSS}	_	_	±10	μA	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}	_	_	250	μA	V _{DS} = 720 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	2.0	_	4.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	R _{DS(on)}	_	2.0	3.0		$I_D = 3 A$ $V_{GS} = 10 V^{*1}$
Forward transfer admittance	y _{fs}	2.3	3.7	_	S	$I_D = 3 A$ $V_{DS} = 20 V^{*1}$
Input capacitance	Ciss	_	980	_	pF	V _{DS} = 10 V
Output capacitance	Coss	_	400	_	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	195	_	pF	f = 1 MHz
Turn-on delay time	t _{d(on)}	_	20	_	ns	I _D = 3 A
Rise time	t _r	_	80	_	ns	V _{GS} = 10 V
Turn-off delay time	t _{d(off)}	_	125	_	ns	$R_L = 10$
Fall time	t _f	_	100	_	ns	
Body to drain diode forward voltage	V_{DF}	_	0.9	_	V	$I_F = 6 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	t _{rr}		1000	_	ns	IF = 6 A, V _{GS} = 0, di _F / dt = 100 A / μs

Note 1. Pulse Test

See characteristic curves of 2SK1341

2SK1859



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