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MOS FIELD EFFECT POWER TRANSISTOR  
**2SK2135**

SWITCHING  
 N-CHANNEL POWER MOS FET  
 INDUSTRIAL USE

**DESCRIPTION**

The 2SK2135 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

**FEATURES**

- Low On-state Resistance  
 $R_{DS(on)} = 0.18 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1100 \text{ pF TYP.}$
- High Avalanche Capability Ratings

**QUALITY GRADE**

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

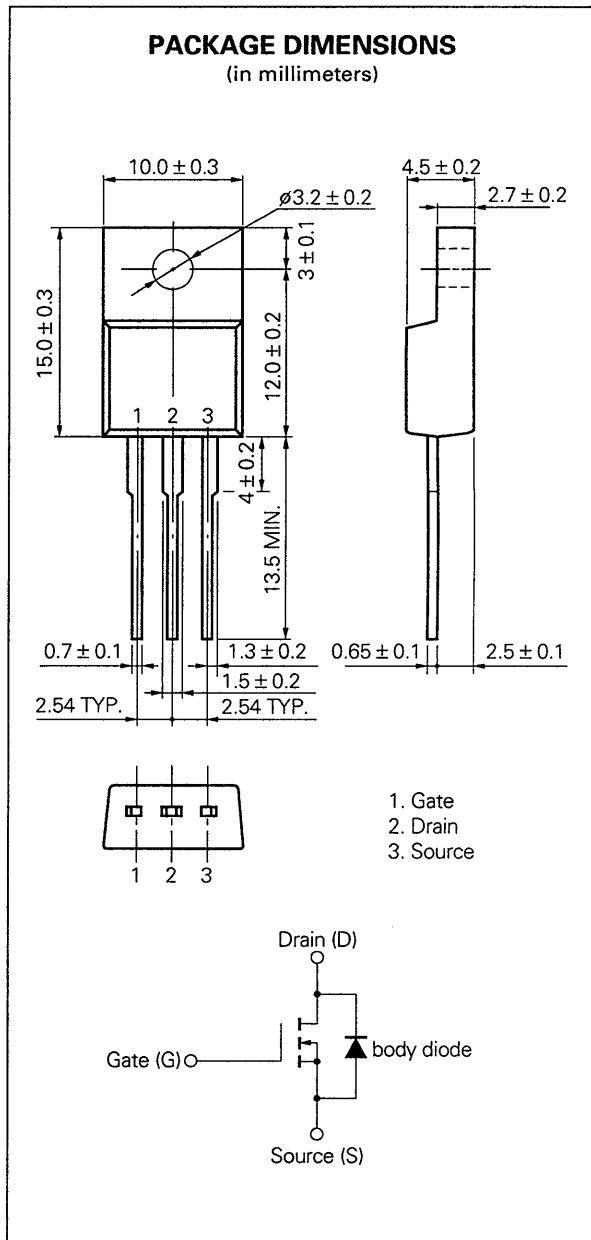
**ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)**

Drain to Source Voltage	$V_{DSS}$	200	V
Gate to Source Voltage	$V_{GSS}$	±30	V
Drain Current (DC)	$I_{D(DC)}$	±14	A
Drain Current (pulse)	$I_{D(pulse)^*}$	±56	A
Single Avalanche Current	$I_{AS}^{**}$	14	A
Single Avalanche Energy	$E_{AS}^{**}$	392	mJ
Total Power Dissipation (Tc = 25 °C)	$P_{T1}$	35	W
Total Power Dissipation (Ta = 25 °C)	$P_{T2}$	2.0	W
Storage Temperature	$T_{stg}$	-55 to +150	°C
Channel Temperature	$T_{ch}$	150	°C

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$

\*\* Starting  $T_{ch} = 25 \text{ °C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

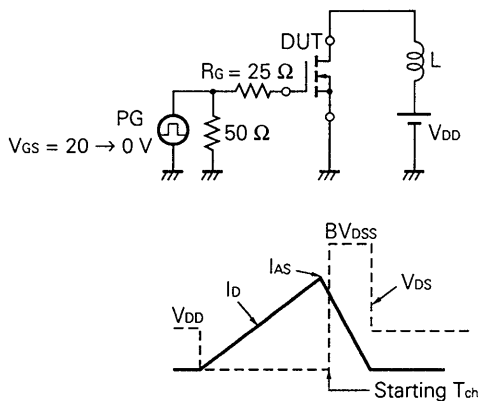
**PACKAGE DIMENSIONS**  
 (in millimeters)



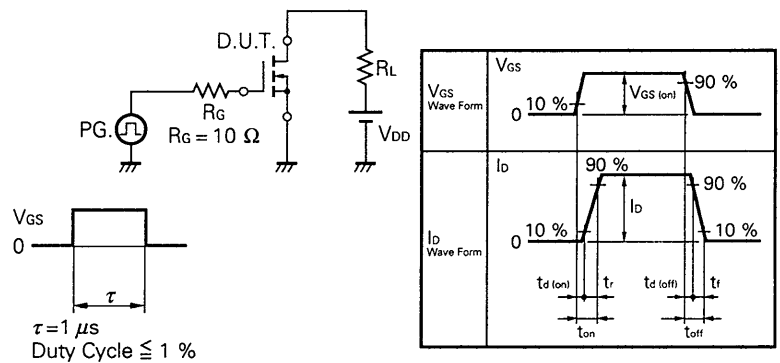
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>			0.18	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.0		4.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	4.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 100		pF	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 f = 1 MHz
Output Capacitance	C <sub>oss</sub>		540		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>		190		pF	
Turn-On Delay Time	t <sub>d(ton)</sub>		20		ns	V <sub>GS</sub> = 10 V V <sub>DD</sub> = 100 V I <sub>D</sub> = 7 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 14.3 Ω
Rise Time	t <sub>r</sub>		50		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		65		ns	
Fall Time	t <sub>f</sub>		25		ns	
Total Gate Charge	Q <sub>G</sub>		30		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 14 A V <sub>DD</sub> = 160 V
Gate to Source Charge	Q <sub>GS</sub>		7.0		nC	
Gate to Drain Charge	Q <sub>GD</sub>		15		nC	
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		170		ns	I <sub>F</sub> = 14 A
Reverse Recovery Charge	Q <sub>rr</sub>		0.6		μC	di/dt = 50 A/μs

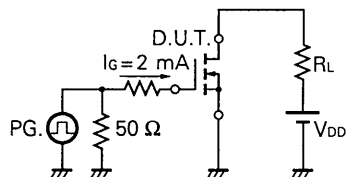
**Test Circuit 1 : Avalanche Capability**



**Test Circuit 2 : Switching Time**

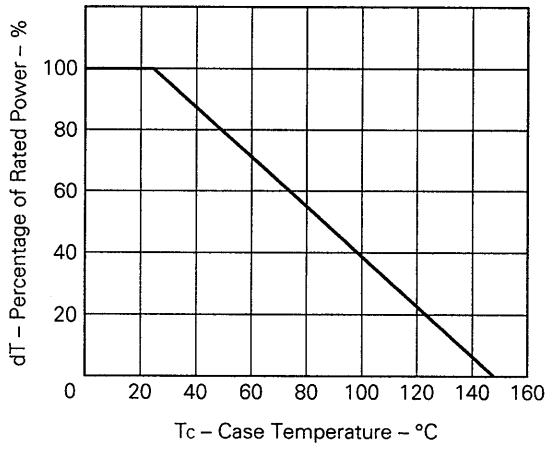


**Test Circuit 3 : Gate Charge**

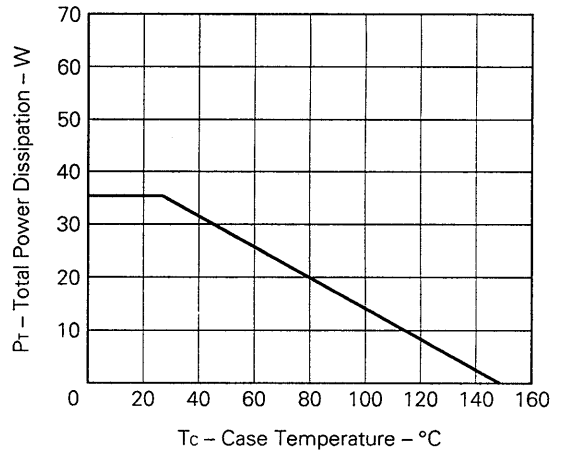


TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )

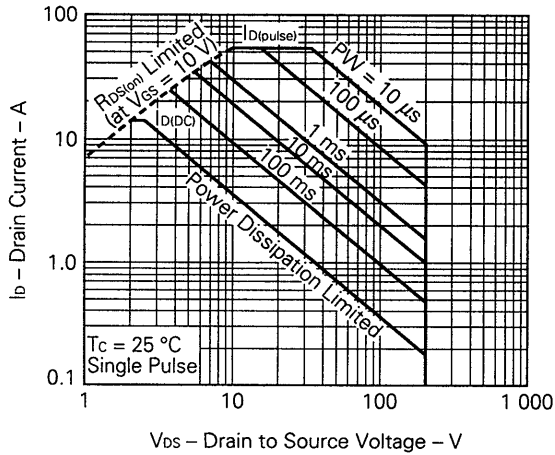
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



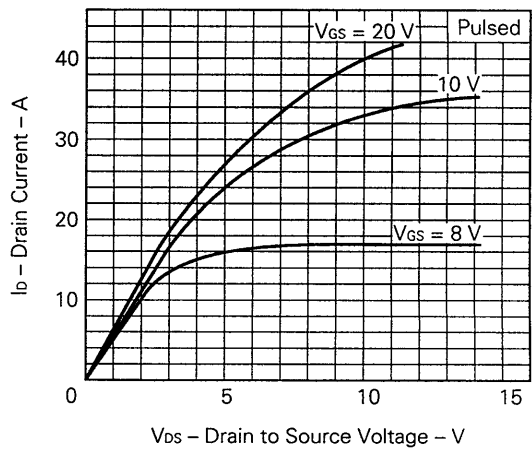
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



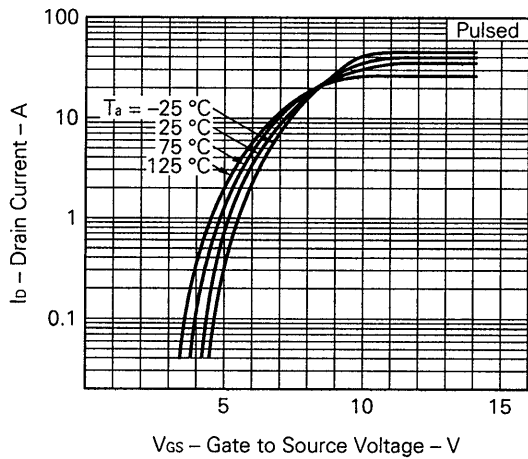
FORWARD BIAS SAFE OPERATING AREA

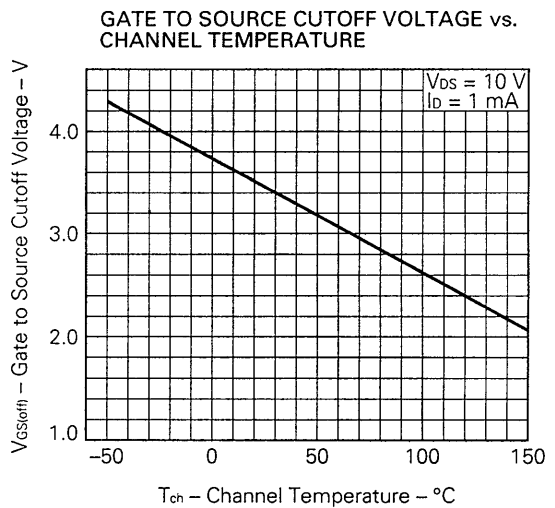
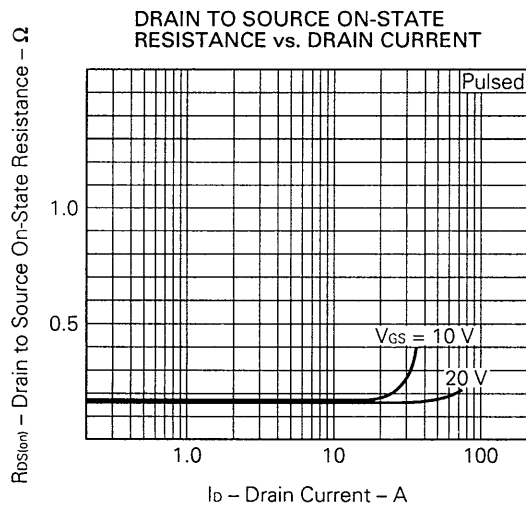
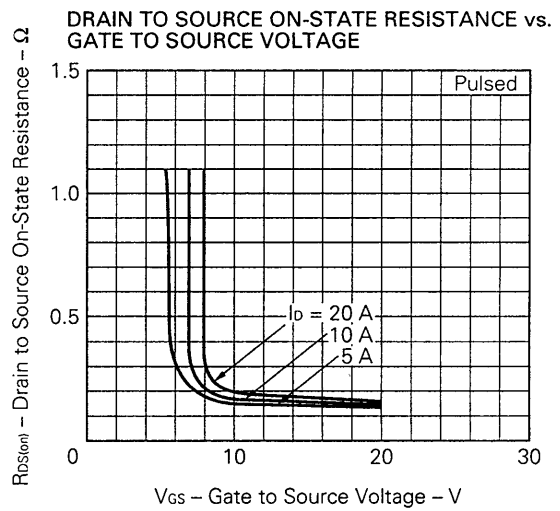
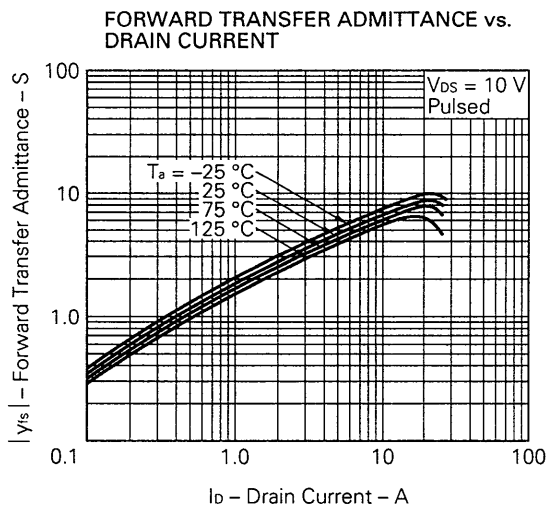
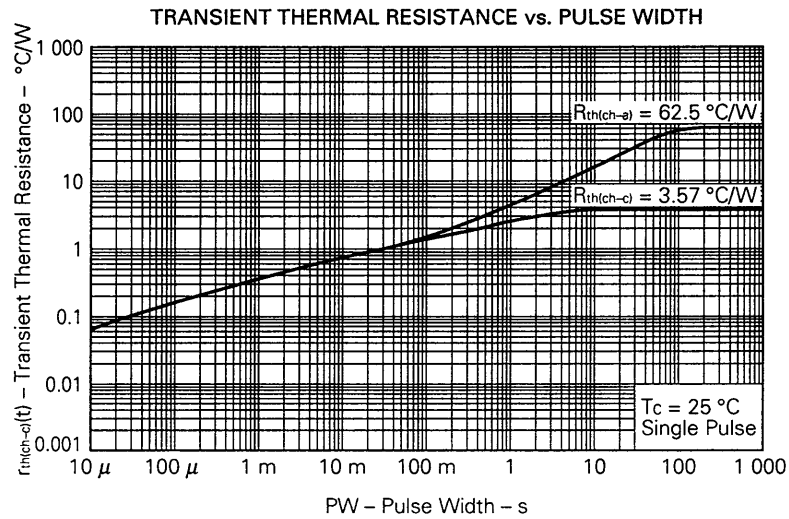


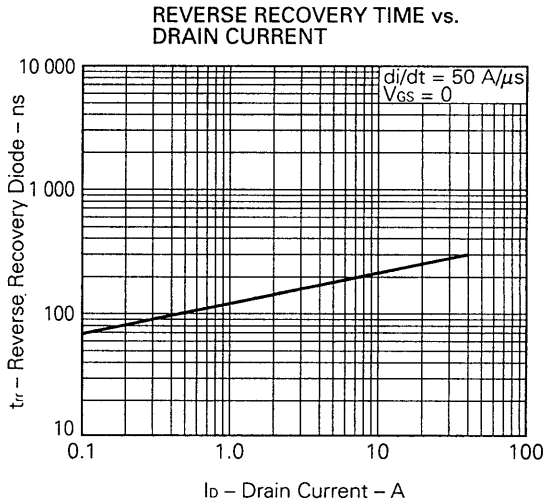
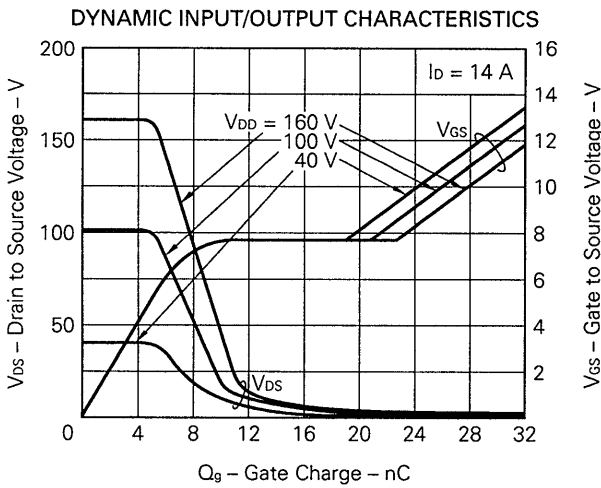
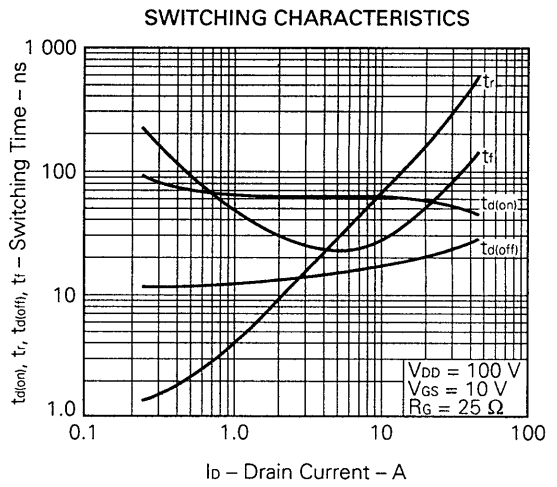
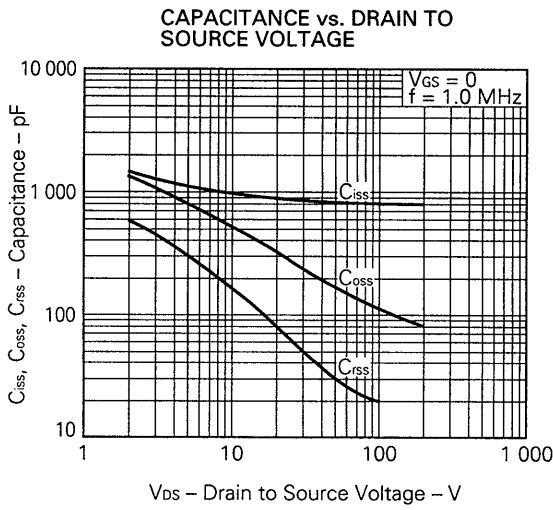
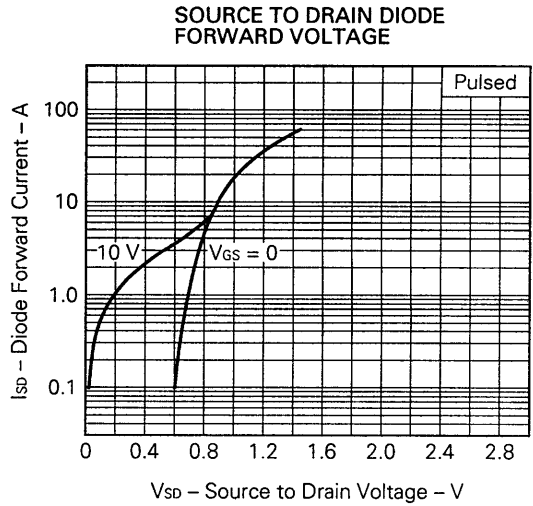
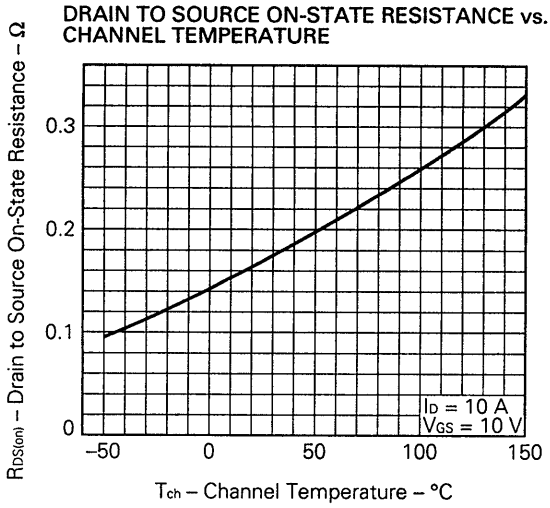
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

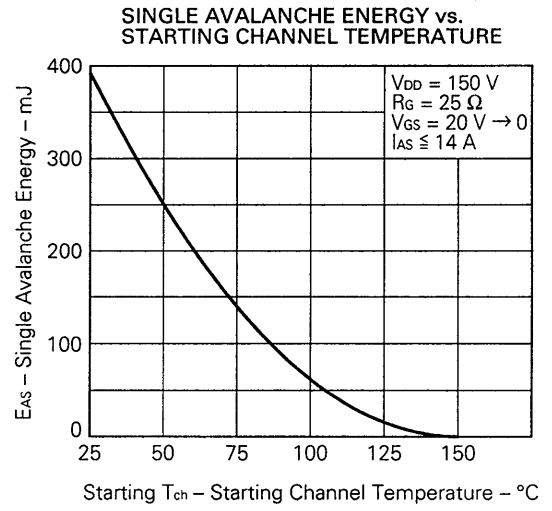
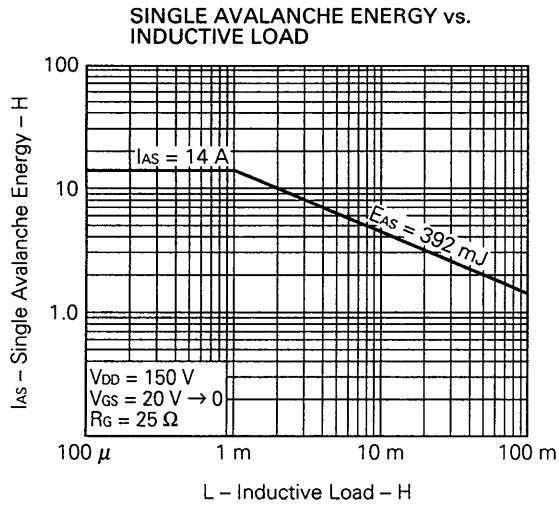


SOURCE TO DRAIN DIODE FORWARD VOLTAGE









[MEMO]



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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