

MOS FIELD EFFECT TRANSISTOR **2SK2511**

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

V

V

А

А

W W

°C °C

DESCRIPTION

The 2SK2511 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-Resistance RDS (on)1 = 27 m Ω (VGS = 10 V, ID = 20 A) RDS (on)2 = 40 m Ω (VGS = 4 V, ID = 20 A)
- Low C_{iss} C_{iss} = 1 210 pF TYP.
- Built-in G-S Protection Diode

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	60
Gate to Source Voltage	Vgss	±20
Drain Current (DC)	D (DC)	±40
Drain Current (pulse)*	D (pulse)	±160
Total Power Dissipation (T _c = 25 $^{\circ}$ C)	Ρ τ1	80
Total Power Dissipation (T _A = 25 $^{\circ}$ C)	Рт2	3.0
Channel Temperature	Tch	150
Storage Temperature	Tstg -5	5 to +150
* PW \leq 10 μ s, Duty Cycle \leq 1 %		

(in millimeter) 4.7 MAX. 15.7 MAX 3.2±0.2 0 1.5 20.0±0 6.0 540. 19 MIN. 3.0±0.2 0.6±0.1 2.2±0.2 1.0±0.2 2.8±0.1 5.45 5.45 1. Gate 2. Drain /••••/ 3. Source 4. Fin (Drain) **MP-88** Drain Body 👗 Diode Gate Gate Protection Diode Source

PACKAGE DIMENSIONS

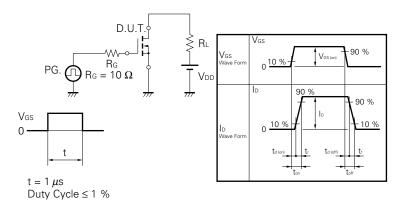
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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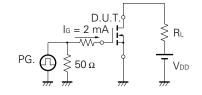
ELECTRICAL CHARACTERISTICS (TA = 25 $^{\circ}$ C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	RDS (on)1		22	27	mΩ	Vgs = 10 V, Id = 20 A
Drain to Source On-Resistance	RDS (on)2		32	40	mΩ	Vgs = 4 V, Id = 20 A
Gate to Source Cutoff Voltage	VGS (off)	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	10			S	$V_{DS} = 10 V, I_{D} = 20 A$
Drain Leakage Current	IDSS			10	μA	Vds = Vdss, Vgs = 0
Gate to Source Leakage Current	Igss			±10	μΑ	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0$
Input Capacitance	Ciss		1 210		pF	$V_{DS} = 10 V$
Output Capacitance	Coss		610		pF	V _{GS} = 0
Reverse Transfer Capacitance	Crss		270		pF	f = 1 MHz
Turn-On Delay Time	td (on)		32		ns	ID = 20 A
Rise Time	tr		300		ns	Vgs = 10 V
Turn-Off Delay Time	td (off)		160		ns	Vdd = 30 V
Fall Time	tr		220		ns	$R_G = 10 \Omega$
Total Gate Charge	Q _G		50		nC	$I_D = 40 A$
Gate to Source Charge	Qgs		4.5		nC	Vdd = 48 V
Gate to Drain Charge	Qgd		21		nC	Vgs = 10 V
Body Diode Forward Voltage	VF (S-D)		1.0		V	$I_F = 40 \text{ A}, \text{ V}_{GS} = 0$
Reverse Recovery Time	trr		70		ns	$I_F = 40 \text{ A}, \text{ V}_{GS} = 0$
Reverse Recovery Charge	Qrr		140		nC	di/dt = 100 A/µs

Test Circuit 1 Switching Time

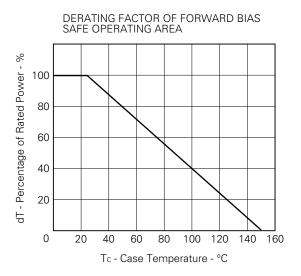


Test Circuit 2 Gate Charge

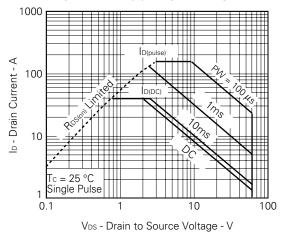


The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

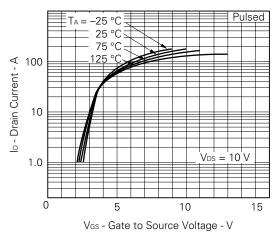


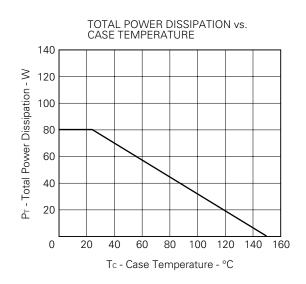




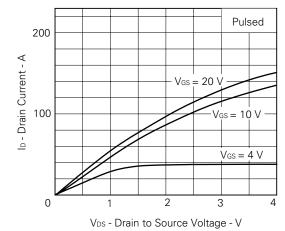


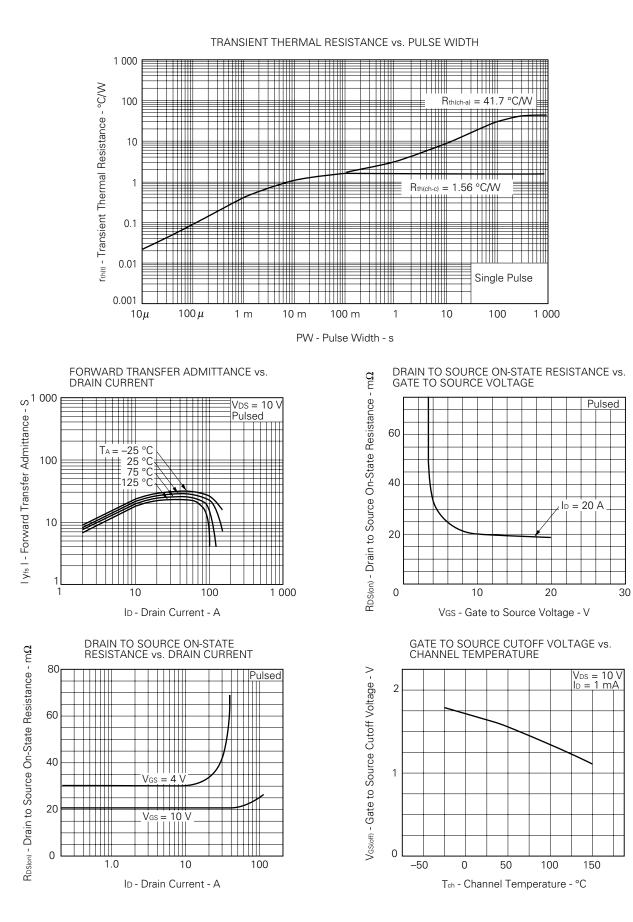
FORWARD TRANSFER CHARACTERISTICS

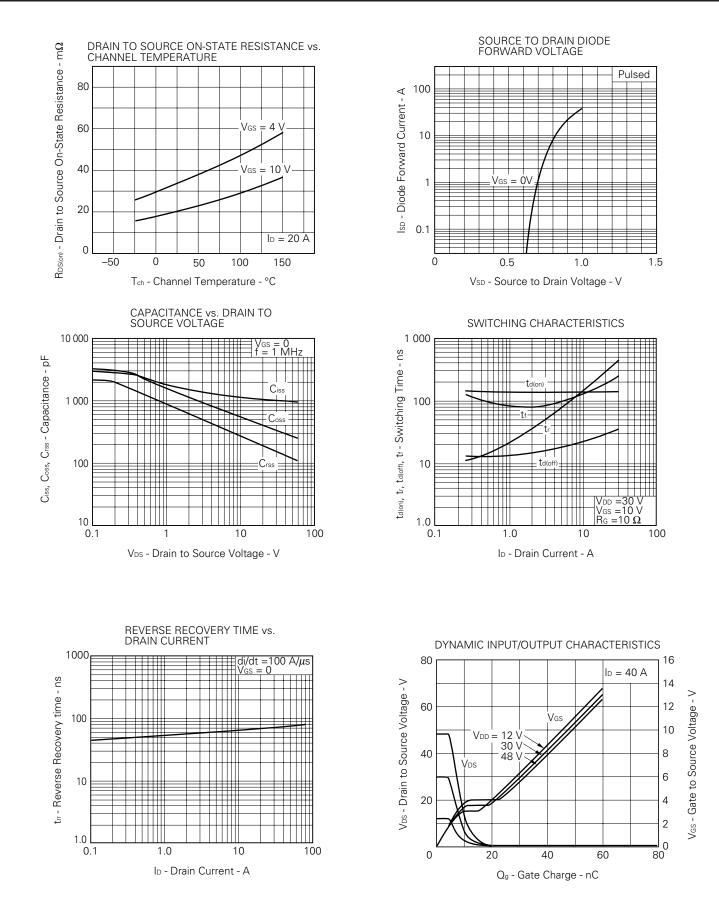












REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

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