

# MOS FIELD EFFECT TRANSISTOR **2SK3108**

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

## DESCRIPTION

The 2SK3108 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

## **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SK3108	Isolated TO-220

### FEATURES

•Gate voltage rating ±30 V

Low on-state resistance

 $R_{DS(on)} = 0.4 \Omega MAX. (V_{GS} = 10 V, I_D = 4.0 A)$ 

- Low input capacitance
- $C_{\text{iss}}$  = 400 pF TYP. (V\_{\text{DS}} = 10 V, V\_{\text{GS}} = 0 V)
- Avalanche capability rated
- •Built-in gate protection diode
- Isolated TO-220 package

## ABSOLUTE MAXIMUM RATING ( $T_A = 25^{\circ}C$ )

Drain to Source Voltage (V <sub>GS</sub> = $0$ V)	Vdss	200	V
Gate to Source Voltage ( $V_{DS} = 0 V$ )	Vgss	±30	V
Drain Current(DC) (Tc = 25°C)	D(DC)	±8.0	А
Drain Current(pulse) Note1	D(pulse)	±24	А
Total Power Dissipation (T <sub>A</sub> = 25°C)	Ρτ1	2.0	W
Total Power Dissipation (Tc = 25°C)	P <sub>T2</sub>	25	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	8.0	А
Single Avalanche Energy Note2	Eas	51	mJ

**Note1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

**2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 100 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20 V $\rightarrow$ 0 V

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90%

90%

tf

tof

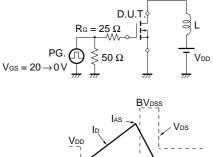
td(off)

-10%

## ELECTRICAL CHARACTERISTICS (TA = 25°C)

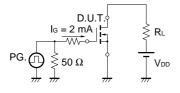
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	loss	Vds = 200 V, Vgs = 0 V			100	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 30 \text{ V}, \text{V}_{DS} = 0 \text{ V}$			±10	μA
Gate to Source Cut-off Voltage	VGS(off)	Vds = 10 V, Id = 1 mA	2.5		4.5	V
Forward Transfer Admittance	y <sub>fs</sub>	VDS = 10 V, ID = 4.0 A	1.5			S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, Id = 4.0 A		0.32	0.4	Ω
Input Capacitance	Ciss	VDS = 10 V		400		pF
Output Capacitance	Coss	Vgs = 0 V		110		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		55		pF
Turn-on Delay Time	td(on)	VDD = 100 V, ID = 4.0 A		12		ns
Rise Time	tr	VGS(on) = 10 V		25		ns
Turn-off Delay Time	td(off)	Rg = 10 Ω		40		ns
Fall Time	tr			20		ns
Total Gate Charge	QG	Vdd = 160 V		18		nC
Gate to Source Charge	QGS	Vgs = 10 V		3.5		nC
Gate to Drain Charge	Qgd	ID = 8.0 A		10		nC
Diode Forward Voltage	VF(S-D)	IF = 8.0 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 8.0 A, VGS = 0 V		250		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/ $\mu$ s		1.0		μC

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

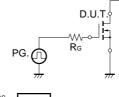


-Starting Tch

## **TEST CIRCUIT 3 GATE CHARGE**

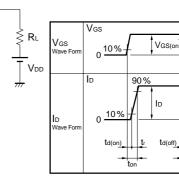


## **TEST CIRCUIT 2 SWITCHING TIME**

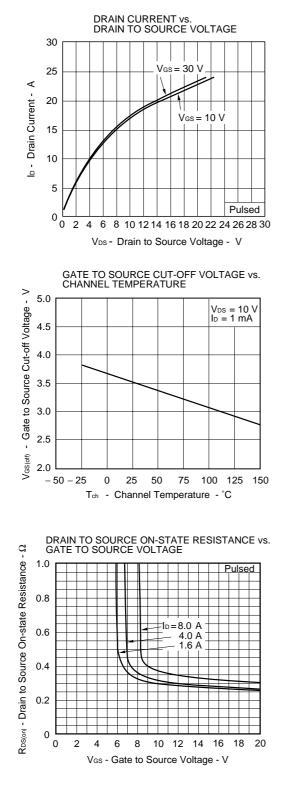


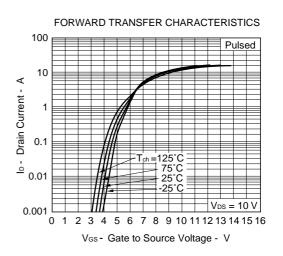


 $\begin{array}{l} \tau = 1 \; \mu s \\ \text{Duty Cycle} \leq 1 \; \% \end{array}$ 

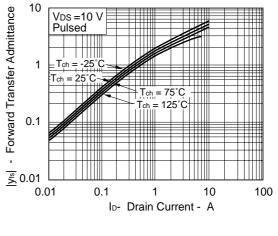


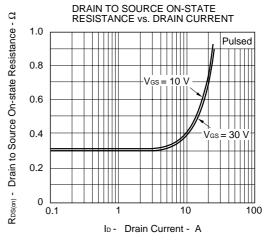
## ★ TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



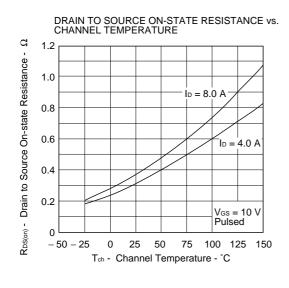


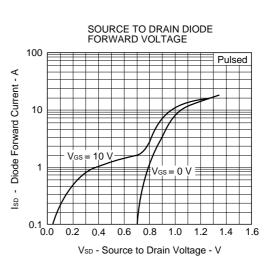
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



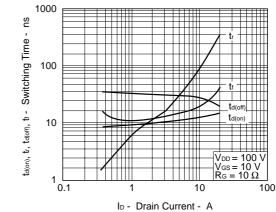


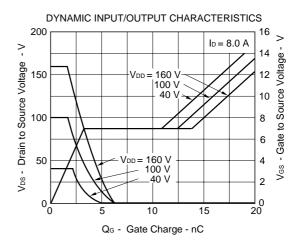
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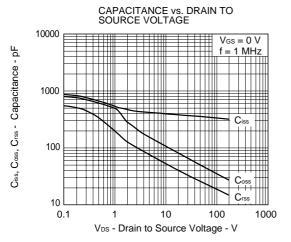


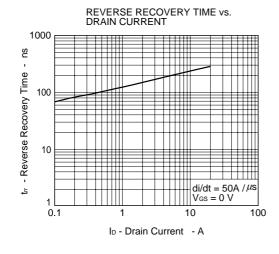


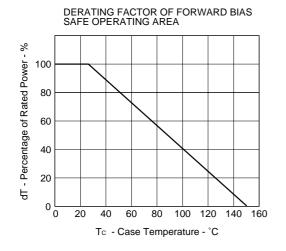
SWITCHING CHARACTERISTICS

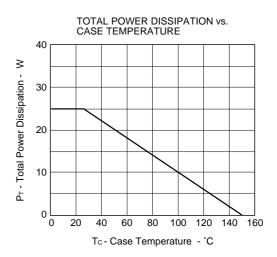




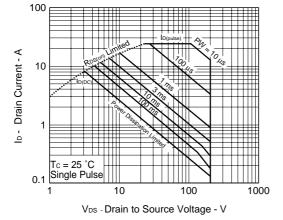






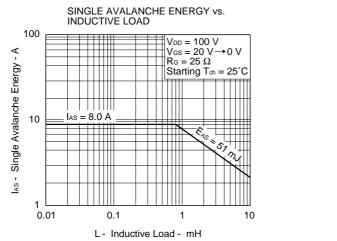


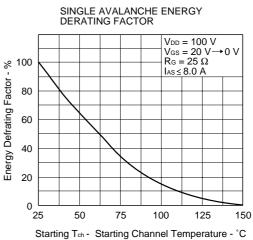
 $\star$ FORWARD BIAS SAFE OPERATING AREA



1 000 rh(t) - Transient Thermal Resistance - °C/W Ш  $R_{th(ch-A)} = 62.5^{\circ}C/W$ 100 10  $R_{th(ch-C)} = 5^{\circ}C/W$ / +++ 1 0.1 Single Pulse 0.01 100*µ* 10*µ* 1 m 10 m 100 m 1 10 100 1 000 PW - Pulse Width - s

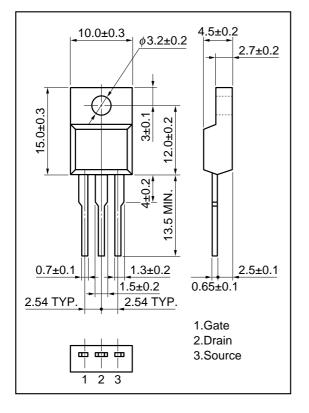
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



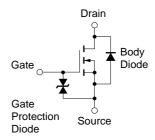


## PACKAGE DRAWING(Unit : mm)

Isolated TO-220 (MP-45F)



**EQUIVALENT CIRCUIT** 



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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