

# MOS FIELD EFFECT TRANSISTOR 2SK3112

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK3112 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter, actuator driver.

#### **ORDERING INFORMATION**

Part number	Package			
2SK3112	TO-220AB			
2SK3112-S	TO-262			
2SK3112-ZJ	TO-263			

#### FEATURES

•Gate voltage rating  $\pm 30 \text{ V}$ •Low on-state resistance RDS(on) = 110 m $\Omega$ (MAX.) @VGS = 10 V, ID = 13 A •Low input capacitance Ciss = 1500 pF TYP. @VDS = 10 V, VGS = 0 V •Built-in gate protection diode

## ABSOLUTE MAXIMUM RATING (T<sub>A</sub> = $25^{\circ}$ C)

Drain to source voltage (Vgs = 0 V)	VDSS	200	V
Gate to source voltage ( $V_{DS} = 0 V$ )	Vgss	±30	V
Drain current(DC) (Tc = 25°C)	D(DC)	±25	А
Drain current(pulse) Note	D(pulse)	±75	А
Total power dissipation (T <sub>A</sub> = $25^{\circ}$ C)	P <sub>T1</sub>	1.5	W
Total power dissipation (Tc = 25°C)	Pt2	70	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note  $PW \le 10 \ \mu s$ , Duty Cycle  $\le 1\%$ 

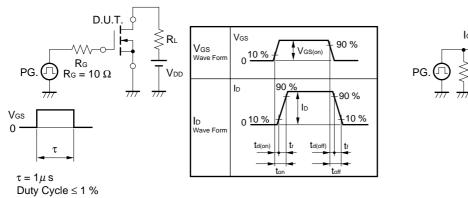
The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

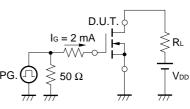
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#### ELECTRICAL CHARACTERISTICS(TA = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain leakage current	IDSS	Vds = 200 V, Vgs = 0 V			100	μA
Gate leakage current	lgss	$V_{GS} = \pm 30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate cut-off voltage	VGS(off)	VDS = 10 V, ID = 1 mA	2.5		4.5	V
Forward transfer admittance	y <sub>fs</sub>	Vds = 10 V, Id = 13 A	8.0			S
Drain to source on-State resistance	RDS(on)	Vgs = 10 V, Id = 13 A		80	110	mΩ
Input capacitance	Ciss	VDS = 10 V		1500		pF
Output capacitance	Coss	Vgs = 0 V		450		pF
Reverse transfer capacitance	Crss	f = 1 MHz		200		pF
Turn-on delay time	<b>t</b> d(on)	Vdd = 100 V, Id = 13 A		50		ns
Rise time	tr	VGS(on) = 10 V		120		ns
Turn-off delay time	td(off)	Rg = 10 Ω		150		ns
Fall time	tr			80		ns
Total gate charge	QG	Vdd = 160 V		60		nC
Gate to source charge	QGS	Vgs = 10 V		8		nC
Gate to drain charge	Qgd	ID = 25 A		30		nC
Diode forward voltage	VF(S-D)	IF = 25 A, VGS = 0 V		1.0		V
Reverse recovery time	Trr	IF = 25 A, VGS = 0 V		1.5		μs
Reverse recovery charge	Qrr	di/dt = 50 A/ <i>µ</i> s		4.5		μC



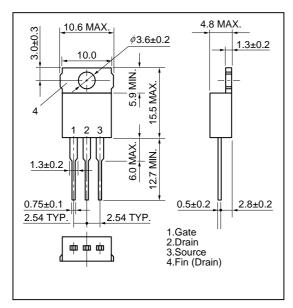


Test circuit 1 Switching time

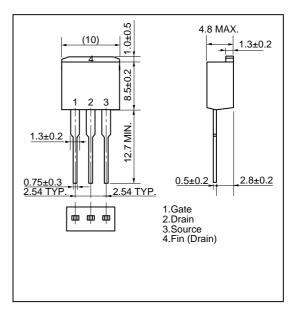
Test circuit 2 Gate charge

## Package Drawing(Unit : mm)

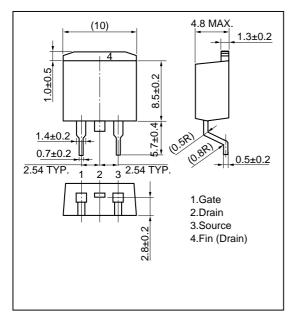
## 1)TO-220AB (MP-25)

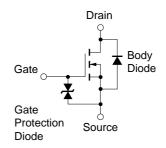


2)TO-262 (TO-220 Fin Cut:MP-25S)



#### 3)TO-263 (JEDEC TYPE:MP-25ZJ)





The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

#### **Preliminary Product Information**

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Anti-radioactive design is not implemented in this product.

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