NEC

MOS FIELD EFFECT TRANSISTOR

2SK3322

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK3322 is N-Channel DMOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3322	TO-220AB
2SK3322-S	TO-262
2SK3322-ZJ	TO-263(MP-25ZJ)

FEATURES

- Low gate charge :
  Q_G = 15 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 4.0 A)
- Gate voltage rating : ±30 V
- Low On-state resistance :
  $R_{DS(on)}$ = 2.2 Ω MAX. (V_{GS} = 10 V, I_D = 2.8 A)
- Avalanche capability ratings
- Surface mount package available.

ABSOLTE MAXIMUM RATINGS (T_A = 25°C)

Drain to source voltage (V_{GS} = 0 V)	V_{DSS}	600	V
Gate to source voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain current (DC) (T_C = 25°C)	$I_{D(DC)}$	±5.5	A
Drain current (pulse) Note1	$I_{D(pulse)}$	±20	A
Total power dissipation (T_A = 25°C)	P_{T1}	1.5	W
Total power dissipation (T_C = 25°C)	P_{T2}	65	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C
Single avalanche current Note2	I_{AS}	4.0	A
Single avalanche energy Note2	E_{AS}	10.7	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

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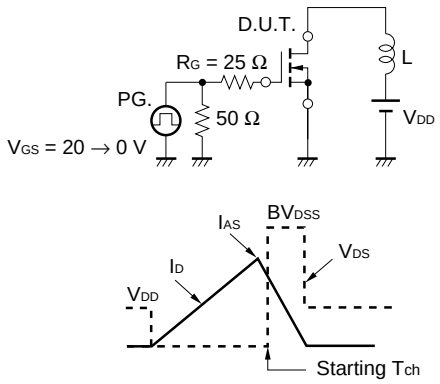
The mark ★ shows major revised points.

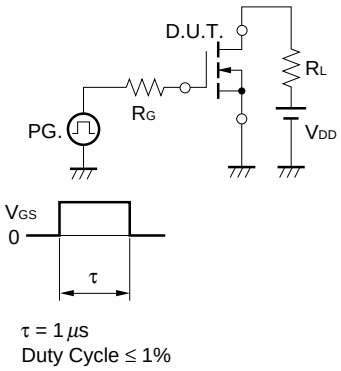
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5		3.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 2.8 A	1.0			S
Drain to Source On-state Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.8 A		1.7	2.2	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		550		pF
Output Capacitance	C_{oss}			115		pF
Reverse Transfer Capacitance	C_{rss}			13		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 2.8 A, $V_{GS(on)}$ = 10 V,		12		ns
Rise Time	t_r	R_G = 10 Ω		10		ns
Turn-off Delay Time	$t_{d(off)}$			35		ns
Fall Time	t_f			12		ns
Total Gate Charge	Q_G	V_{DD} = 450 V, V_{GS} = 10 V, I_D = 4.0 A		15		nC
Gate to Source Charge	Q_{GS}			4		nC
Gate to Drain Charge	Q_{GD}			4.4		nC
Diode Forward Voltage	$V_{F(S-D)}$	I_F = 5.5 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 4.0 A, V_{GS} = 0 V, di/dt = 50 A /μs		1.3		μs
Reverse Recovery Charge	Q_{rr}			4.3		μC

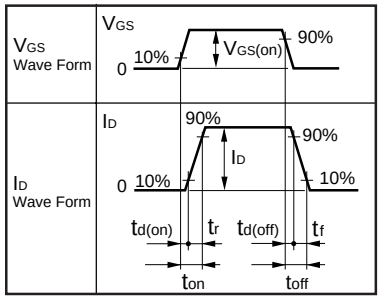
TEST CIRCUIT 1 AVALANCHE CAPABILITY



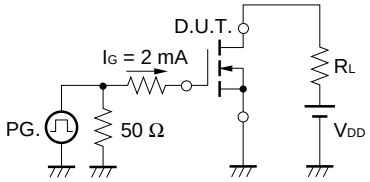
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

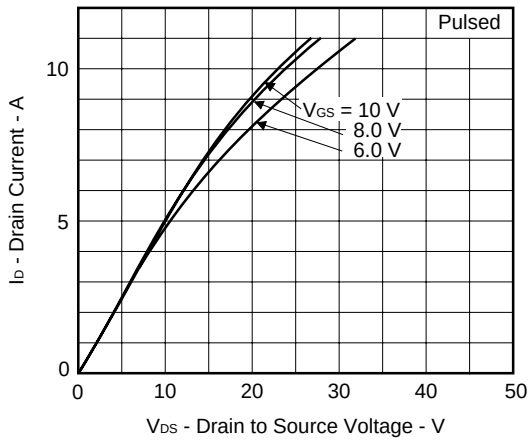


TEST CIRCUIT 3 GATE CHARGE

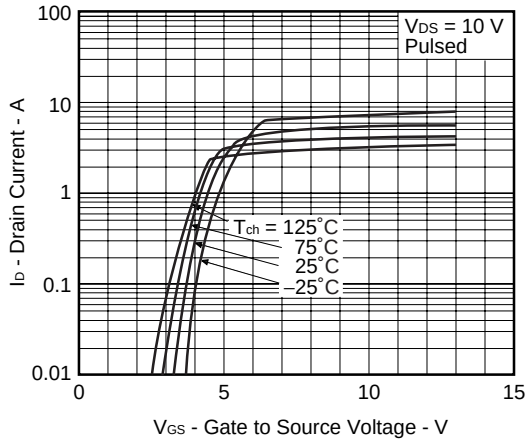


★ TYPICAL CHARACTERISTICS (T_A = 25°C)

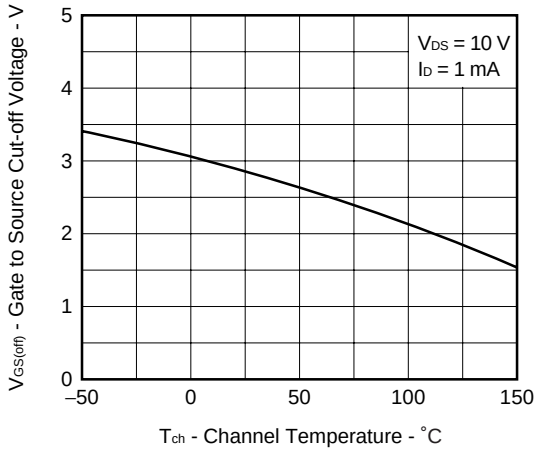
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



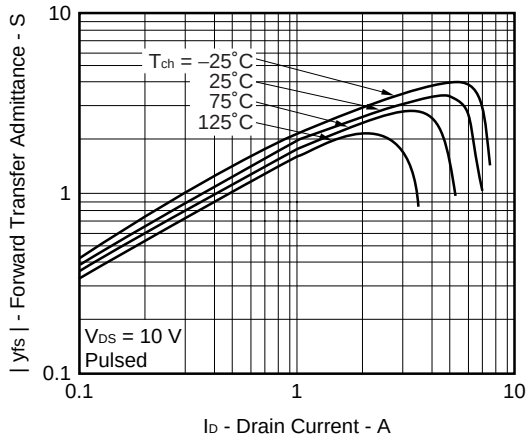
FORWARD TRANSFER CHARACTERISTICS



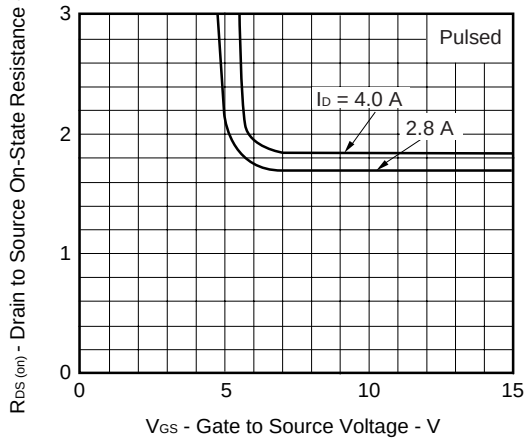
GATE TO SOURCE CUT-OFF VOLTAGE
vs. CHANNEL TEMPERATURE



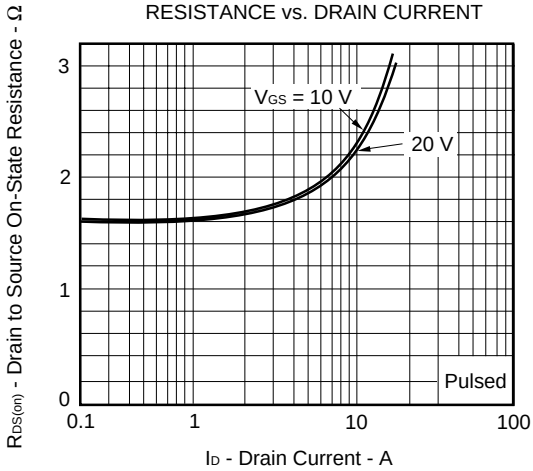
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



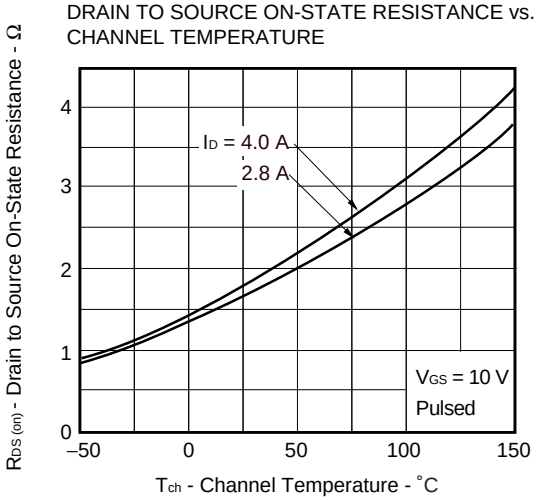
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



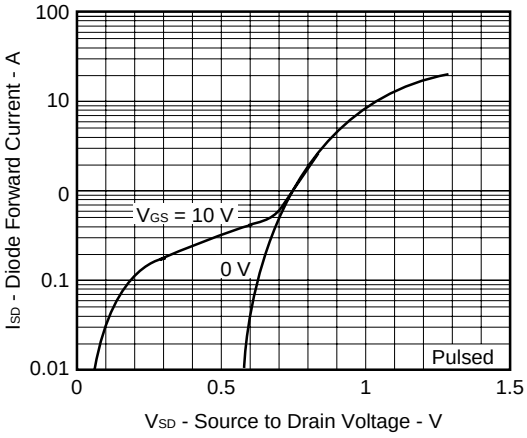
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



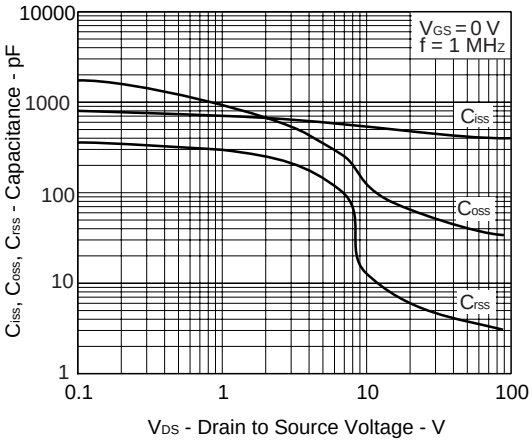
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



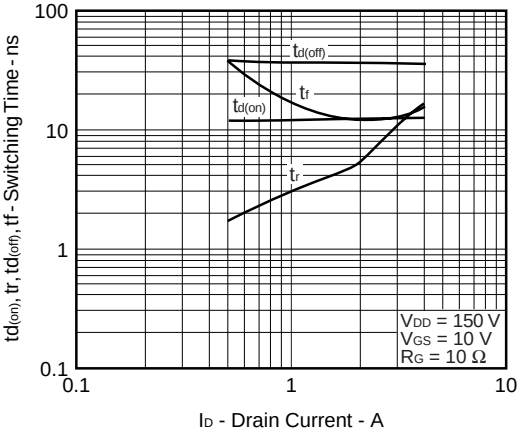
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



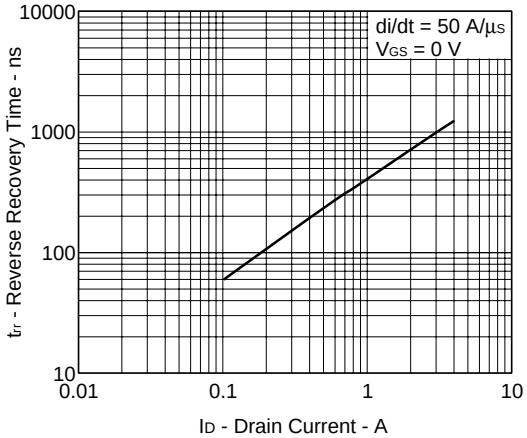
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



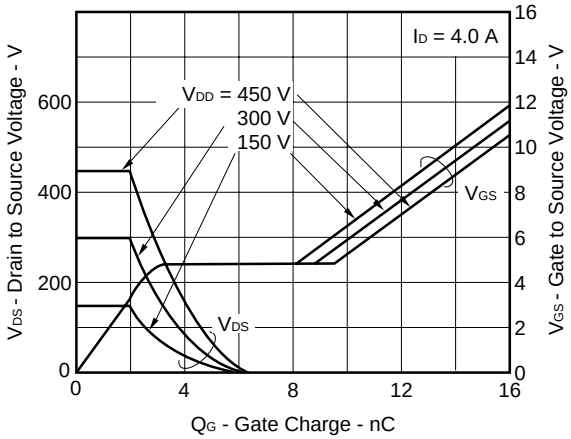
SWITCHING CHARACTERISTICS



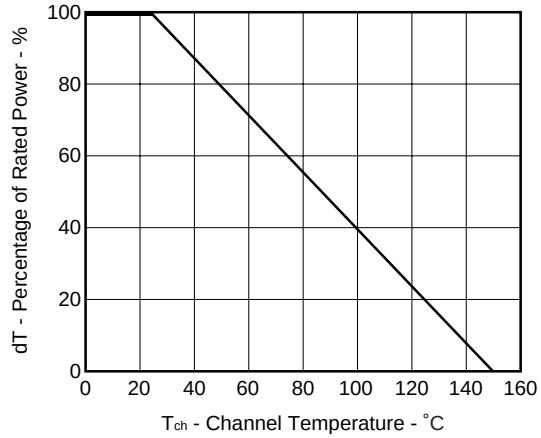
REVERSE RECOVERY TIME vs. DRAIN CURRENT



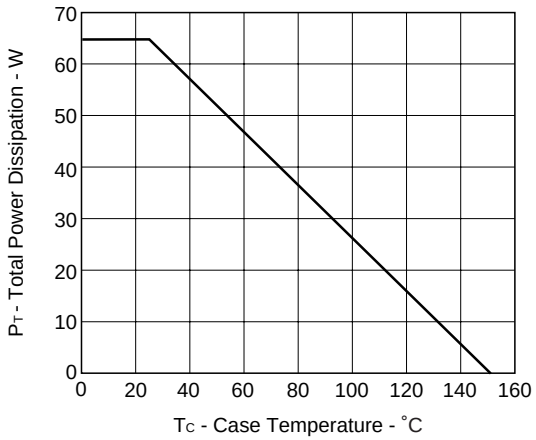
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



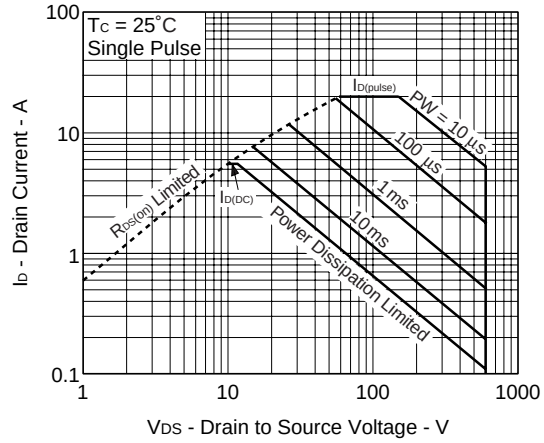
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



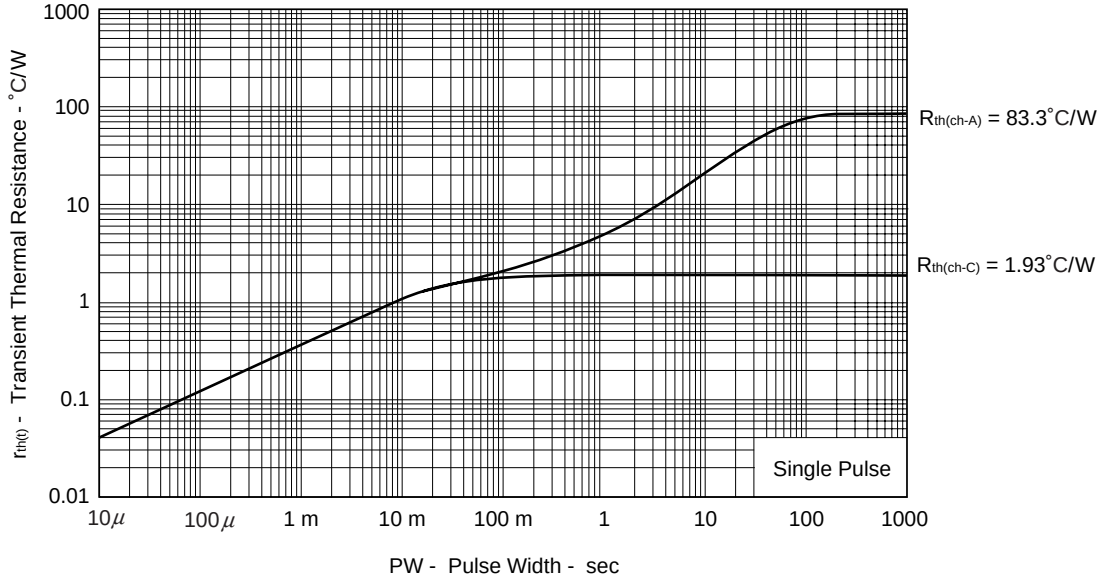
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



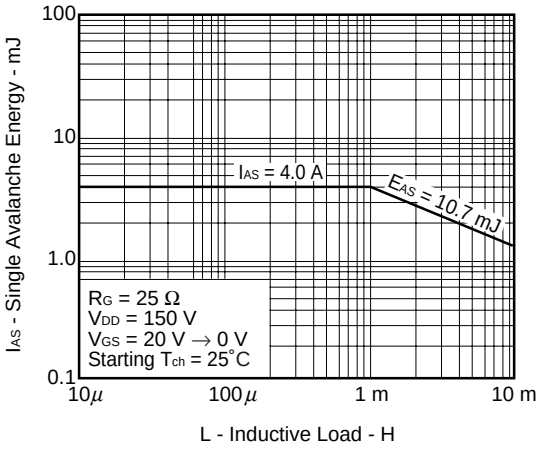
FORWARD BIAS SAFE OPERATING AREA



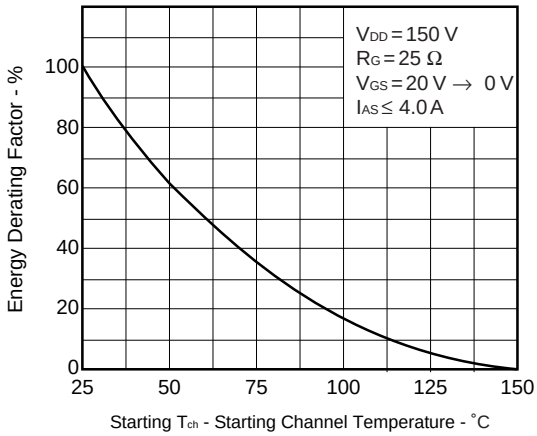
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



SINGLE AVALANCHE ENERGY vs.
INDUCTIVE LOAD

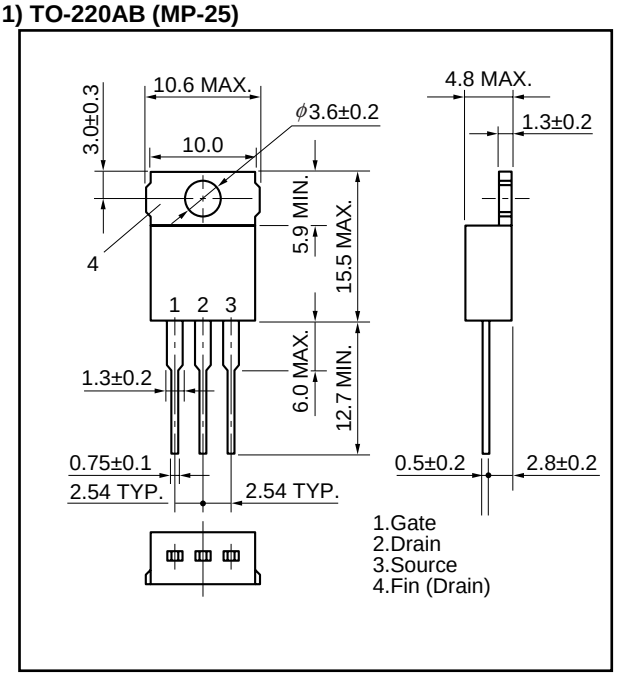


SINGLE AVALANCHE ENERGY
DERATING FACTOR

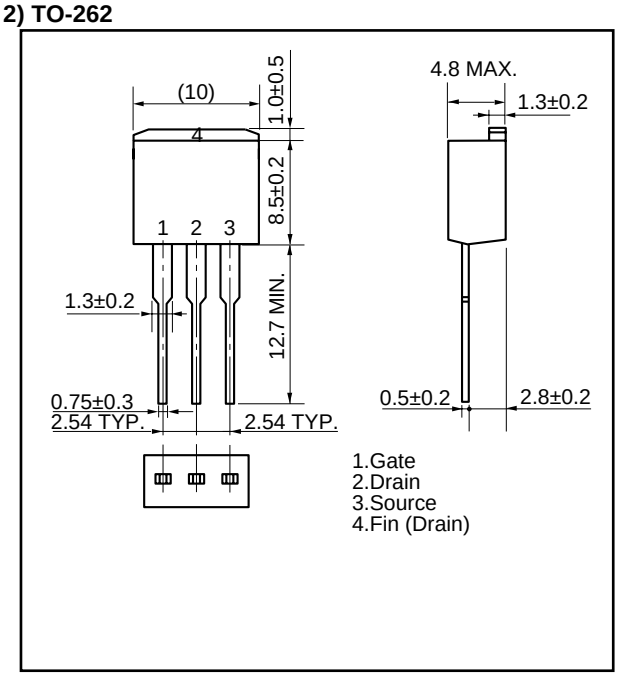


PACKAGE DRAWINGS (Unit : mm)

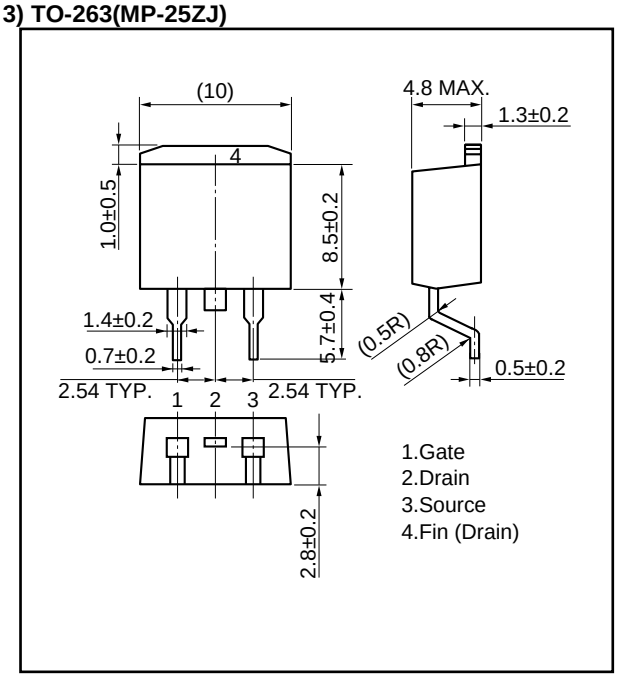
1) TO-220AB (MP-25)



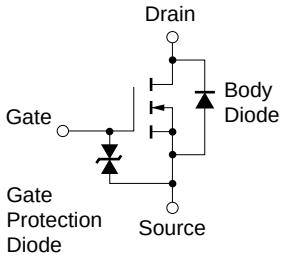
2) TO-262



3) TO-263(MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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