

MOS FIELD EFFECT TRANSISTOR

2SK3510

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3510 is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super low on-state resistance:
- $R_{DS(on)} = 8.5 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, \text{ ID} = 42 \text{ A})$
- Low Ciss: $C_{iss} = 8500 \, pF \, TYP$.
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	•	,	
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	75	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	D(DC)	±83	А
Drain Current (pulse) ^{Note1}	D(pulse)	±332	А
Total Power Dissipation (Tc = 25°C)	P⊤1	125	W
Total Power Dissipation (T _A = 25°C)	P T2	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	69	А
Single Avalanche Energy Note2	Eas	450	mJ

Notes 1. PW \leq 10 $\mu s,$ Duty Cycle \leq 1%

2. Starting T_ch = 25°C, V_DD = 35 V, R_G = 25 $\Omega,$ V_Gs = 20 \rightarrow 0 V

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3510	TO-220AB
2SK3510-S	TO-262
2SK3510-ZJ	TO-263
2SK3510-Z	TO-220SMD ^{Note}

Note TO-220SMD package is produced only in Japan.

(TO-220AB)





(TO-263, TO-220SMD)



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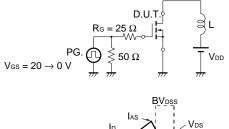
Document No. Date Published Printed in Japan

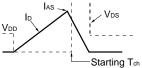
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	Vds = 75 V, Vgs = 0 V			10	μA
Gate Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	Vds = 10 V, Id = 1 mA	2.0	3.0	4.0	V
Forward Transfer Admittance	yfs	Vds = 10 V, Id = 42 A	30	60		S
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, Id = 42 A		6.5	8.5	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		8500		pF
Output Capacitance	Coss	Vgs = 0 V		1300		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		650		pF
Turn-on Delay Time	td(on)	Vdd = 38 V, Id = 42 A		35		ns
Rise Time	tr	V _G s = 10 V		28		ns
Turn-off Delay Time	td(off)	R _G = 0 Ω		105		ns
Fall Time	tr			16		ns
Total Gate Charge	QG	Vdd = 60 V		150		nC
Gate to Source Charge	Q _{GS}	Vgs = 10 V		30		nC
Gate to Drain Charge	Qgd	ID = 83 A		52		nC
Body Diode Forward Voltage	VF(S-D)	IF = 83 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 83 A, VGS = 0 V		80		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		240		nC

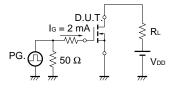
TEST CIRCUIT 1 AVALANCHE CAPABILITY

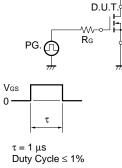
TEST CIRCUIT 2 SWITCHING TIME

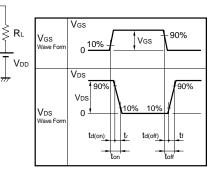




TEST CIRCUIT 3 GATE CHARGE

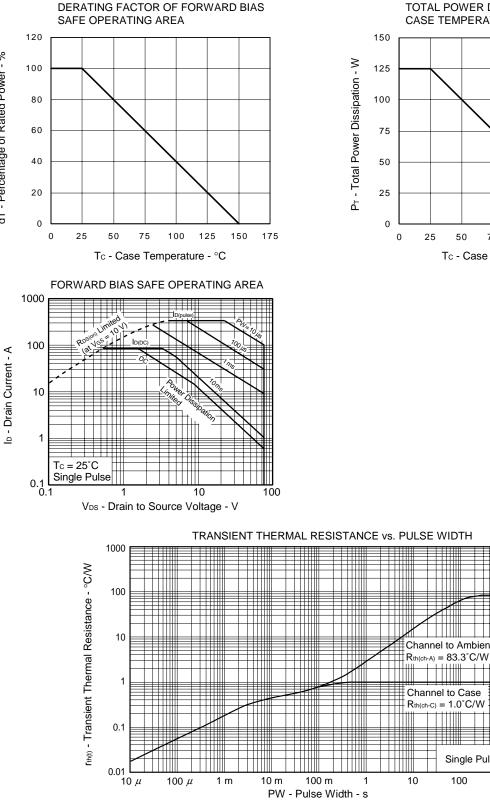


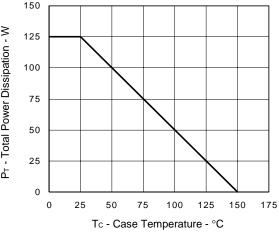




dT - Percentage of Rated Power - %

TYPICAL CHARACTERISTICS ($T_A = 25^{\circ}C$)





Channel to Ambient

Single Pulse

1000

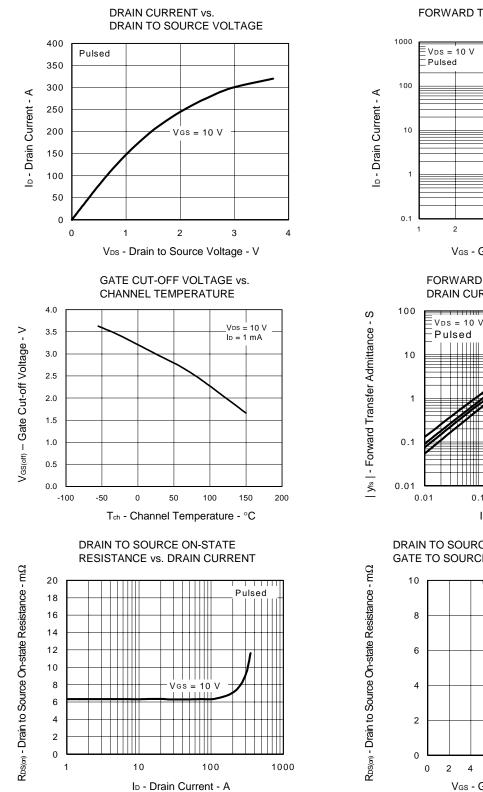
100

10

TOTAL POWER DISSIPATION vs.

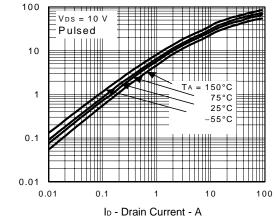
CASE TEMPERATURE

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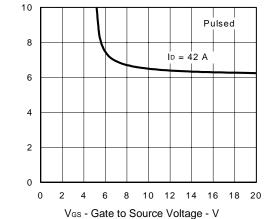


FORWARD TRANSFER CHARACTERISTICS

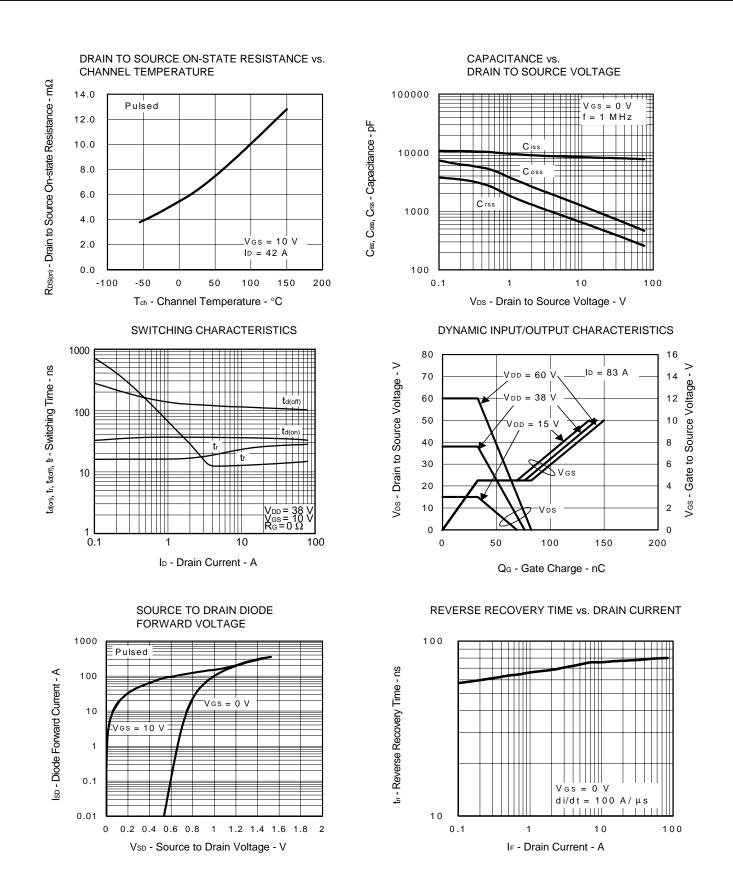
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

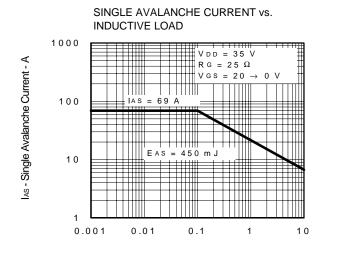


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



NEC





L - Inductive Load - mH

SINGLE AVALANCHE ENERGY DERATING FACTOR 160 Vdd = 35 V Rg = 25 Ω 140 $V\text{Gs}=20\rightarrow 0~\text{V}$ Ias ≤ 69 A 120 100 80 60 40 20 0L 25 50 75 100 150

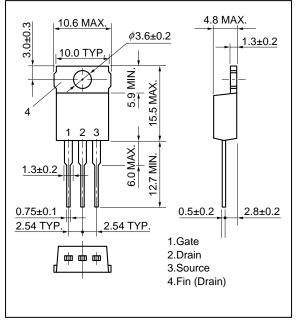
Energy Derating Factor - %

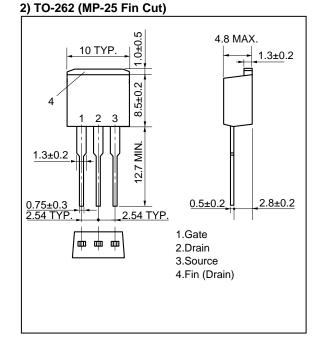
Starting Tch - Starting Channel Temperature - °C

125

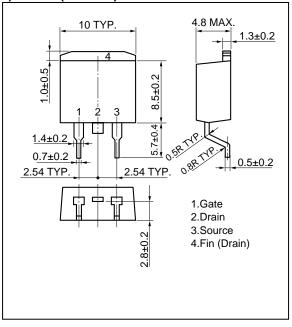
PACKAGE DRAWINGS (Unit: mm)

1) TO-220AB (MP-25)

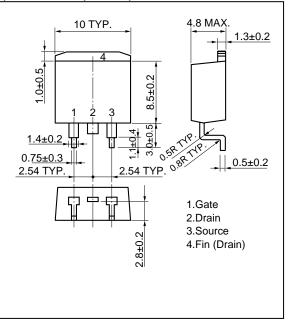




3) TO-263 (MP-25ZJ)



4) TO-220SMD (MP-25Z)^{Note}



Note This package is produced only in Japan.

Gate

Source

Gate Protection

Diode

EQUIVALENT CIRCUIT

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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