

MOS FIELD EFFECT TRANSISTOR 2SK3572

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3572 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

ORDERING INFORMATION

Part number	Package
2SK3572-ZK	TO-263(MP-25ZK)

FEATURES

- 4.5V drive available.
- Low on-state resistance,
 $R_{DS(on)} = 5.7 \text{ m}\Omega \text{ MAX. @ } V_{GS} = 10 \text{ V, } I_D = 40 \text{ A}$
- Low gate charge,
 $Q_g = 32 \text{ nC TYP. @ } I_D = 80 \text{ A, } V_{DD} = 16 \text{ V, } V_{GS} = 10 \text{ V}$
- Built-in gate protection diode.
- Surface mount device available.

ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$)

Drain to source voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	20	V
Gate to source voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain current(DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 80	A
Drain current(pulse) ^{Note}	$I_{D(pulse)}$	± 300	A
Total power dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	1.5	W
Total power dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	52	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

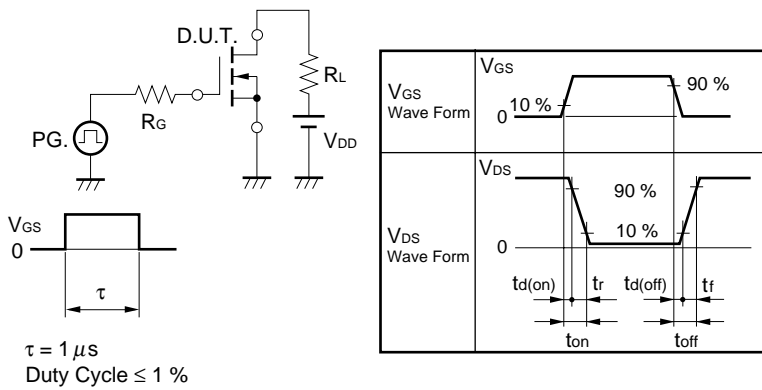
Note $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

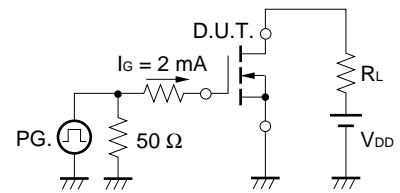
ELECTRICAL CHARACTERISTICS(T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain leakage current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate leakage current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate cut-off voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward transfer admittance	y _{fs}	V _{DS} = 10 V, I _D = 40 A	15			S
Drain to source on-State resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 40 A		4.4	5.7	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 40 A		7.4	9.9	mΩ
Input capacitance	C _{iss}	V _{DS} = 10 V		1700		pF
Output capacitance	C _{oss}	V _{GS} = 0 V		700		pF
Reverse transfer capacitance	C _{rss}	f = 1 MHz		250		pF
Turn-on delay time	t _{d(on)}	V _{DD} = 10 V, I _D = 40 A V _{GS(on)} = 10 V R _G = 10 Ω		16		ns
Rise time	t _r			14		ns
Turn-off delay time	t _{d(off)}			50		ns
Fall time	t _f			12		ns
Total gate charge	Q _G	V _{DD} = 16 V		32		nC
Gate to source charge	Q _{GS}	V _{GS} = 10 V		7.1		nC
Gate to drain charge	Q _{GD}	I _D = 80 A		7.7		nC
Diode forward voltage	V _{F(S-D)}	I _F = 80 A, V _{GS} = 0 V		1.0		V
Reverse recovery time	t _{rr}	I _F = 80 A, V _{GS} = 0 V		42		ns
Reverse recovery charge	Q _{rr}	di/dt = 100 A/μs		34		nC

TEST CIRCUIT 1 SWITCHING TIME

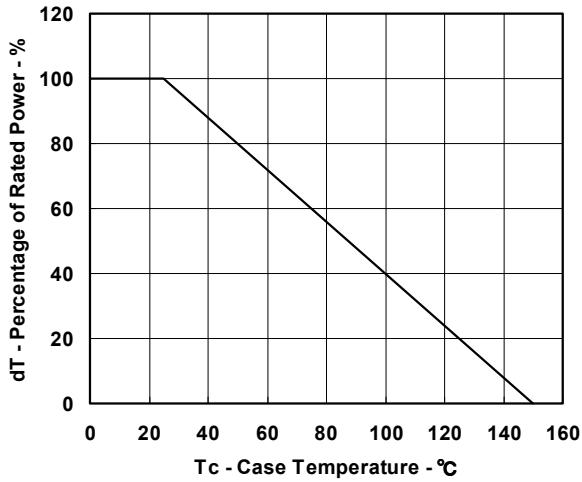


TEST CIRCUIT 2 GATE CHARGE

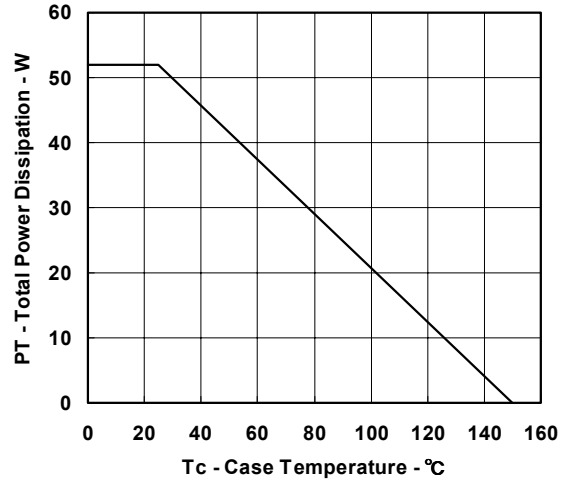


TYPICAL CHARACTERISTICS(T_A = 25°C)

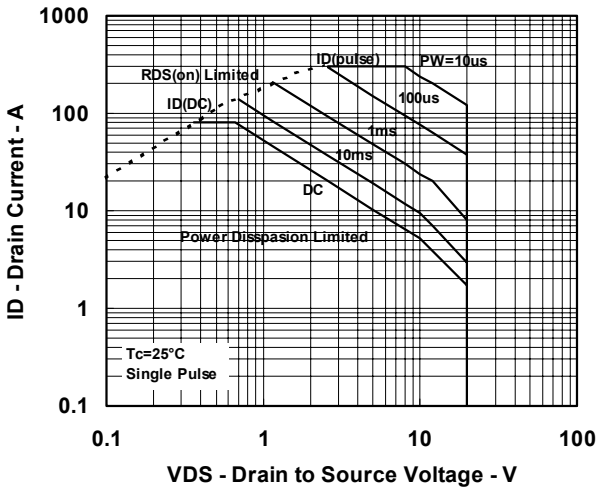
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



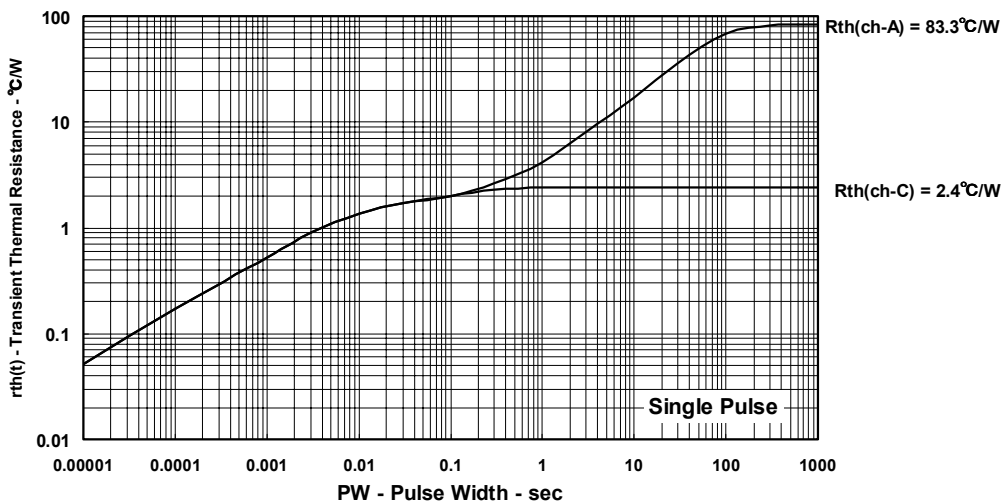
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

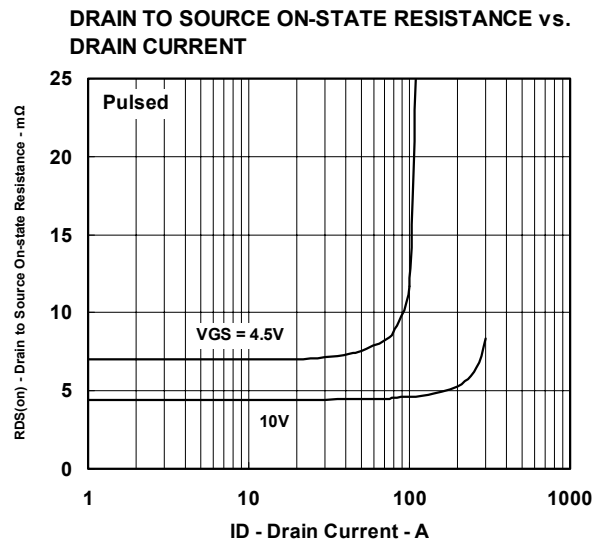
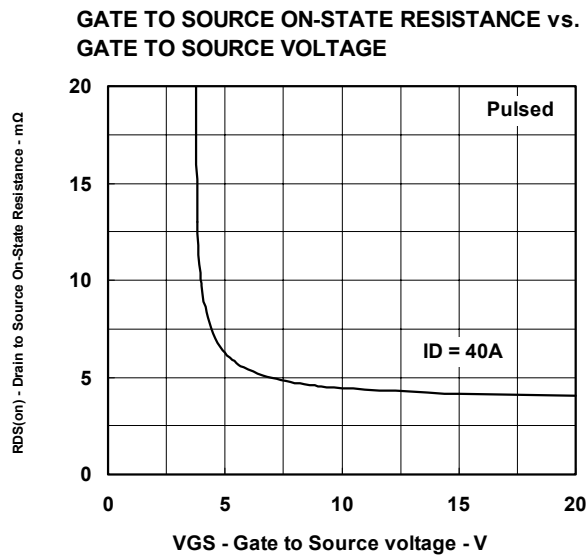
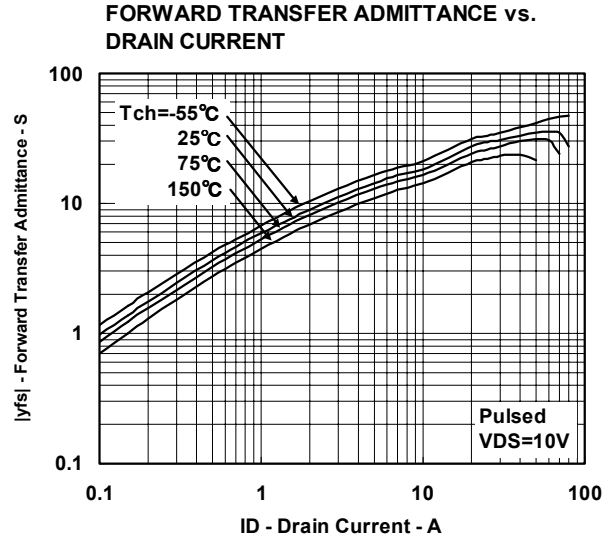
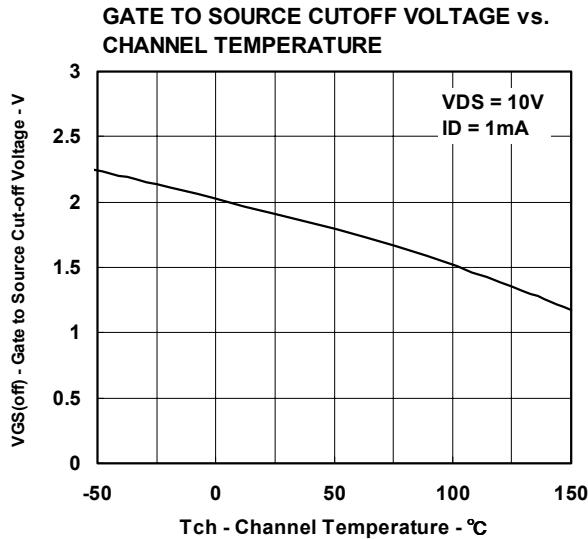
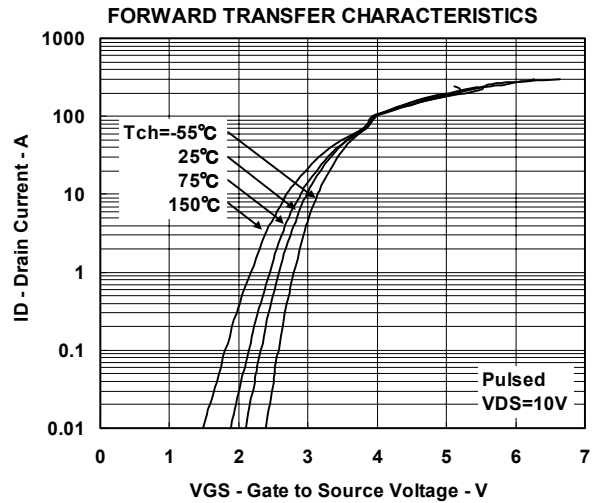
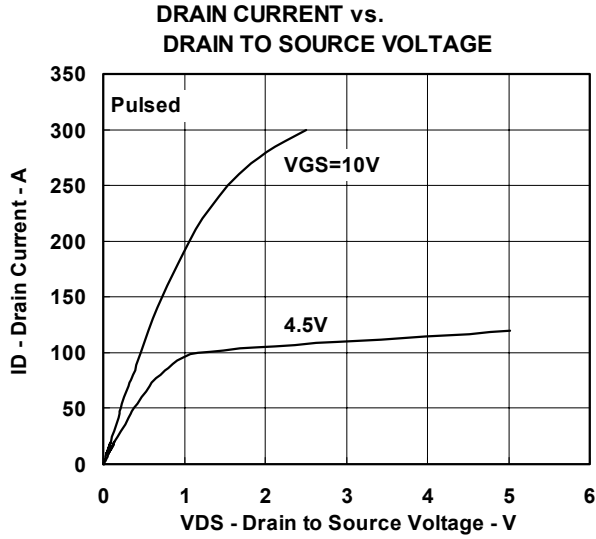


FORWARD BIAS SAFE OPERATING AREA

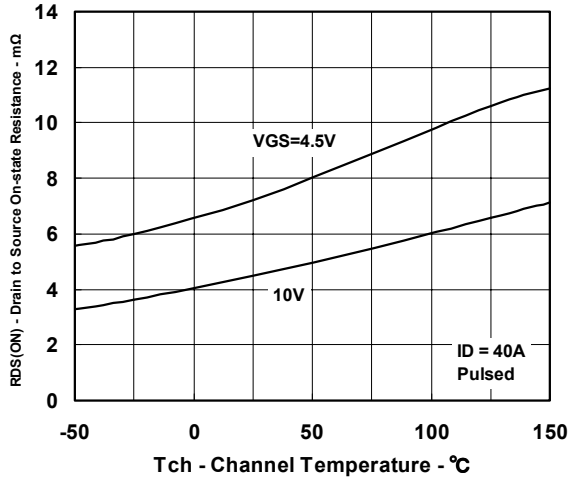


Transient Thermal Resistance vs. Pulse Width

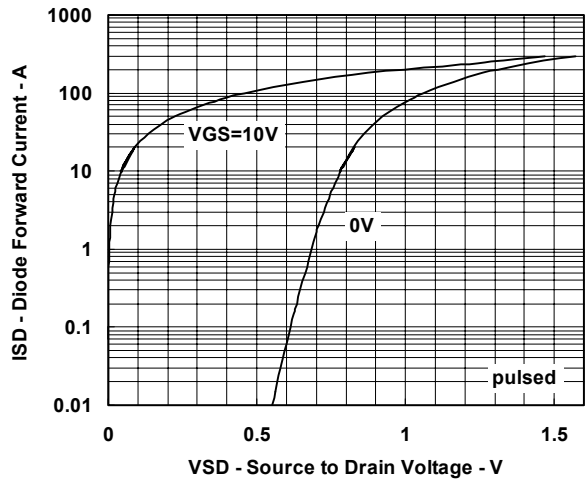




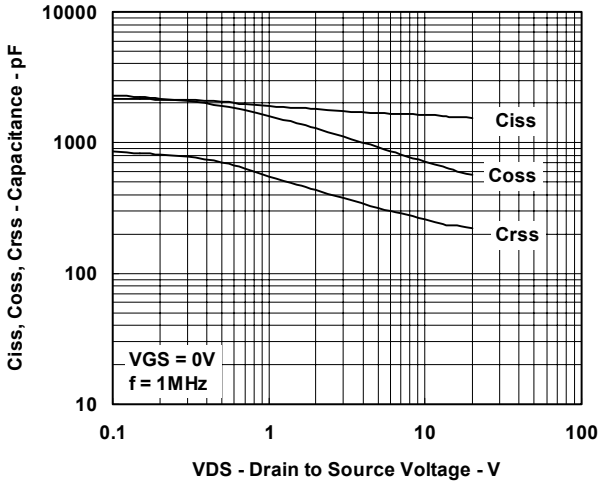
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



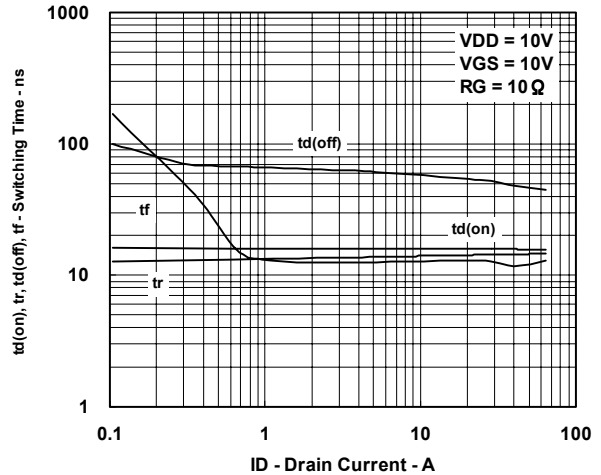
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



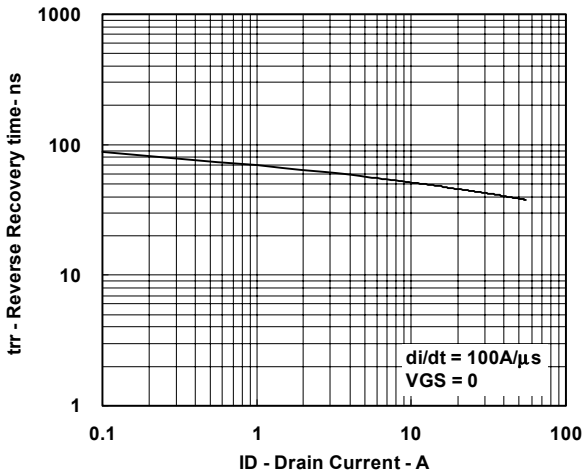
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



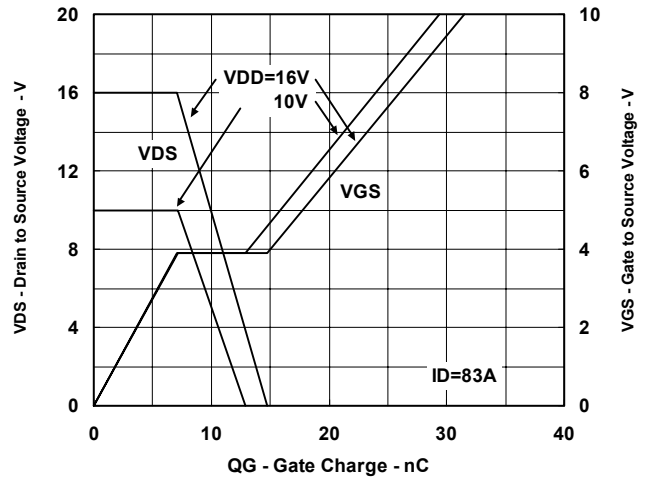
SWITCHING CHARACTERISTIC



REVERSE RECOVERY TIME vs. DRAIN CURRENT

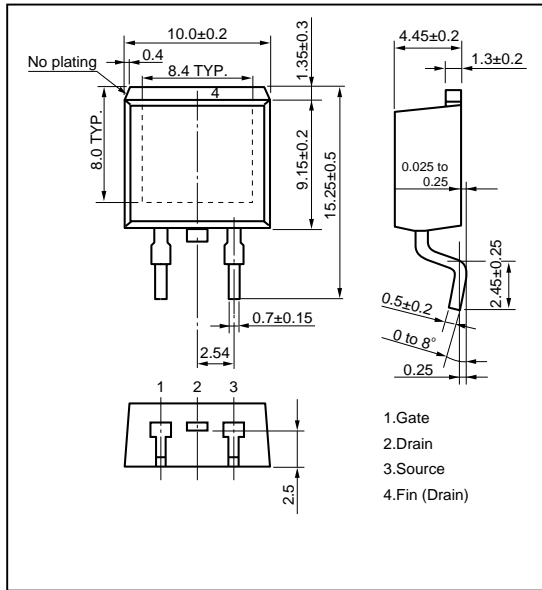


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

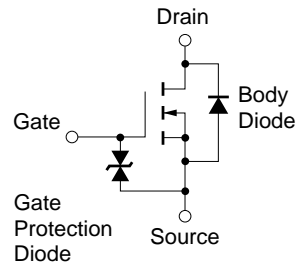


Package Drawing(Unit : mm)

1)TO-263 (MP-25ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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