



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

5LN01SP — N-Channel Silicon MOSFET — Ultrahigh-Speed Switching Applications

Features

- Low ON-resistance
- Ultrahigh-speed switching
- 2.5V drive

Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V _{DSS}		50	V
Gate-to-Source Voltage	V _{GSS}		±10	V
Drain Current (DC)	I _D		0.1	A
Drain Current (Pulse)	I _{DP}	PW≤10μs, duty cycle≤1%	0.4	A
Allowable Power Dissipation	P _D		0.25	W
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

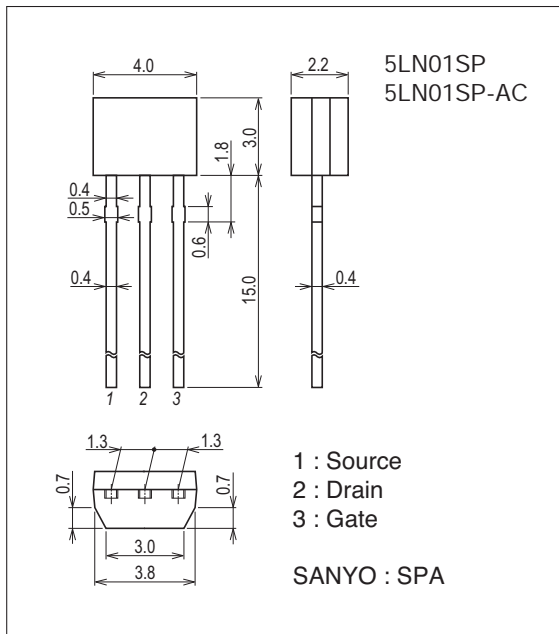
This product is designed to "ESD immunity < 200V**", so please take care when handling.

* Machine Model

Package Dimensions

unit : mm (typ)

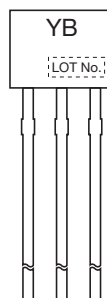
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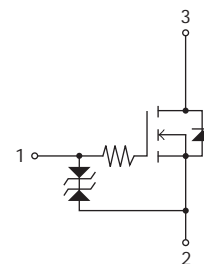
Product & Package Information

- Package : SPA
- JEITA, JEDEC : SC-72
- Minimum Packing Quantity : 2,500 pcs./box, 500 pcs./bag

Marking



Electrical Connection

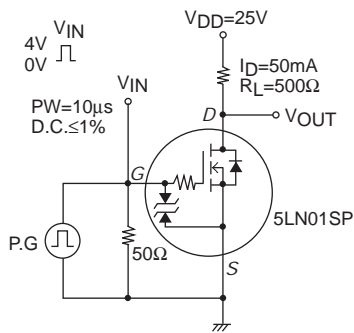


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Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	V(BR)DSS	I _D =1mA, V _{GS} =0V	50			V
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} =50V, V _{GS} =0V			10	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±8V, V _{DS} =0V			±10	μA
Cutoff Voltage	V _{GS(off)}	V _{DS} =10V, I _D =100μA	0.4		1.3	V
Forward Transfer Admittance	y _{fs}	V _{DS} =10V, I _D =50mA	0.13	0.18		S
Static Drain-to-Source On-State Resistance	R _{DS(on)1}	I _D =50mA, V _{GS} =4V		6	7.8	Ω
	R _{DS(on)2}	I _D =30mA, V _{GS} =2.5V		7.1	9.9	Ω
	R _{DS(on)3}	I _D =10mA, V _{GS} =1.5V		10	20	Ω
Input Capacitance	C _{iss}	V _{DS} =10V, f=1MHz		6.6		pF
Output Capacitance	C _{oss}			4.7		pF
Reverse Transfer Capacitance	C _{rss}			1.7		pF
Turn-ON Delay Time	t _{d(on)}		See specified Test Circuit.		18	
Rise Time	t _r			42		ns
Turn-OFF Delay Time	t _{d(off)}			190		ns
Fall Time	t _f			105		ns
Total Gate Charge	Q _g	V _{DS} =10V, V _{GS} =10V, I _D =100mA			1.57	
Gate-to-Source Charge	Q _{gs}			0.20		nC
Gate-to-Drain "Miller" Charge	Q _{gd}			0.32		nC
Diode Forward Voltage	V _{SD}	I _S =100mA, V _{GS} =0V		0.85	1.2	V

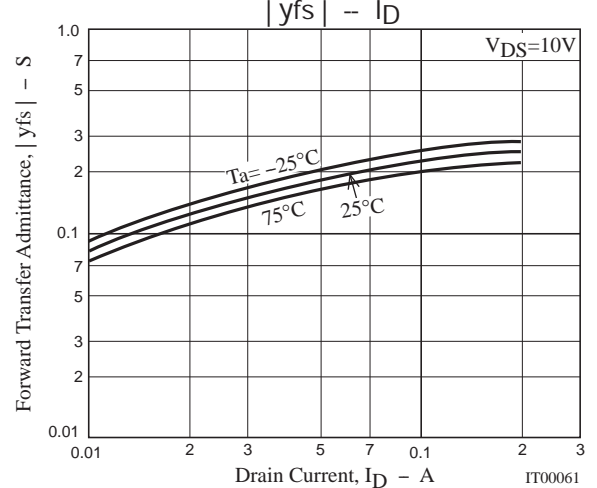
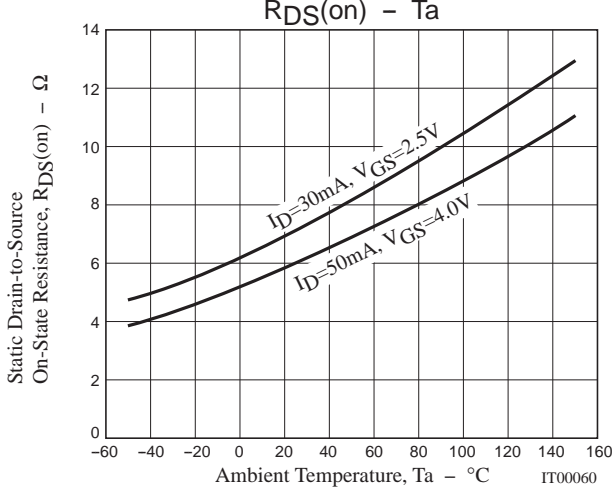
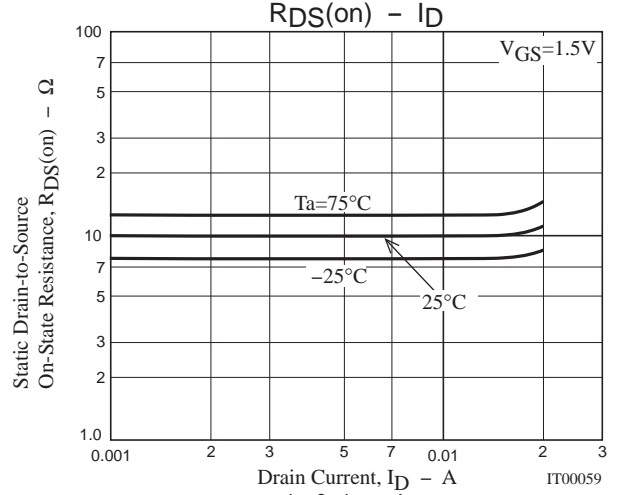
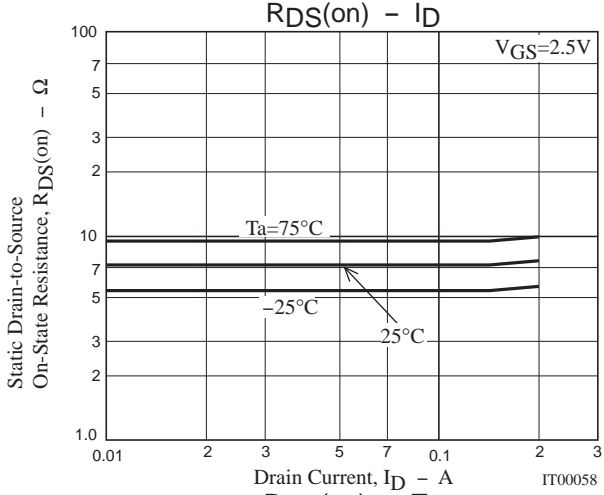
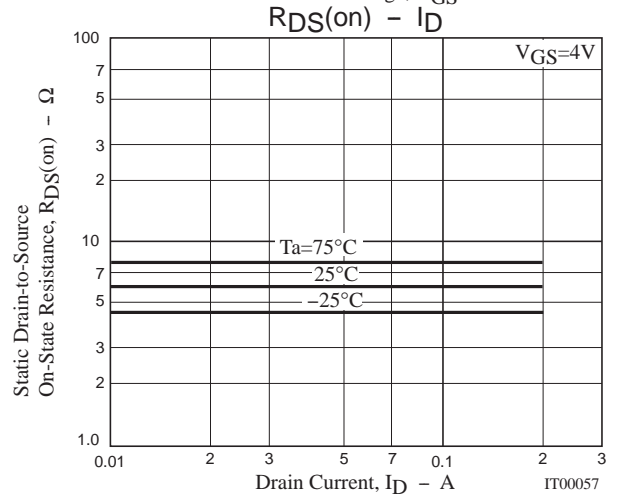
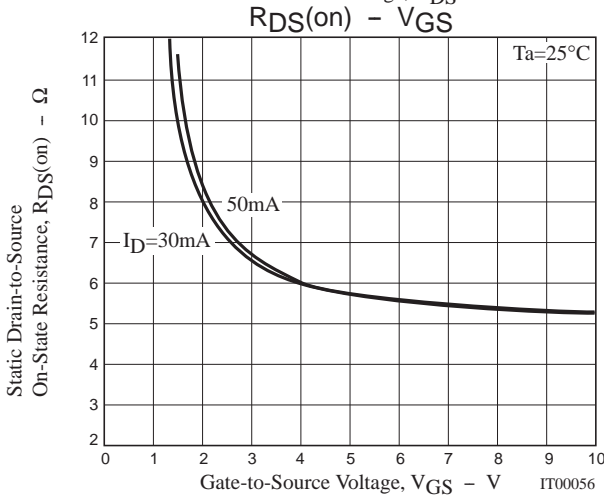
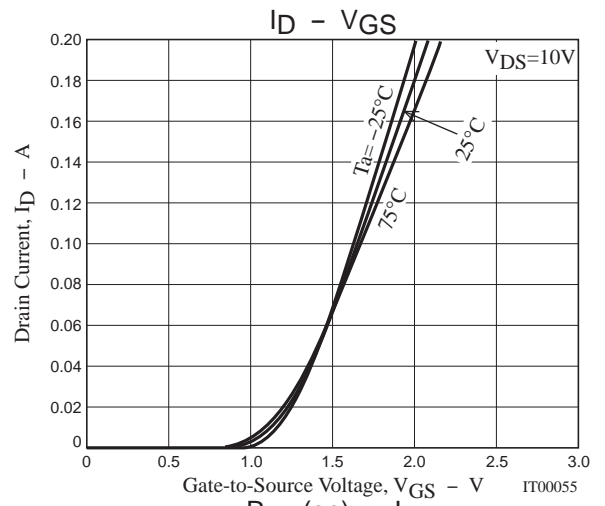
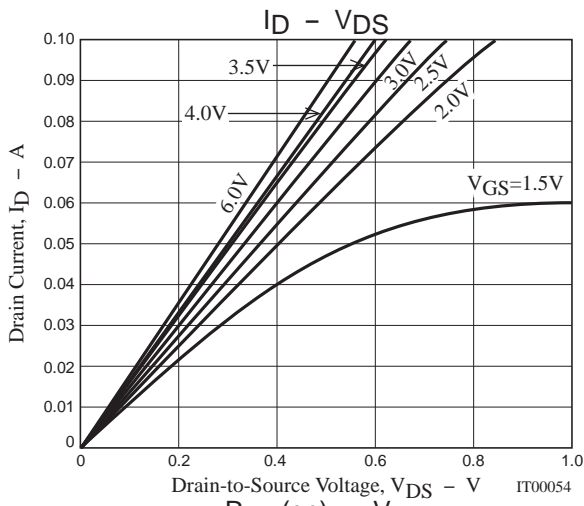
Switching Time Test Circuit



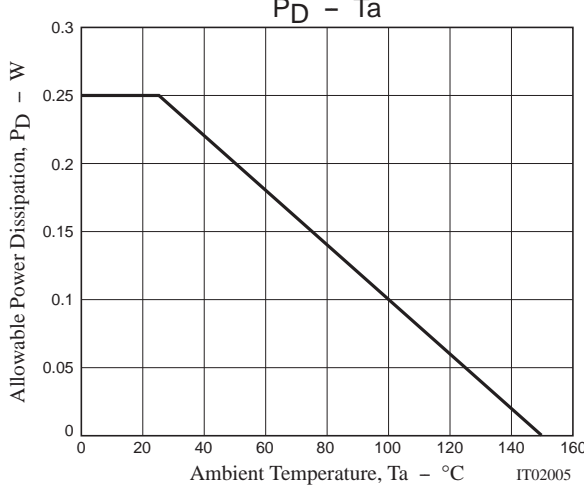
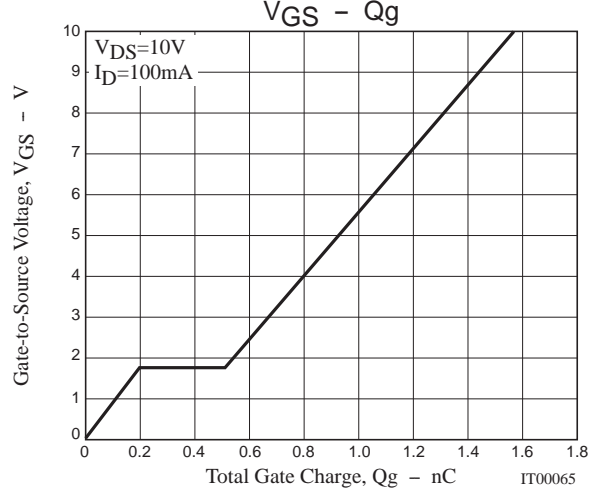
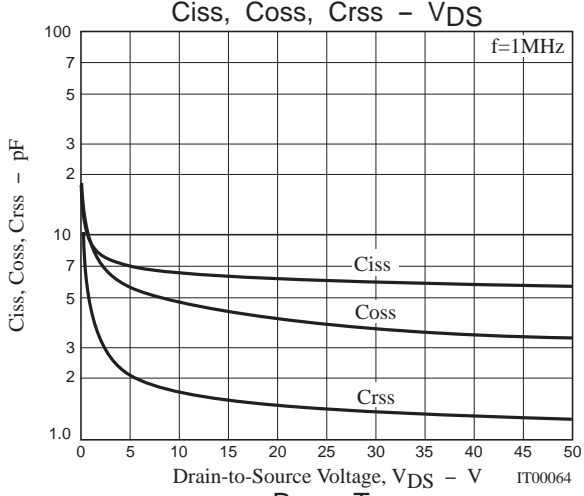
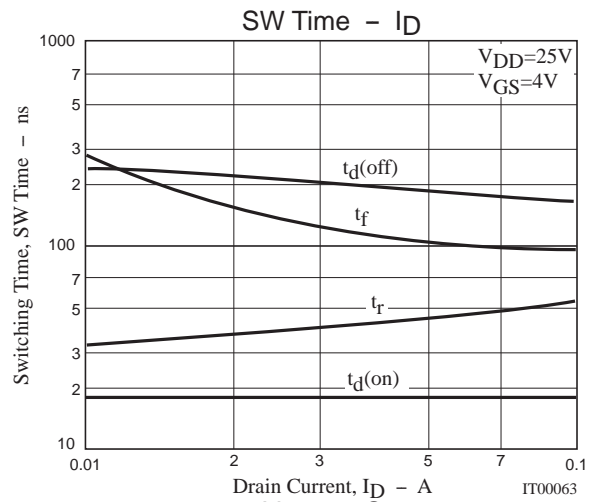
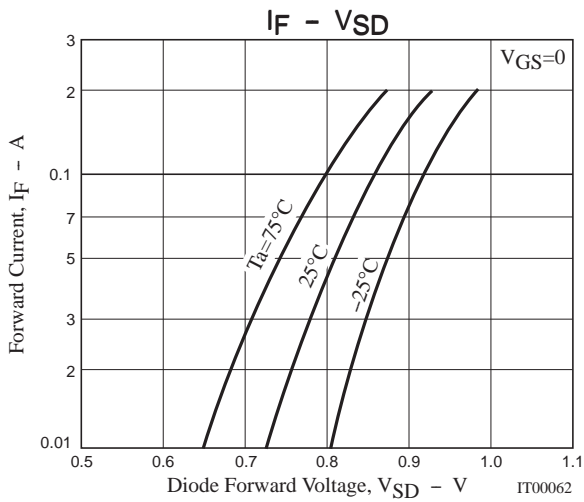
Ordering Information

Device	Package	Shipping	memo
5LN01SP	SPA	500pcs./bag	Pb Free
5LN01SP-AC	SPA	2,500pcs./box	

5LN01SP



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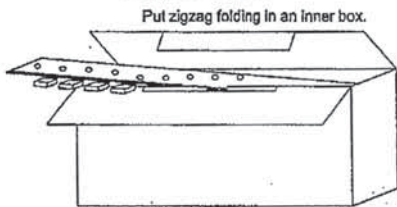
Taping Specification

5LN01SP-AC

Storage package Outline name	Package type	Maximum Number of devices contained(pcs.)		Packing format	
		Inner box No.	Storage quantity	Outer box (C-6)	Outer box (C-8)
SPA	A C	C-2 Inner box Dimensions :mm(external) 330×45×145	2,500	16 inner boxes contained(40,000pcs.) Outer box Dimensions:mm(external) 585×345×200	8 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(external) 345×300×200
	A L	C-2 Inner box Dimensions :mm(external) 330×45×145	2,400	16 inner boxes contained(38,400pcs.) Outer box Dimensions:mm(external) 585×345×200	8 inner boxes contained(19,200pcs.) Outer box Dimensions:mm(internal) 345×300×200
	A P	C-4 Inner box Dimensions :mm(external) 330×45×285	5,000	8 inner boxes contained(40,000pcs.) Outer box Dimensions:mm(external) 585×345×200	4 inner boxes contained(20,000pcs.) Outer box Dimensions:mm(internal) 345×300×200
	A S	C-2 Inner box Dimensions :mm(external) 330×45×145	1,200	16 inner boxes contained(9,200pcs.) Outer box Dimensions:mm(external) 585×345×200	8 inner boxes contained(9,600 pcs.) Outer box Dimensions:mm(internal) 345×300×200

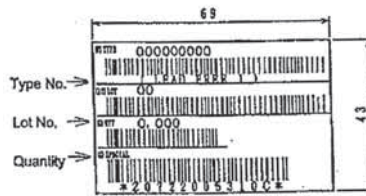
1. Packing format

Packing method



Sample bar code label

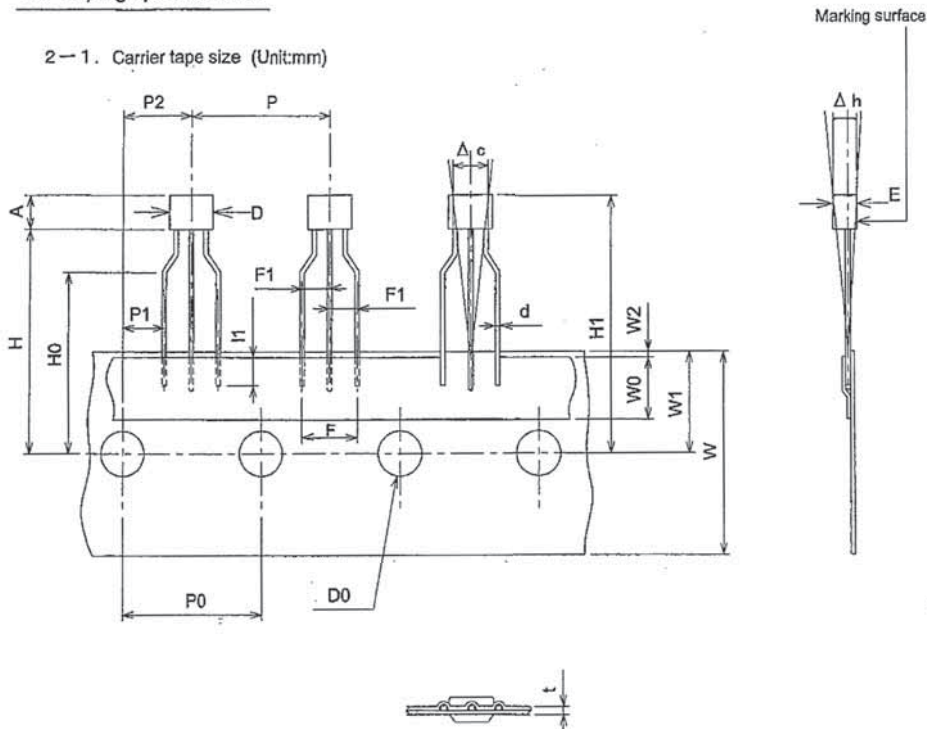
(Unit : mm)



*LEAD FREE 1 :
Lead-free external terminal surface treatment product.

2. Taping specifications

2-1. Carrier tape size (Unit:mm)



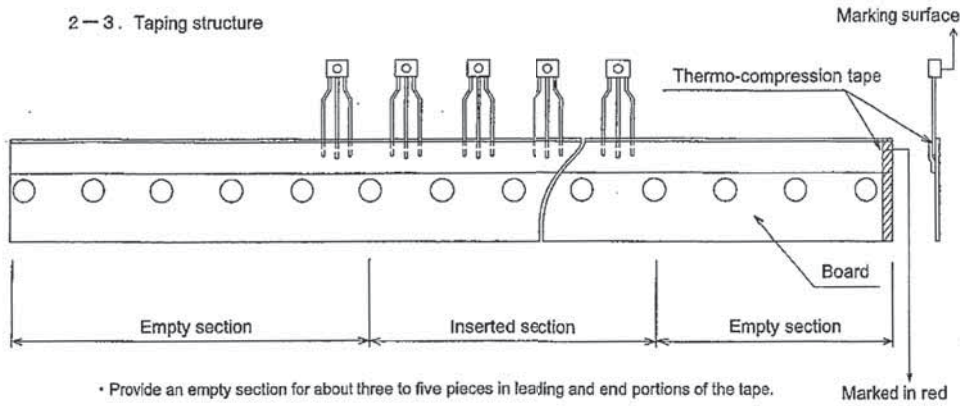
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2-2. Taping size standard

Unit:mm

Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	4.0	±0.2
	E	2.2	±0.2
Work piece height	A	3.0	±0.2
Lead wire diameter	d	0.4 × 0.4 t	±0.1
Bonded lead wire	l1	2.5MIN	
Pitch between products	P	12.7	±1.0
Pitch between perforations	P0	12.7	±0.2
Total pitch for 21 perforations	P0 × 20	254.0	±1.0
Distance between lead wire	F	5.0	+0.8 -0.2
Lead wire pitch distance	F1	2.5	+0.4 -0.1
Product inclination	Δ h	0	±2.0
Displacement of perforations	P1	3.85	±0.3
	P2	6.35	±0.3
Displacement of tape	W2	0.5MAX	Not to be displaced to the outside of the board

2-3. Taping structure



- Provide an empty section for about three to five pieces in leading and end portions of the tape.
- Provide marking in red to the E-side end of the board.

5LN01SP

Bag Packing Specification

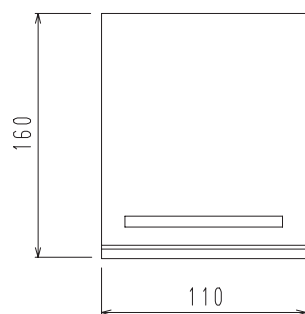
5LN01SP

1. Packing Format

Package Name	Maximum Number of devices contained (pcs)				
	Bag	Inner BOX		Outer BOX	
SPA	500	B-1	B-1/2	A-1	A-2
		20,000	10,000	100,000	60,000
Packing format (Dimensions:mm (external))					
		Inner BOX		Outer BOX	
		B-1	B-1/2	A-1	A-2
		445×225×55	445×225×55	470×250×300	470×250×190

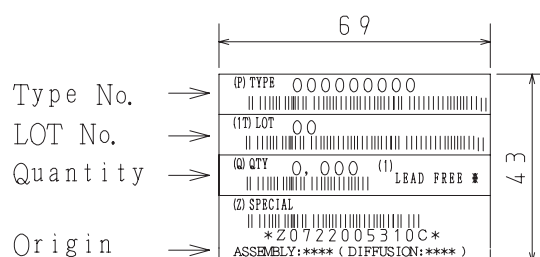
2. Bag dimensions

(unit:mm)



3. Bag label, Inner box label

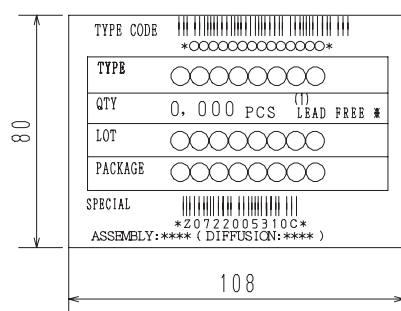
(unit:mm)



4. Outer box label

(unit:mm)

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



NOTE (1)

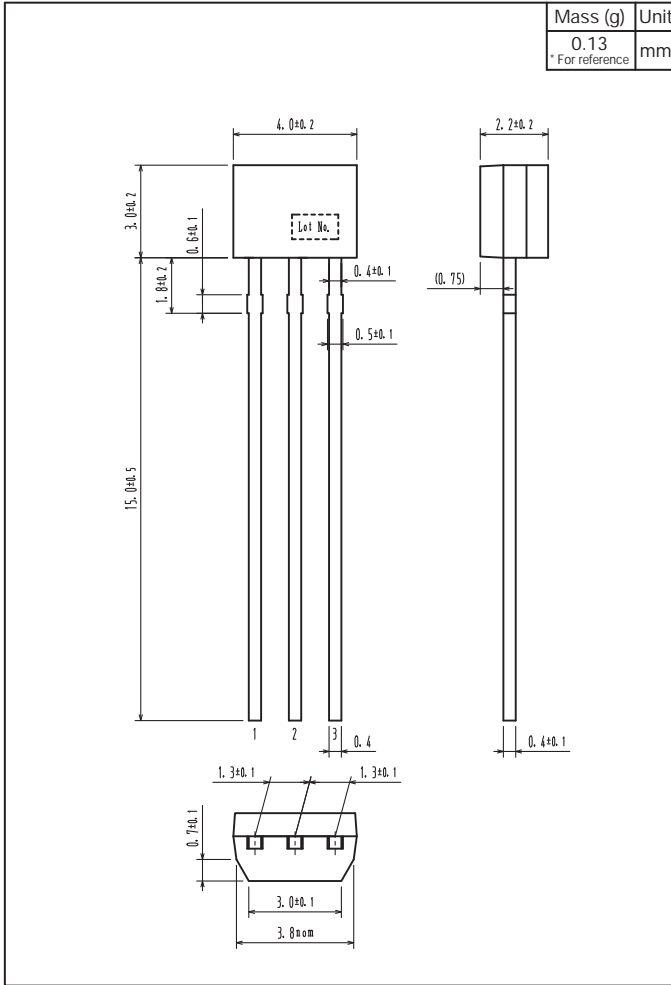
The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

5LN01SP

Outline Drawing

5LN01SP



Note on usage : Since the 5LN01SP is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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