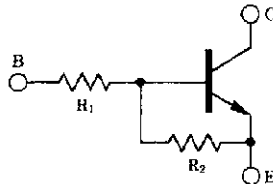


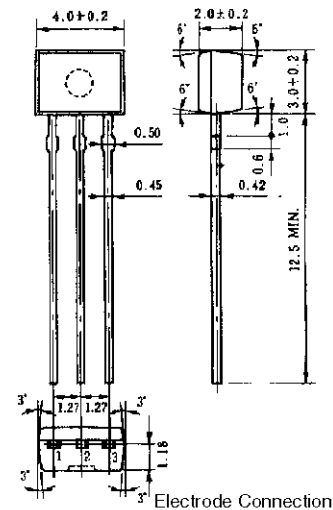
on-chip resistor NPN silicon epitaxial transistor For mid-speed switching

FEATURES

- On-chip bias resistor
($R_1 = 4.7 \text{ k}\Omega$, $R_2 = 10 \text{ k}\Omega$)
- Complementary transistor with BN1L3N



PACKAGE DRAWING (UNIT: mm)



1. Emitter
2. Collector
3. Base

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	V_{CBO}	60	V
Collector to emitter voltage	V_{CEO}	50	V
Emitter to base voltage	V_{EBO}	5	V
Collector current (DC)	$I_{C(DC)}$	100	mA
Collector current (Pulse)	$I_{C(pulse)}$ *	200	mA
Total power dissipation	P_T	250	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \text{ ms}$, duty cycle $\leq 50 \%$

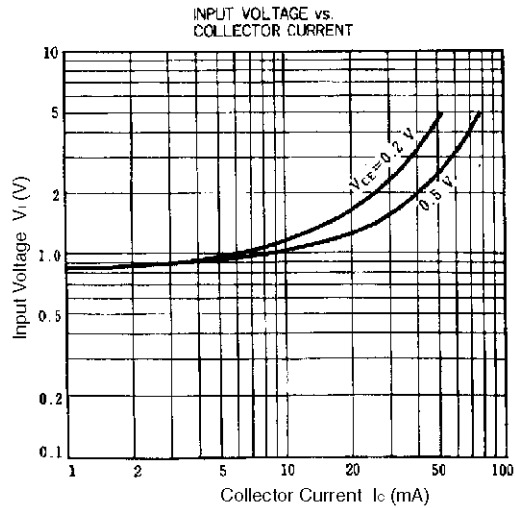
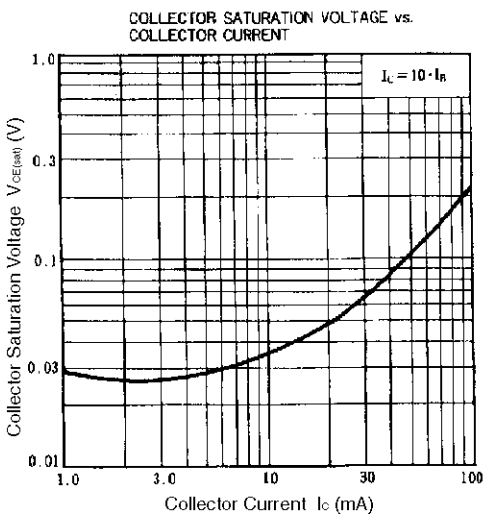
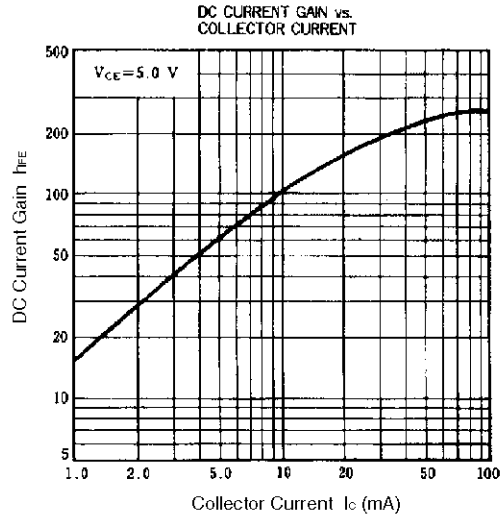
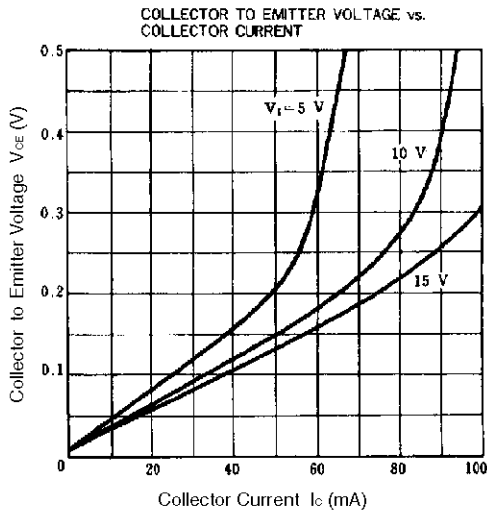
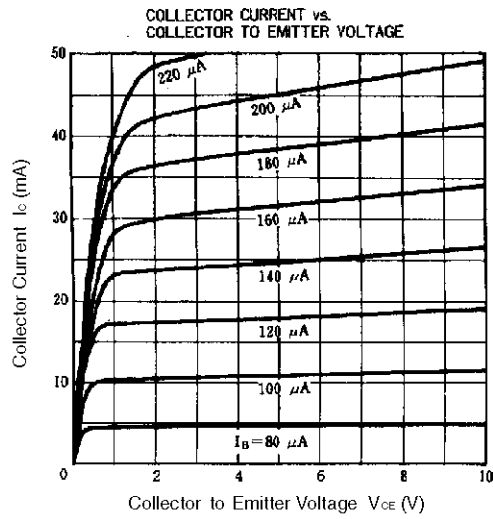
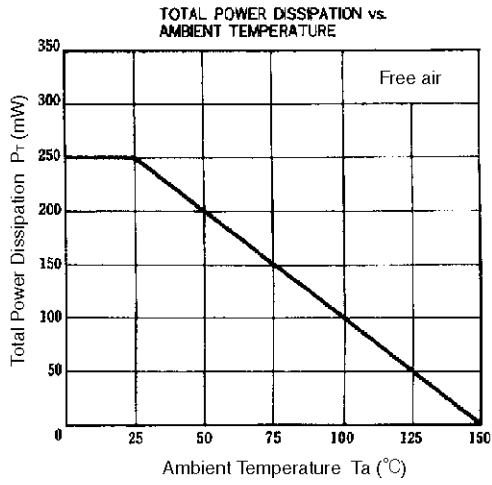
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

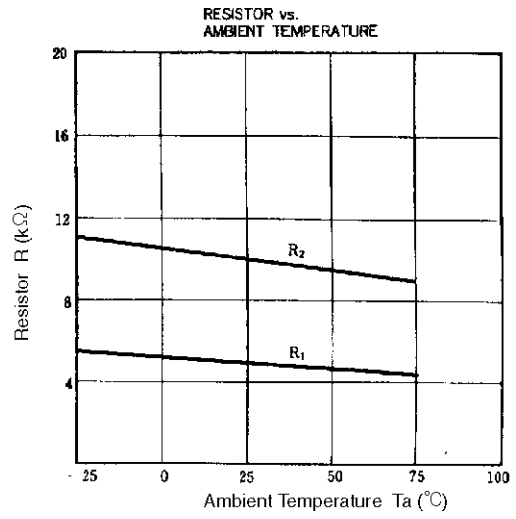
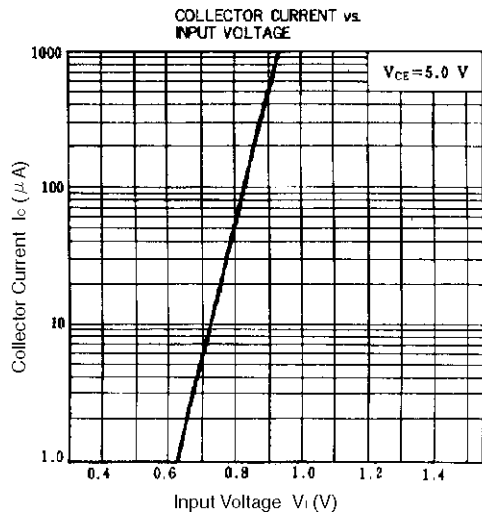
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Collector cutoff current	I_{CBO}	$V_{CB} = 50 \text{ V}$, $I_E = 0$			100	nA
DC current gain	h_{FE1} **	$V_{CE} = 5.0 \text{ V}$, $I_C = 5.0 \text{ mA}$	35	60	80	-
DC current gain	h_{FE2} **	$V_{CE} = 5.0 \text{ V}$, $I_C = 50 \text{ mA}$	80	230		-
Collector saturation voltage	$V_{CE(sat)}$ **	$I_C = 5.0 \text{ mA}$, $I_B = 0.25 \text{ mA}$		0.05	0.2	V
Low level input voltage	V_{IL} **	$V_{CE} = 5.0 \text{ V}$, $I_C = 100 \mu\text{A}$		0.9	0.6	V
High level input voltage	V_{IH} **	$V_{CE} = 0.2 \text{ V}$, $I_C = 5.0 \text{ mA}$	3.0	1.5		V
Input resistance	R_1		3.29	4.7	6.11	$\text{k}\Omega$
E-to-B resistance	R_2		7	10	13	$\text{k}\Omega$
Turn-on time	t_{on}	$V_{CC} = 5 \text{ V}$, $R_L = 1 \text{ k}\Omega$			0.2	μs
Storage time	t_{stg}	$V_i = 5 \text{ V}$, $PW = 2 \mu\text{s}$			5.0	μs
Turn-off time	t_{off}	duty cycle $\leq 2 \%$			6.0	μs

** $PW \leq 350 \mu\text{s}$, duty cycle $\leq 2 \%$

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TYPICAL CHARACTERISTICS (T_a = 25°C)





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