

UHF linear push-pull power transistor

BLV62

FEATURES

- Internal matching for an optimum wideband capability and high gain
- Poly-silicon emitter-ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

Two npn silicon planar epitaxial sections in push-pull structure, intended for use in linear television transmitters (vision or sound).

The device is encapsulated in a 4-lead SOT262A2 flange envelope with 2 ceramic caps. The common emitter is connected to the flange.

PINNING - SOT262A2

PIN	DESCRIPTION
1	collector 1
2	collector 2
3	base 1
4	base 2
5	emitter

QUICK REFERENCE DATA

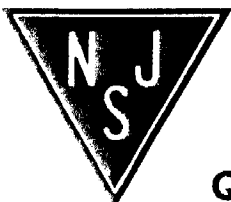
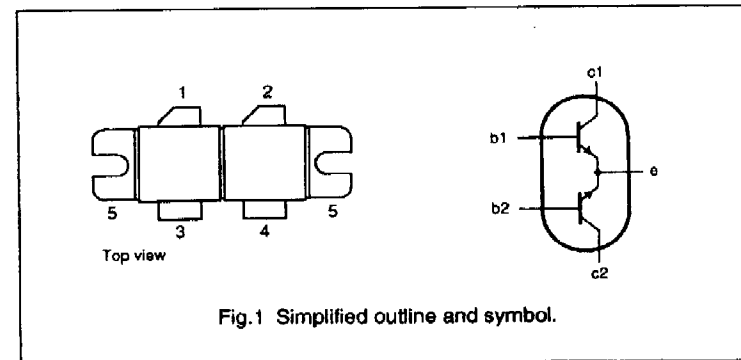
RF performance at $T_h = 25^\circ\text{C}$ in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_c (%)	ΔG_p (dB) (note 1)
c.w. class-AB	860	28	150	> 8.5 typ. 9.5	> 45 typ. 50	< 1 typ. 0.5

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% sync input/25% sync output compression in television service (negative modulation, CCIR system).

PIN CONFIGURATION



NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

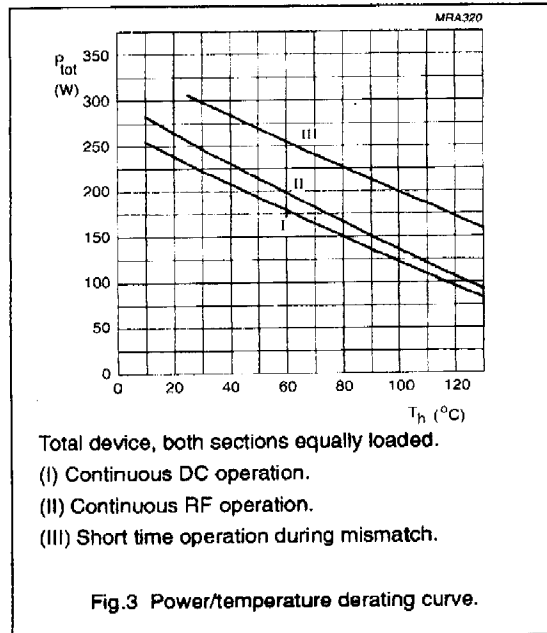
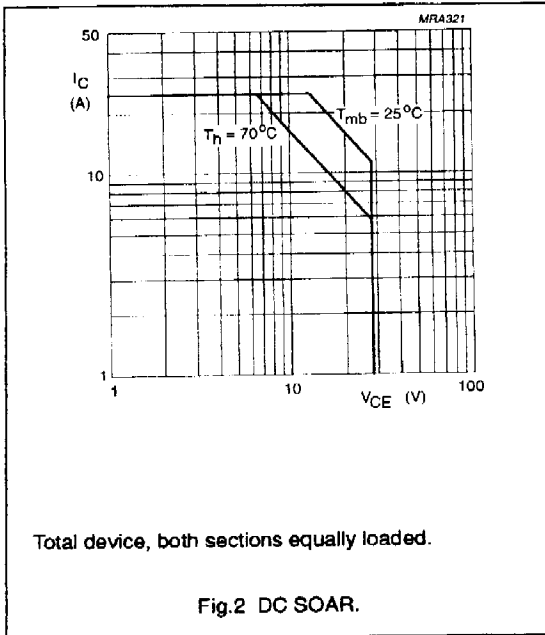
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LIMITING VALUES (per transistor section unless otherwise specified)
 In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	-	60	V
V_{CEO}	collector-emitter voltage	open base	-	28	V
V_{EBO}	emitter-base voltage	open collector	-	3	V
$I_C, I_{C(AV)}$	collector current	DC or average value	-	12.5	A
P_{tot}	total power dissipation	DC operation; $T_{mb} = 25^\circ\text{C}$ (note 1)	-	320	W
T_{stg}	storage temperature range		-65	150	$^\circ\text{C}$
T_j	junction operating temperature		-	200	$^\circ\text{C}$

Note

1. Total device, both sections equally loaded.



THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
$R_{th(j-mb)(DC)}$	from junction to mounting base	$P_{tot} = 320 \text{ W};$ $T_{mb} = 25 \text{ }^\circ\text{C}$ (note 1)	0.55	K/W
$R_{th(j-mb)(RF)}$	from junction to mounting base	$P_{tot} = 350 \text{ W};$ $T_{mb} = 25 \text{ }^\circ\text{C}$ (note 1)	0.5	K/W
$R_{th(mb-h)}$	from mounting base to heatsink	(note 1)	0.15	K/W

Note

1. Total device, both sections equally loaded.

CHARACTERISTICS

Values apply to either transistor section; $T_j = 25 \text{ }^\circ\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; $I_C = 60 \text{ mA}$	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; $I_C = 150 \text{ mA}$	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; $I_E = 3 \text{ mA}$	3	–	–	V
I_{CES}	collector-emitter leakage current	$V_{BE} = 0;$ $V_{CE} = 28 \text{ V}$	–	–	30	mA
h_{FE}	DC current gain	$V_{CE} = 25 \text{ V};$ $I_C = 4.5 \text{ A}$	30	–	–	
Δh_{FE}	DC current gain ratio of both sections	$V_{CE} = 25 \text{ V};$ $I_C = 4.5 \text{ A}$	0.67	–	1.5	
C_c	collector capacitance	$V_{CB} = 28 \text{ V};$ $I_E = I_C = 0;$ $f = 1 \text{ MHz}$	–	81	–	pF
C_{c-f}	collector-flange capacitance	$f = 1 \text{ MHz}$	–	5.7	–	pF

