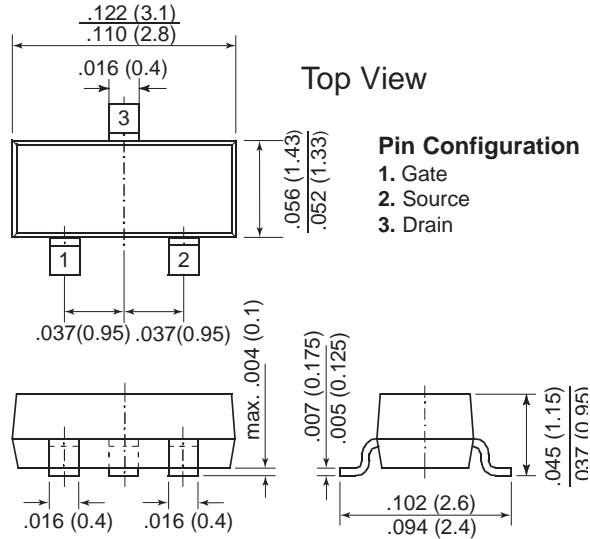


## DMOS Transistors (P-Channel)

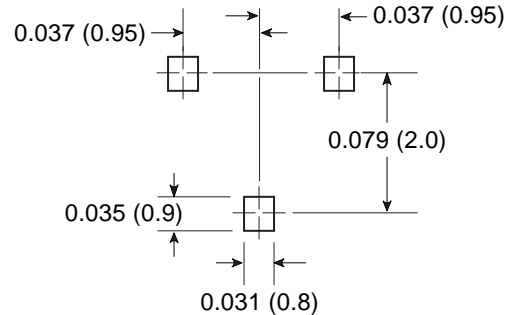


### TO-263AB (SOT-23)



Dimensions in inches and (millimeters)

### Mounting Pad Layout



## Features

- High input impedance
- High-speed switching
- No minority carrier storage time
- CMOS logic compatible input
- No thermal runaway
- No secondary breakdown

## Mechanical Data

**Case:** SOT-23 Plastic Package

**Weight:** approx. 0.008 grams

**Packaging Codes/Options:**

E8/10K per 13" reel (8mm tape), 30K/box

E9/3K per 7" reel (8mm tape), 30K/box

## Maximum Ratings and Thermal Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	-V <sub>DSS</sub>	60	V
Drain-Gate Voltage	-V <sub>DGS</sub>	60	V
Gate-Source-Voltage (pulsed)	V <sub>GS</sub>	±20	V
Drain Current (continuous)	-I <sub>D</sub>	250	mA
Power Dissipation at T <sub>SB</sub> = 50°C	P <sub>tot</sub>	0.310 <sup>(1)</sup>	W
Thermal Resistance Junction to Substrate Backside	R <sub>θSB</sub>	320 <sup>(1)</sup>	°C/W
Thermal Resistance Junction to Ambient Air	R <sub>θJA</sub>	450 <sup>(1)</sup>	°C/W
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature Range	T <sub>S</sub>	-65 to +150	°C

**Note:**

(1) Device on Fiberglass Substrate, see layout on second page

## DMOS Transistors (P-Channel)

### Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	-V <sub>(BR)DSS</sub>	-I <sub>D</sub> = 100μA, V <sub>GS</sub> = 0	60	90	—	V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , -I <sub>D</sub> = 1mA	1.0	2.0	3.0	V
Gate-Body Leakage Current	-I <sub>GSS</sub>	-V <sub>GS</sub> = 15V, V <sub>DS</sub> = 0	—	—	10	nA
Drain Cutoff Current	-I <sub>DSS</sub>	-V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0	—	—	0.5	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	-V <sub>GS</sub> = 10V, -I <sub>D</sub> = 200mA	—	3.5	5.0	Ω
Forward Transconductance	g <sub>m</sub>	-V <sub>DS</sub> = 10V, -I <sub>D</sub> = 200mA, f = 1MHz	—	200	—	mS
Input Capacitance	C <sub>iss</sub>	-V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0, f = 1MHz	—	60	—	pF
Turn-On Time	t <sub>on</sub>	-V <sub>GS</sub> = 10V, -V <sub>DS</sub> = 10V	—	5	—	ns
Turn-Off Time	t <sub>off</sub>	R <sub>D</sub> = 100Ω	—	25	—	ns

**Note:**

(1) Device on fiberglass substrate, see layout

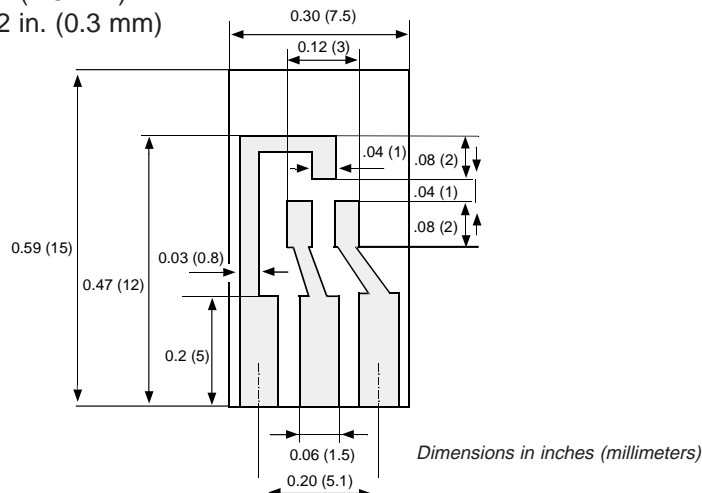
### Inverse Diode

Parameters	Symbol	Test Condition	Value	Unit
Max. Forward Current (continuous)	I <sub>F</sub>	T <sub>amb</sub> = 25°C	0.3	A
Forward Voltage Drop (typ.)	V <sub>F</sub>	V <sub>GS</sub> = 0, I <sub>F</sub> = 0.12A T <sub>j</sub> = 25°C	0.85	V

### Layout for R<sub>thJA</sub> test

Thickness: Fiberglass 0.059 in. (1.5 mm)

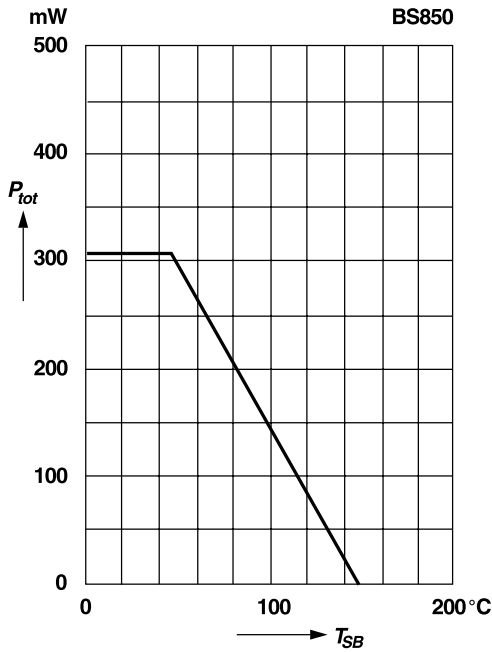
Copper leads 0.012 in. (0.3 mm)



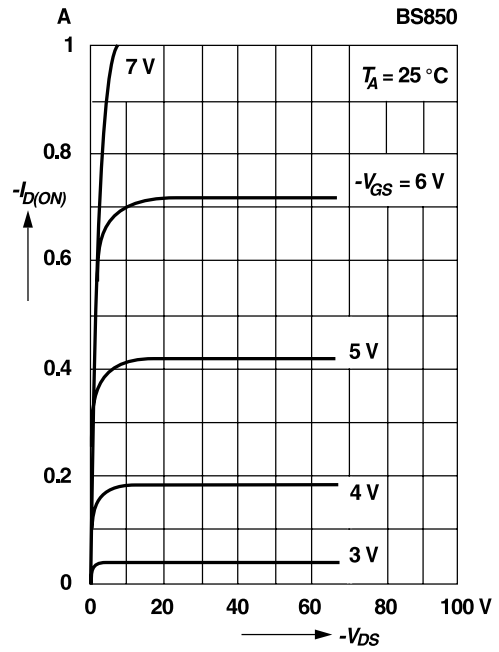
DMOS Transistors (P-Channel)

Ratings and Characteristic Curves ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

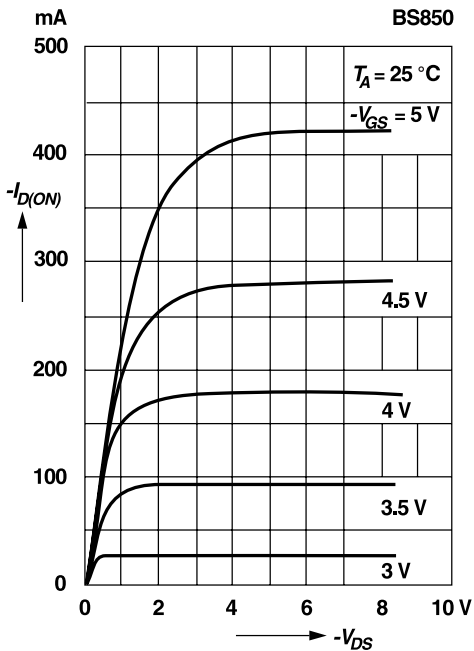
**Admissible power dissipation versus temperature of substrate backside**  
 Device on fiberglass substrate, see layout



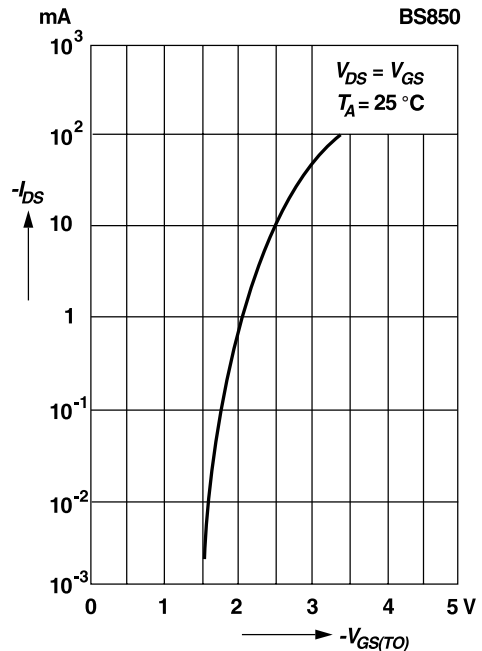
**Output characteristics**  
 Pulse test width 80 ms; pulse duty factor 1%



**Saturation characteristics**  
 Pulse test width 80 ms; pulse duty factor 1%



**Drain-source current versus gate threshold voltage**

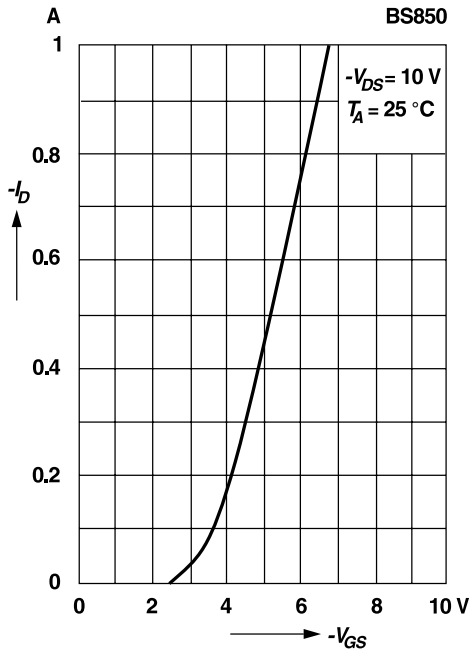


DMOS Transistors (P-Channel)

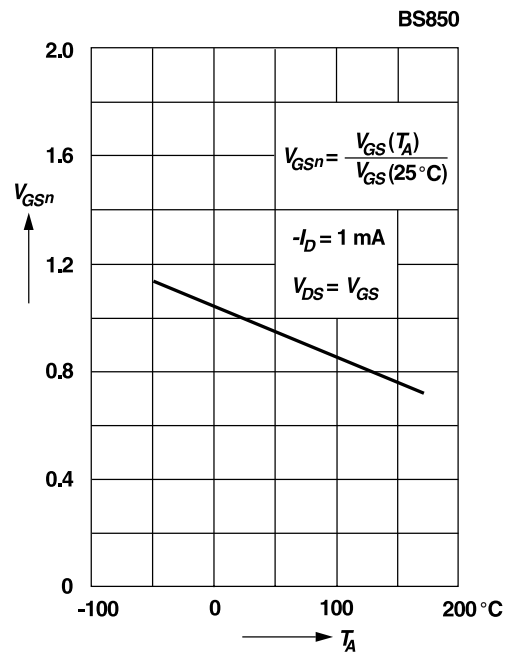
Ratings and Characteristic Curves (T<sub>A</sub> = 25°C unless otherwise noted)

Drain current versus gate-source voltage

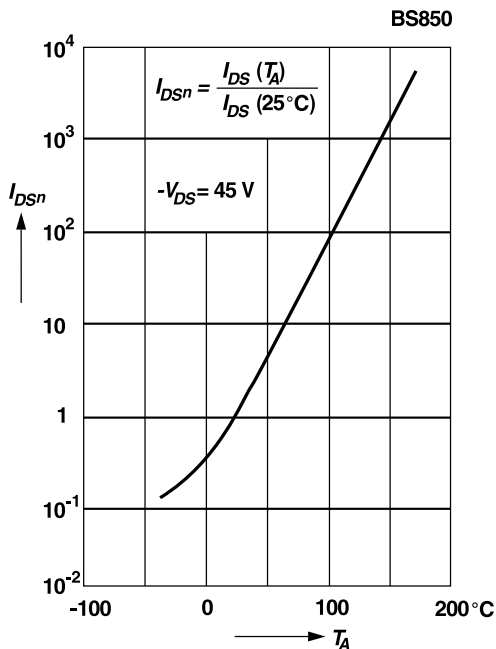
Pulse test width 80 ms; pulse duty factor 1%



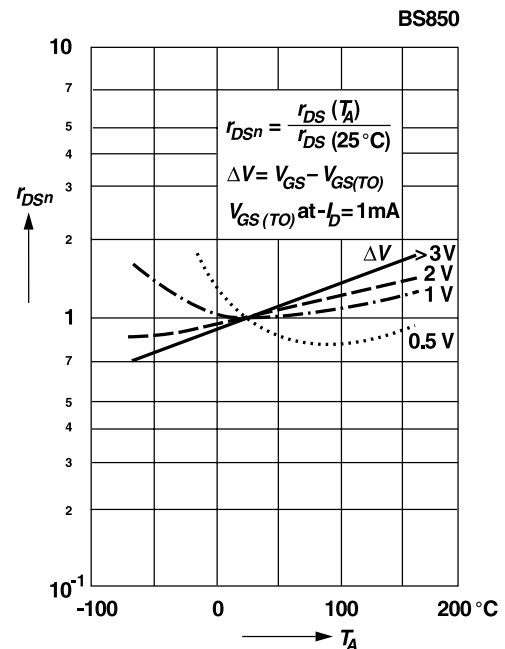
Normalized gate-source voltage versus temperature



Normalized drain-source current versus temperature



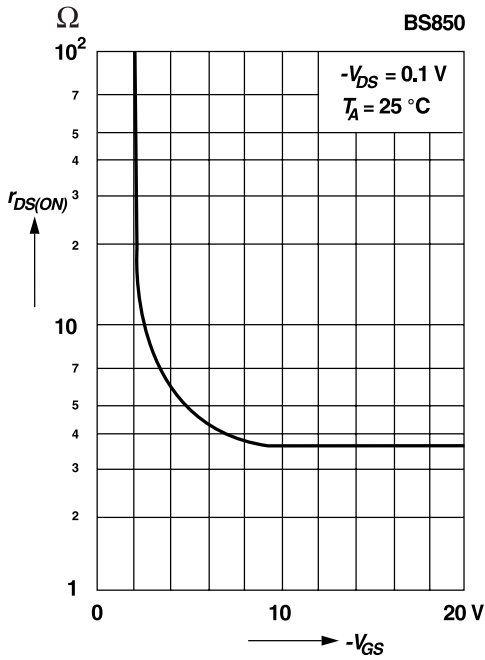
Normalized drain-source resistance versus temperature



DMOS Transistors (P-Channel)

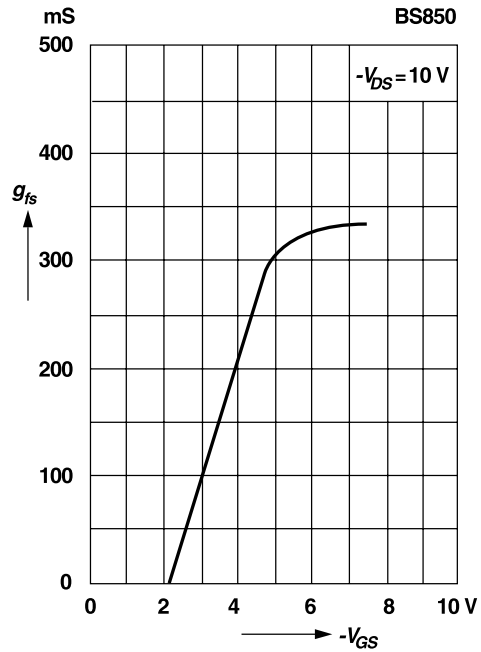
Ratings and Characteristic Curves (T<sub>A</sub> = 25°C unless otherwise noted)

Drain-source resistance versus gate-source voltage



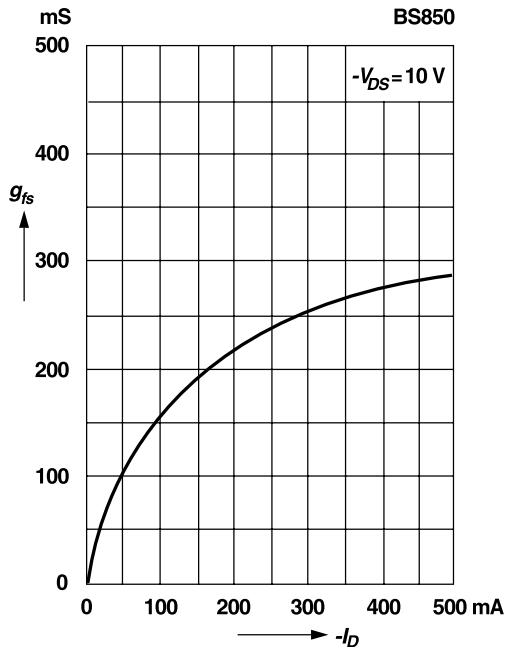
Transconductance versus gate-source voltage

Pulse test width 80 ms; pulse duty factor 1%



Transconductance versus drain current

Pulse test width 80 ms; pulse duty factor 1%



Capacitance versus drain-source voltage

