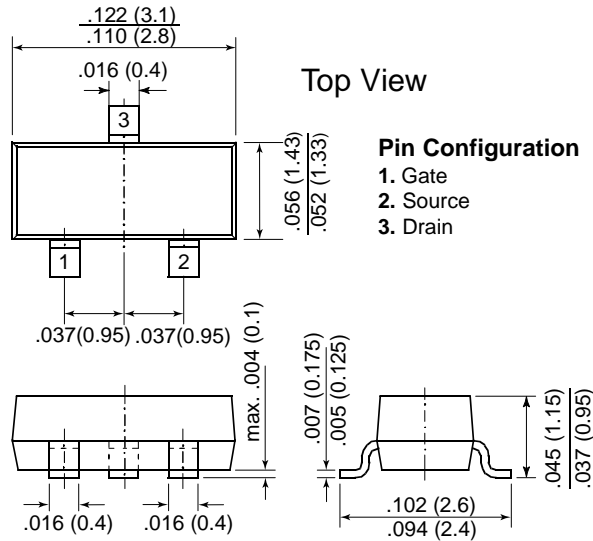


DMOS Transistor (N-Channel)

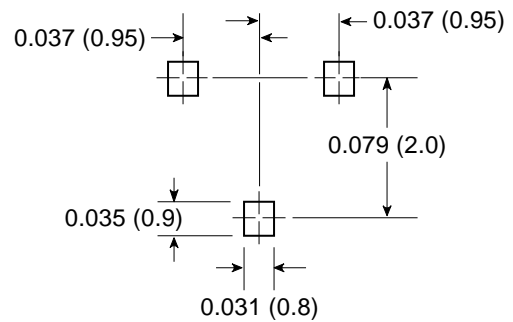


TO-236AB (SOT-23)



Dimensions in inches and (millimeters)

Mounting Pad Layout



Features

- High input impedance
- High-speed switching
- No minority carrier storage time
- CMOS logic compatible input
- No thermal runaway
- No secondary breakdown

Mechanical Data

Case: SOT-23 Plastic Package

Weight: approx. 0.008g

Packaging Codes/Options:

- E8/10K per 13" reel (8mm tape), 30K/box
- E9/3K per 7" reel (8mm tape), 30K/box

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DSS}	60	V
Drain-Gate Voltage	V _{DGS}	60	V
Gate-Source-Voltage (pulsed)	V _{GS}	±20	V
Drain Current (continuous)	I _D	250	mA
Power Dissipation at T _{SB} = 50°C	P _{tot}	0.310 ⁽¹⁾	W
Thermal Resistance Junction to Substrate Backside	R _{θSB}	320 ⁽¹⁾	°C/W
Thermal Resistance Junction to Ambient Air	R _{θJA}	450 ⁽¹⁾	°C/W
Junction Temperature	T _j	150	°C
Storage Temperature Range	T _s	-65 to +150	°C

Note: (1) Ceramic Substrate 0.7mm; 2.5 cm² area

DMOS Transistors (N-Channel)

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = 100\mu\text{A}, V_{GS} = 0$	60	80	—	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$	1.0	2.0	3.0	
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = 15\text{V}, V_{DS} = 0\text{V}$	—	—	10	nA
Drain Cutoff Current	I_{DSS}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$	—	—	0.5	μA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 200\text{mA}$	—	3.5	5.0	Ω
Forward Transconductance	g_m	$V_{DS} = 10\text{V}, I_D = 200\text{mA}, f = 1\text{MHz}$	—	200	—	mS
Input Capacitance	C_{iss}	$V_{DS} = 10\text{V}, V_{GS} = 0, f = 1\text{MHz}$	—	30	—	pF
Turn-On Time	t_{on}	$V_{GS} = 10\text{V}, V_{DS} = 10\text{V}$	—	5	—	ns
Turn-Off Time	t_{off}	$R_D = 100\Omega$	—	25	—	

Note:

(1) Device on fiberglass substrate, see layout

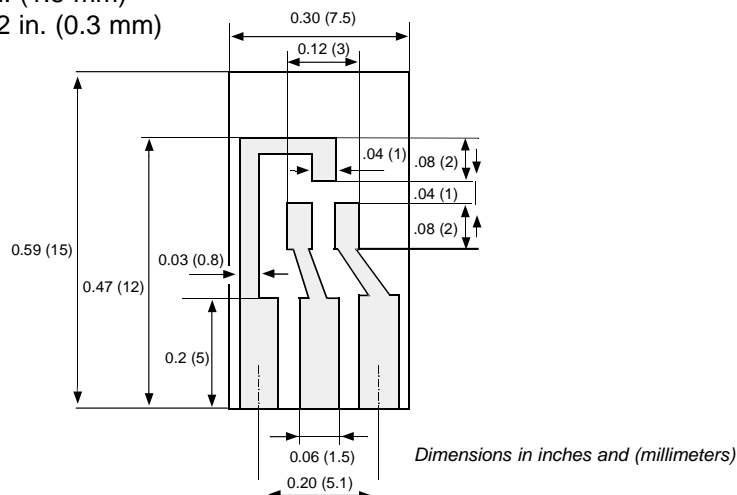
Inverse Diode

Parameter	Symbol	Test Condition	Value	Unit
Max. Forward Current (continuous)	I_F	$T_{amb} = 25^\circ\text{C}$	0.3	A
Forward Voltage Drop (typ.)	V_F	$V_{GS} = 0\text{V}, I_F = 0.3\text{A}, T_J = 25^\circ\text{C}$	0.85	V

Layout for R_{thJA} test

Thickness: Fiberglass 0.059 in. (1.5 mm)

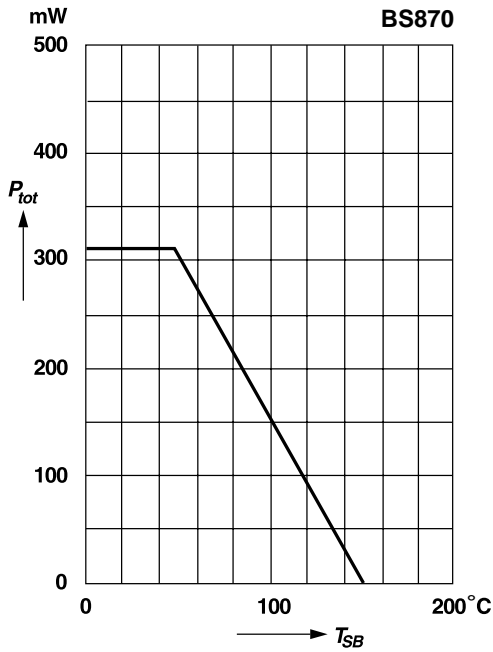
Copper leads 0.012 in. (0.3 mm)



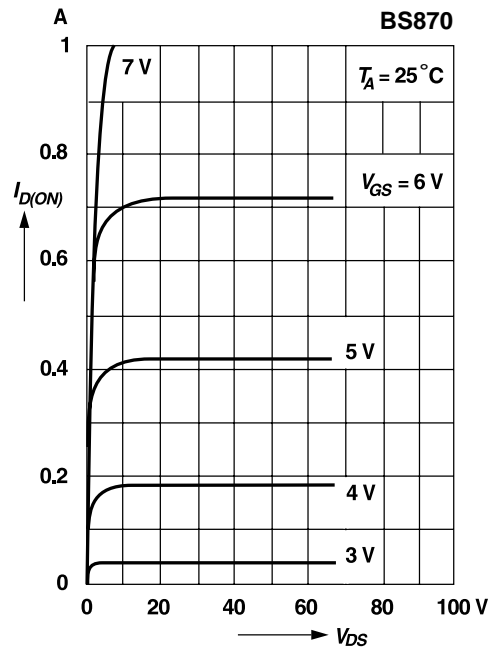
DMOS Transistors (N-Channel)

Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

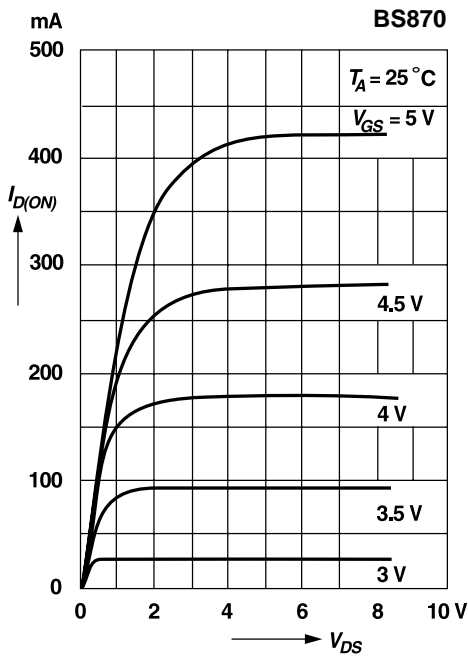
Admissible power dissipation versus temperature of substrate backside
 Device on fiberglass substrate, see layout



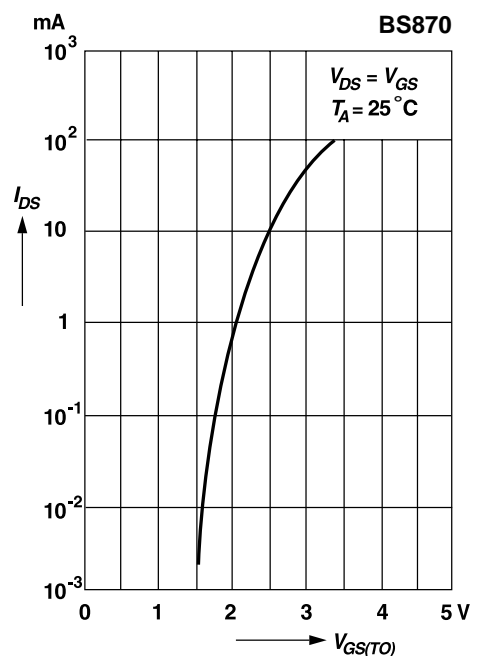
Output characteristics
 Pulse test width 80 ms; pulse duty factor 1%.



Saturation characteristics
 Pulse test width 80 ms; pulse duty factor 1%.



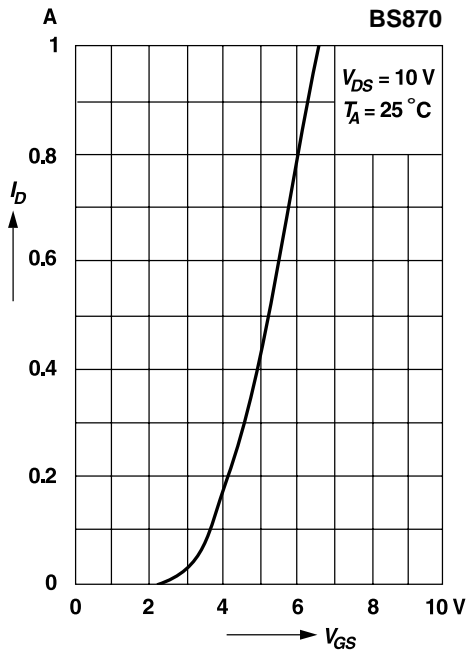
Drain-source current versus gate threshold voltage



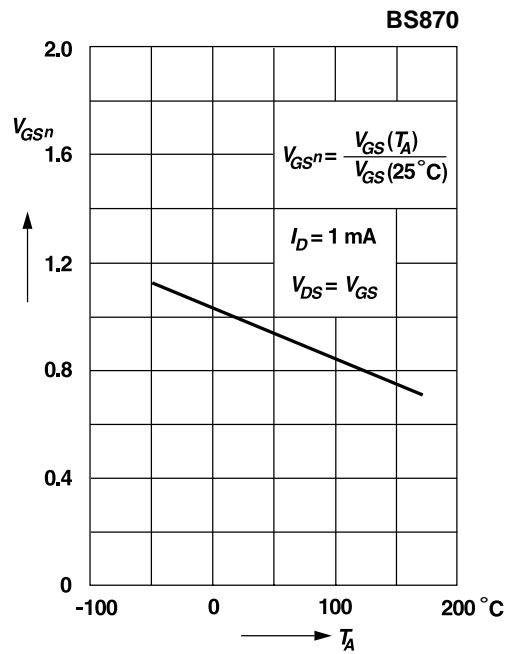
DMOS Transistors (N-Channel)

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

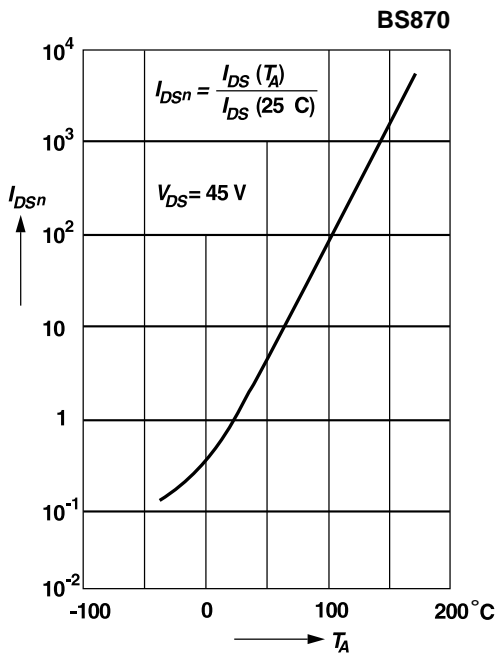
Drain current versus gate-source voltage
Pulse test width 80 ms; pulse duty factor 1%.



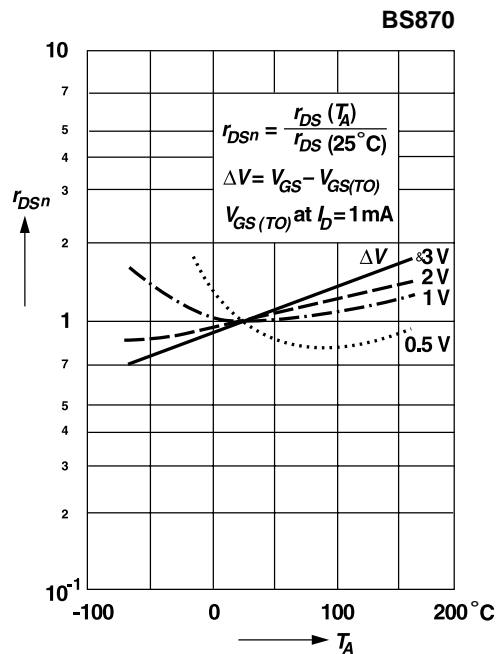
Normalized gate-source voltage versus temperature



Normalized drain-source current versus temperature



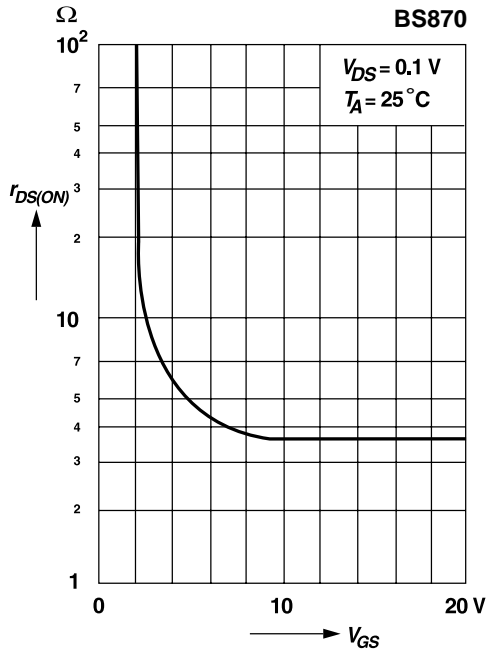
Normalized drain-source resistance versus temperature



DMOS Transistors (N-Channel)

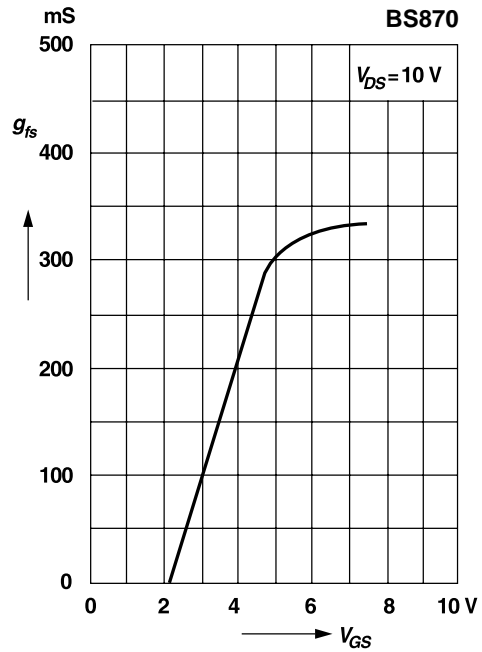
Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Drain-source resistance versus gate-source voltage



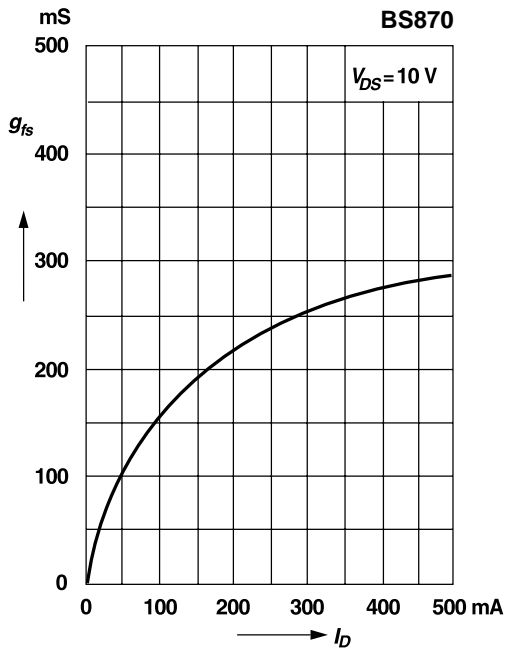
Transconductance versus gate-source voltage

Pulse test width 80 ms; pulse duty factor 1%



Transconductance versus drain current

Pulse test width 80 ms; pulse duty factor 1%



Capacitance versus drain-source voltage

