42V PowerNet

BUK9226-75A

TrenchMOS™ logic level FET

Rev. 01 — 10 October 2000 Product specification

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™[1] technology, featuring very low on-state resistance.

Product availability:

BUK9226-75A in SOT428 (D-PAK).

2. Features

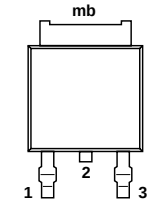
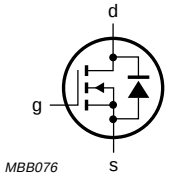
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching
  - 12 V, 24 V and 42 V loads
  - Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		

SOT428 (D-PAK)

1. TrenchMOS is a trademark of Royal Philips Electronics.

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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		–	75	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	–	45	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	114	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A	22.1	26	mΩ
		V_{GS} = 4.5 V; I_D = 25 A	–	29	mΩ

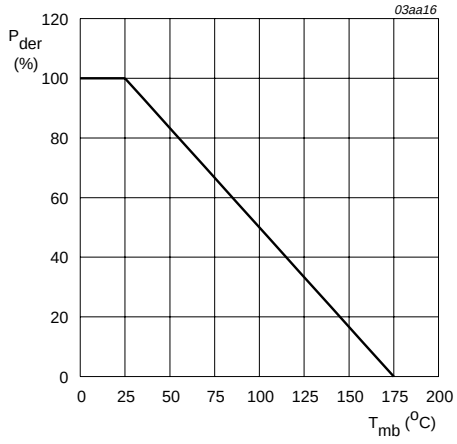
6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

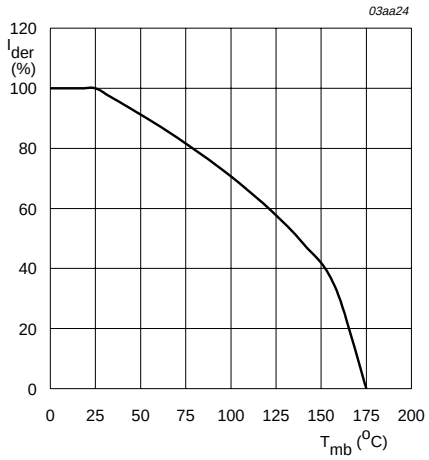
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			–	75	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		–	75	V
V_{GS}	gate-source voltage (DC)			–	±10	V
V_{GSM}	non-repetitive gate-source voltage	$t_p \leq 50$ µs		–	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3		–	45	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2		–	32	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3;	[1]	–	182	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		–	114	W
T_{stg}	storage temperature			–55	+175	°C
T_j	operating junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C		–	45	A
I_{DRM}	pulsed reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		–	182	A
Avalanche ruggedness						
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; I_D = 49 A; $V_{DS} \leq 75$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting T_j = 25°C		–	120	mJ

[1] I_{DM} is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

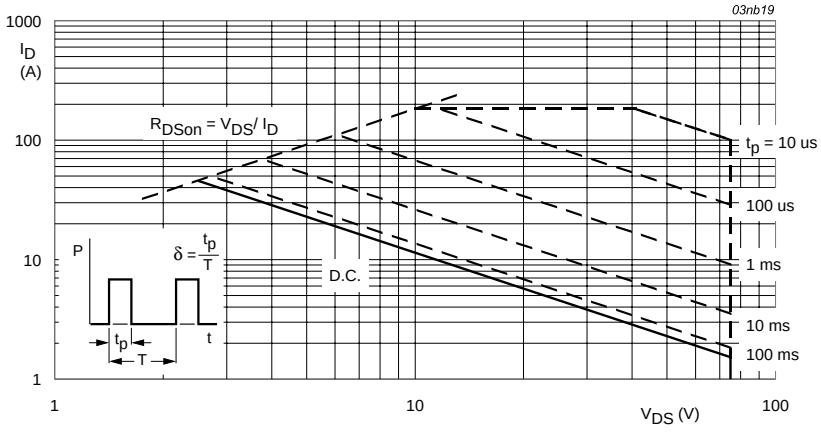
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 4.5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	71.4	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.3	K/W

7.1 Transient thermal impedance

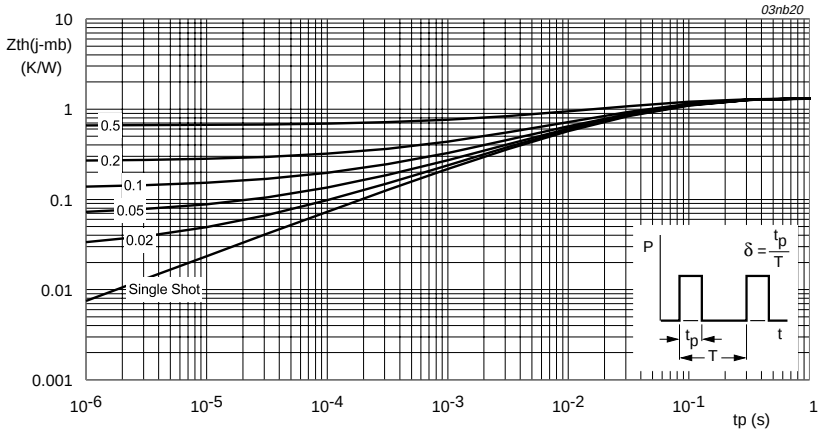


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

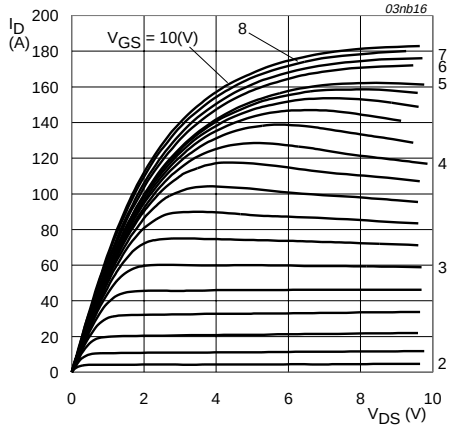
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	75	–	–	V
		T_j = –55 °C	70	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	–	–	V
		T_j = –55 °C	–	–	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	–	0.05	10	µA
		T_j = 175 °C	–	–	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	–	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	–	22.1	26	mΩ
		T_j = 175 °C	–	–	54.6	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C	–	–	29	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	–	20.9	24.6	mΩ
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	–	2340	3120	pF
C_{oss}	output capacitance		–	319	383	pF
C_{rss}	reverse transfer capacitance		–	215	295	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω;	–	24	–	ns
t_r	rise time		–	141	–	ns
$t_{d(off)}$	turn-off delay time		–	142	–	ns
t_f	fall time		–	108	–	ns
L_d	internal drain inductance	measured from drain lead from package to centre of die	–	2.5	–	nH
L_s	internal source inductance	measured from source lead from package to source bond pad	–	7.5	–	nH

Table 5: Characteristics...*continued*

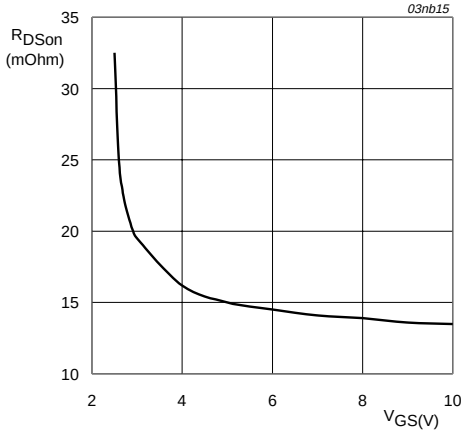
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 15	–	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = –10 V; V_{DS} = 30 V	–	49	–	ns
Q_r	recovered charge		–	115	–	nC



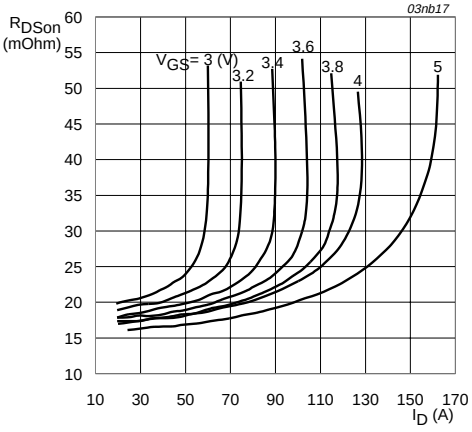
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



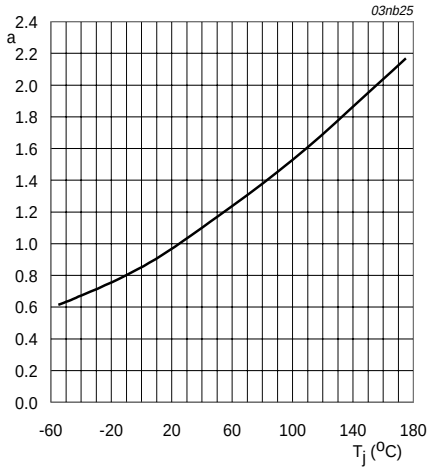
T_j = 25 °C; I_D = 25 A

Fig 6. On-state resistance: typical values.



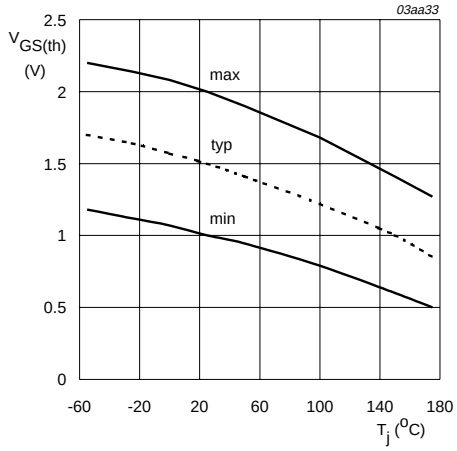
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



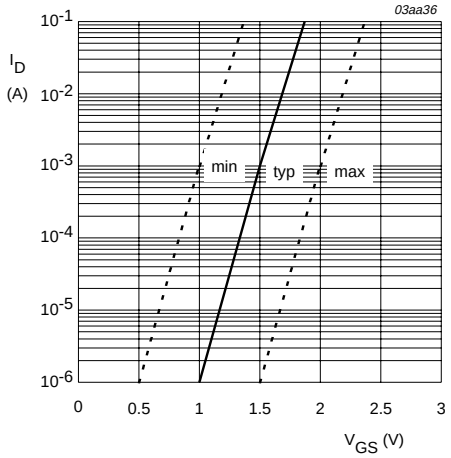
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



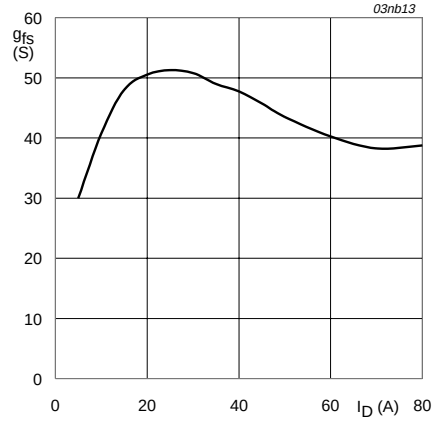
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



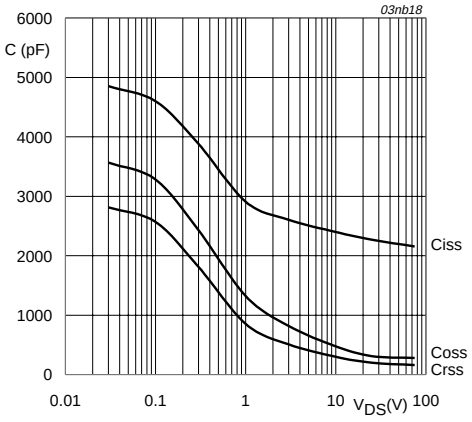
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



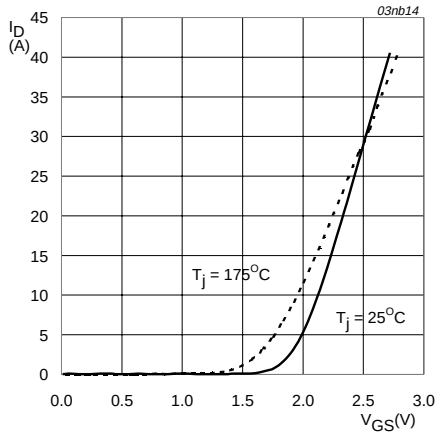
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



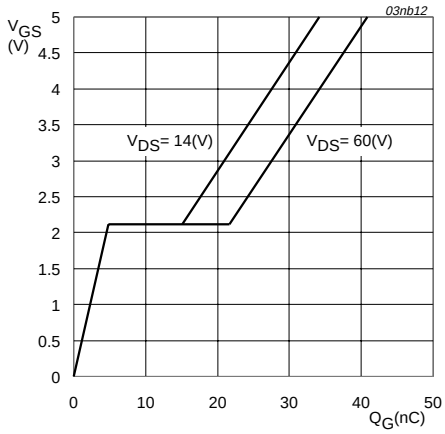
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



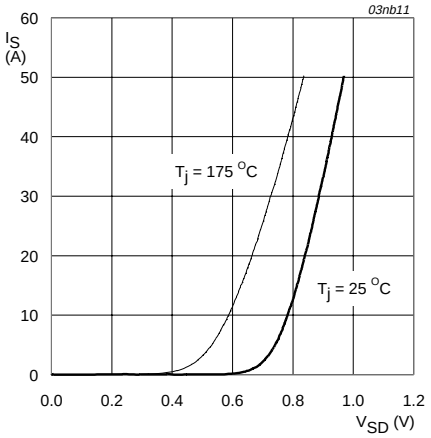
V_{DS} = 25 V

Fig 13. Transfer characteristics; typical values.



T_j = 25 °C; I_D = 25 A

Fig 14. Turn-on gate charge characteristics; typical values.



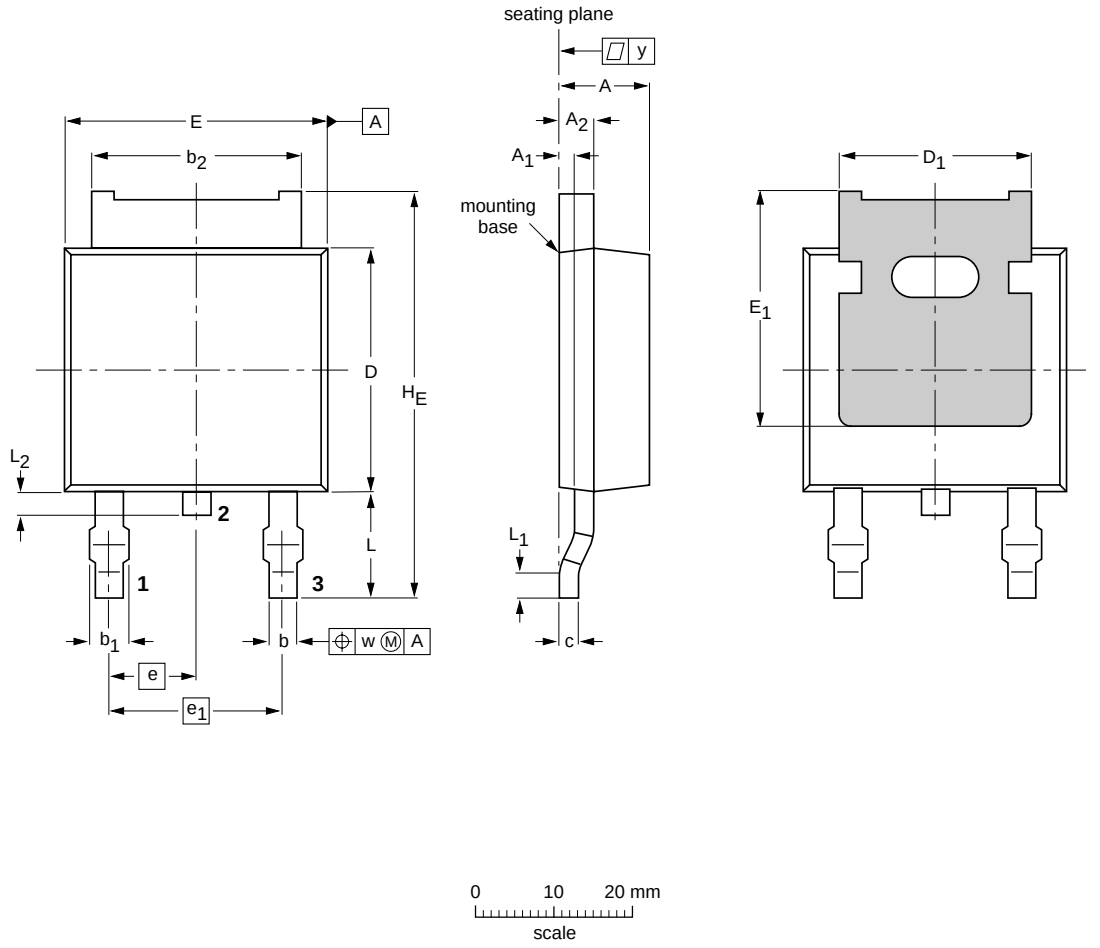
V_{GS} = 0 V

Fig 15. Reverse diode current; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 (1)	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252	SC-63			~~98-04-07~~ 99-09-13

Fig 16. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20001010	-	Product specification; initial version.

11. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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